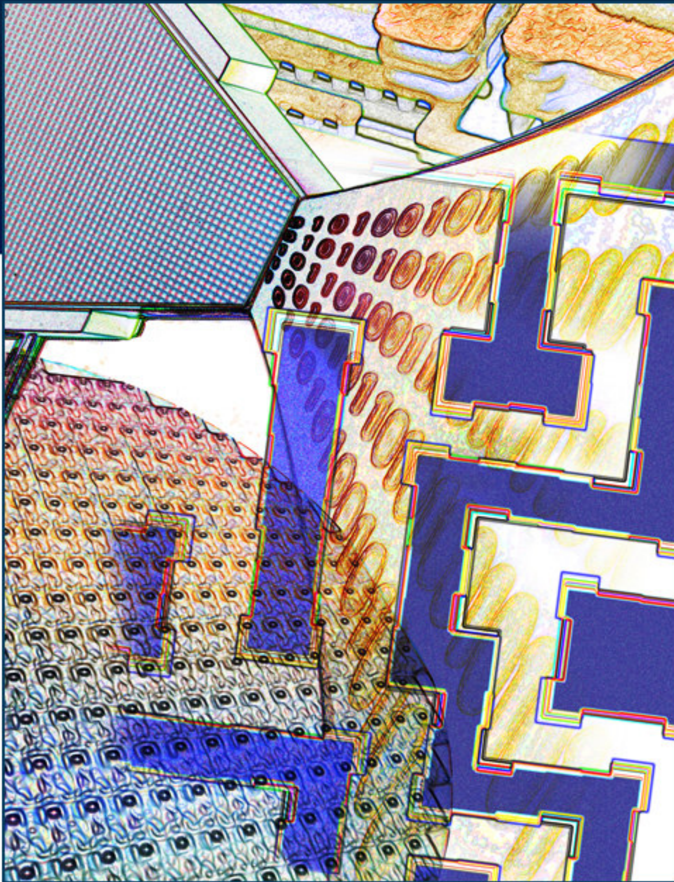
3D-IC System Verification Methodology: Solutions and Challenges



Dusan Petranovic & Karen Chow

Marketing, Design to Silicon Division

April 2011

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I. Introduction
II. Die stacking configurations and descriptions
III. Stack verification methodologies
IV. Example
V. New challenges and future work
VI. Conclusion

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TSV-based 3D-IC Technology

- 3D Integration Drivers
  - Complexity, increasing cost and saturating performance curve of SoC technology
  - Possibility of heterogeneous 3D integration to optimize technology and cost for each chip
  - Improved performance and power
  - Miniaturization - improved capacity/volume ratio

- 3D Integration Issues
  - Reliable, repeatable and cost effective manufacturing
  - Reliable power delivery and on-chip thermal management
  - Lack of methodology and EDA tools to support efficient design (and verification)
  - Lack of test vehicles and data for validation of new solutions

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EDA Challenges

- Physically aware architectural exploration of increasing number of system level options
- Determination of optimal 3D granularity and number of stack levels to achieve performance benefit through 3D integration
- Optimal TSV allocation and congestion management through 3D floor-planning, placement and routing
- Thermal management and thermally aware physical design
- 3D IC related Stress sources and impact on parametric yield
- Power grid design to avoid IR drop and electro-migration problems
- Determination of modeling and extraction accuracy needed to analyze TSV effects and dies interactions and model flow integration
- 3D stack verification and testing
- Application and design domain specific solutions

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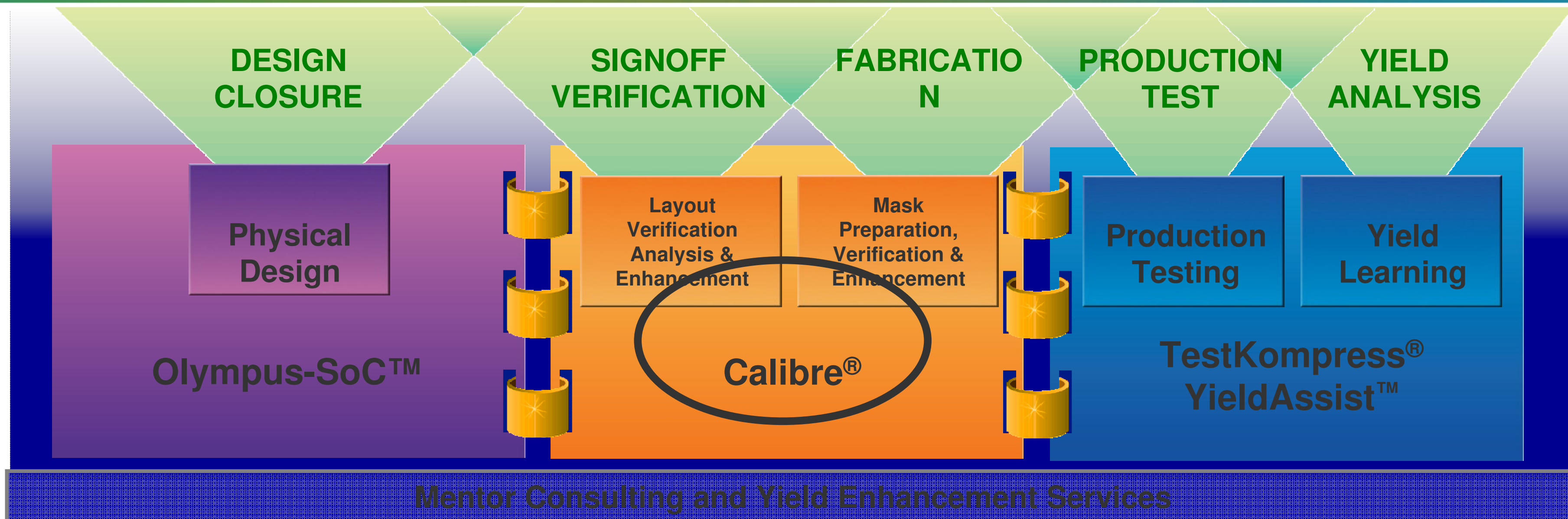
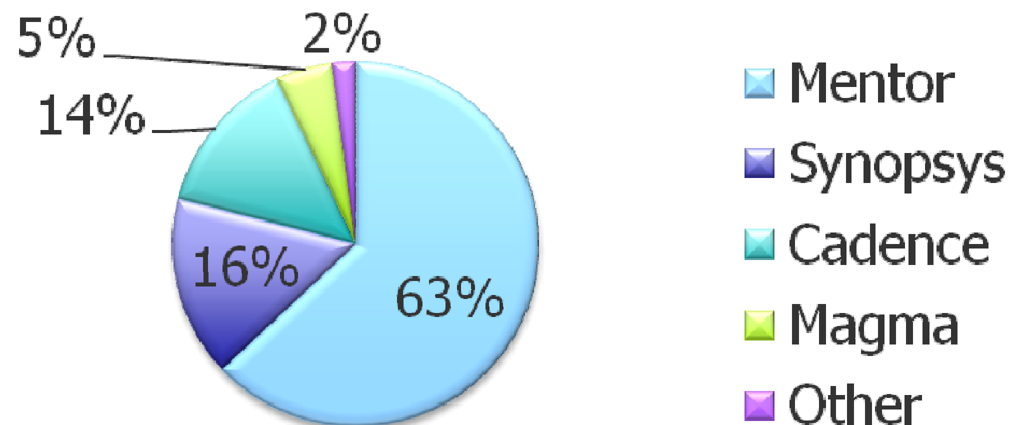
Physical Verification: Mentor's Technology Leadership



Prioritization:

- 3D Verification needs to come first



(Source: Gary Smith EDA, October 2010)

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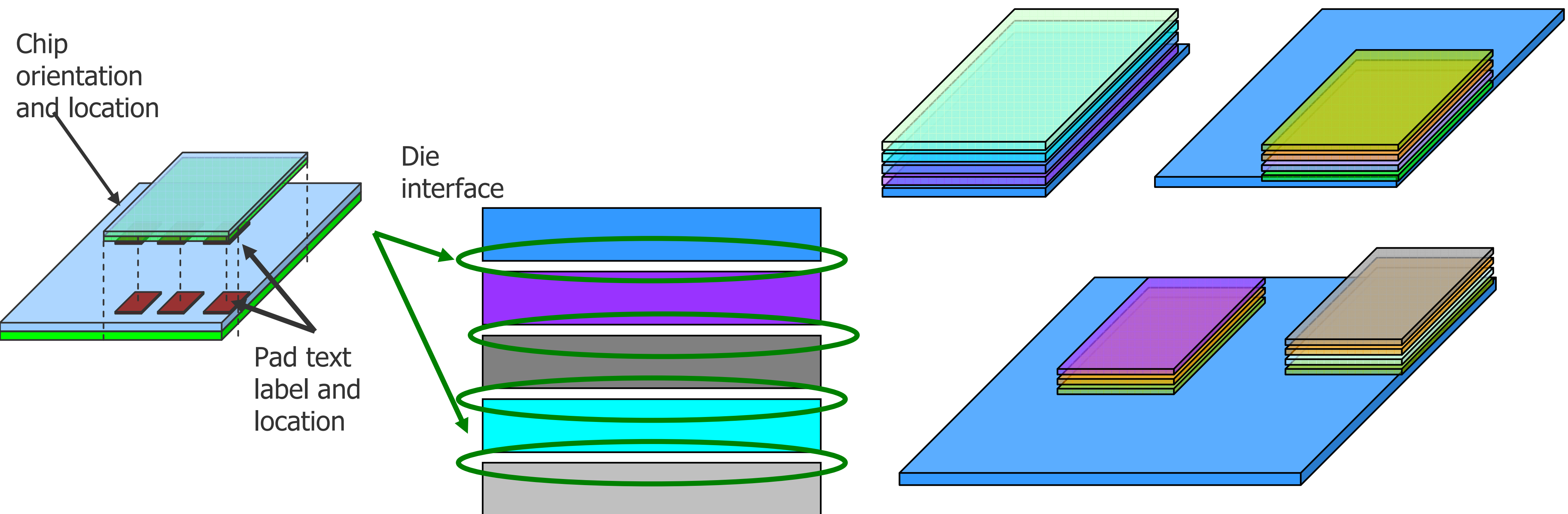
3D-IC Stack Description

- Configuration file to describe 3D-IC Stack
  - Supports various stacking configurations
  - List of Dies with their order number
  - Information of the die position, orientation , rotation
  - Text ports at the bump or pad locations
  - Interface type, geometry and materials



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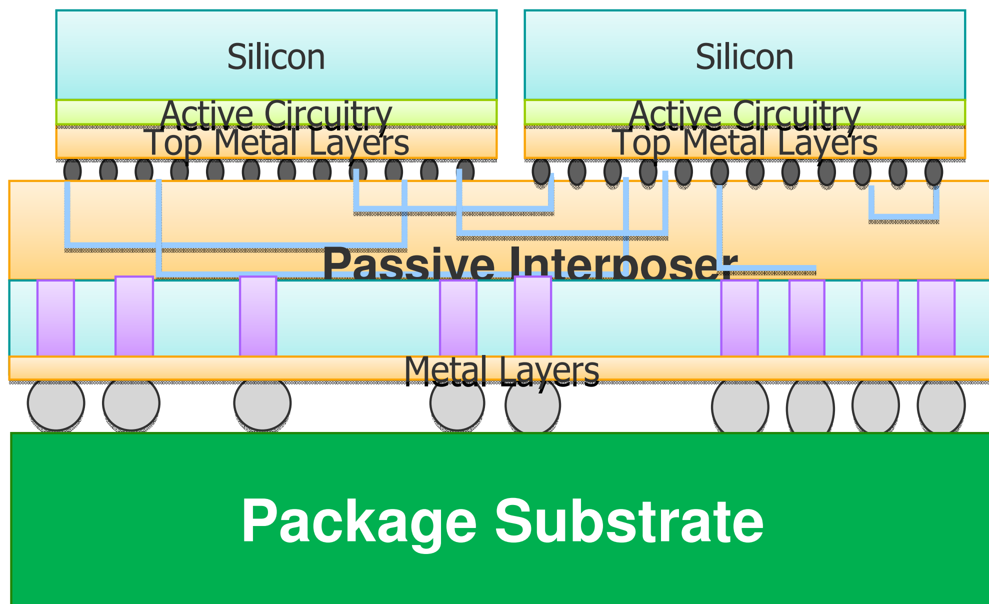
3D-IC Stack Configurations

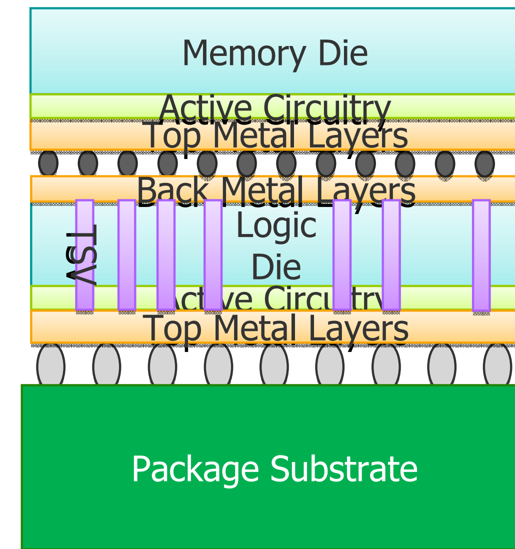
2.5D Stacking, Interposer



Advantage: No on-chip TSVs

Concern: Interposer size and cost

3D Stacking, Die on Die



Advantage: form factor, performance

Concern: TSV integration, thermal, stress

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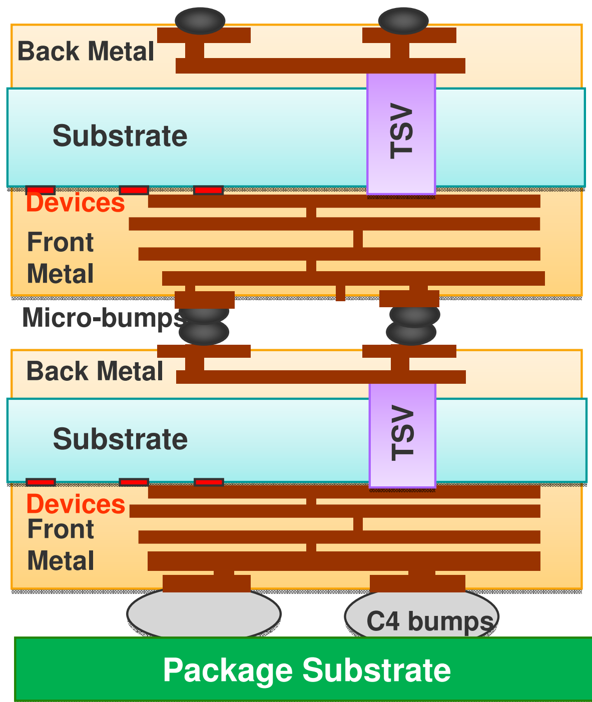
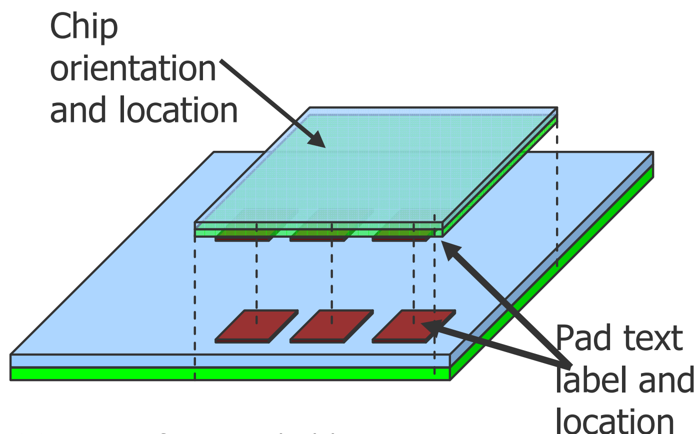
3D-IC DRC/LVS/PEX



- DRC/LVS of the double sided dies in the stack including TSV and backside metal
- TSV as LVS device or as a VIA
- Model of arbitrary complexity supported for TSV in simulation
- Calibration of front and back metal stacks, combined or separated
- Double sided die front and back metal parasitic extraction



- DRC/LVS connectivity check at the die to die or die to interposer interfaces (micro-bumps or pads locations)

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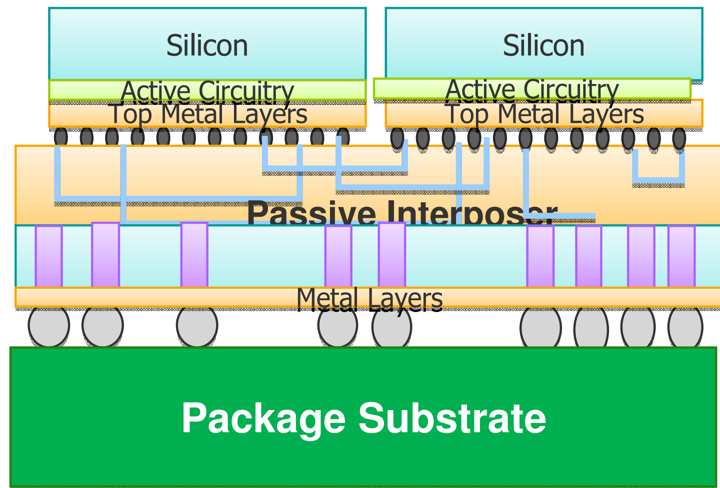
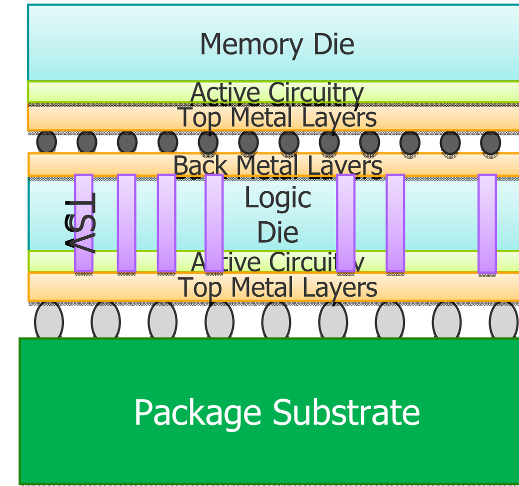
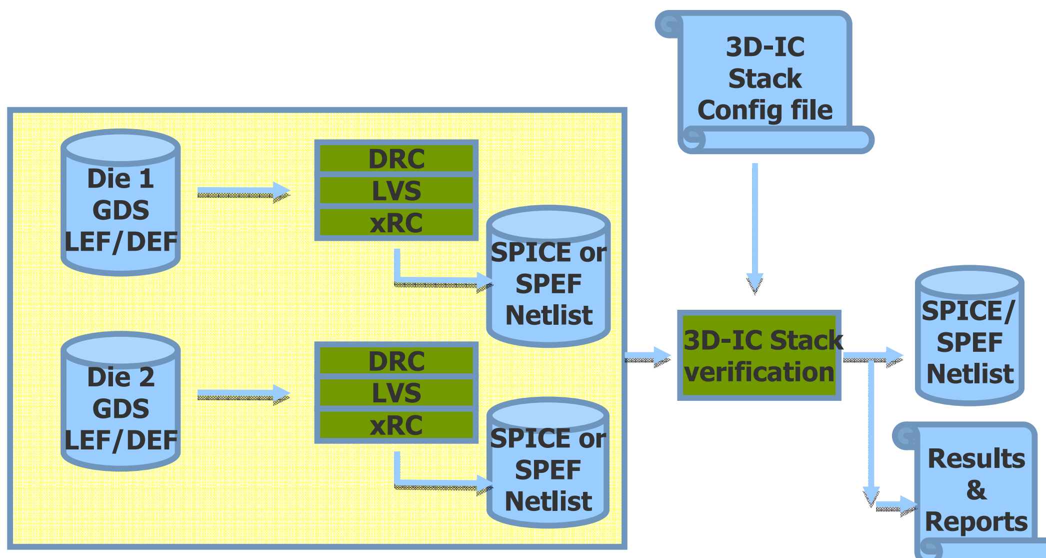
3D-IC Verification Flows







- Single net-list for double sided die including front metal parasitics, TSV and back metal parasitics stack including TSV and backside metal
- Combined netlist, if desired, for simulation across the dies in the stack

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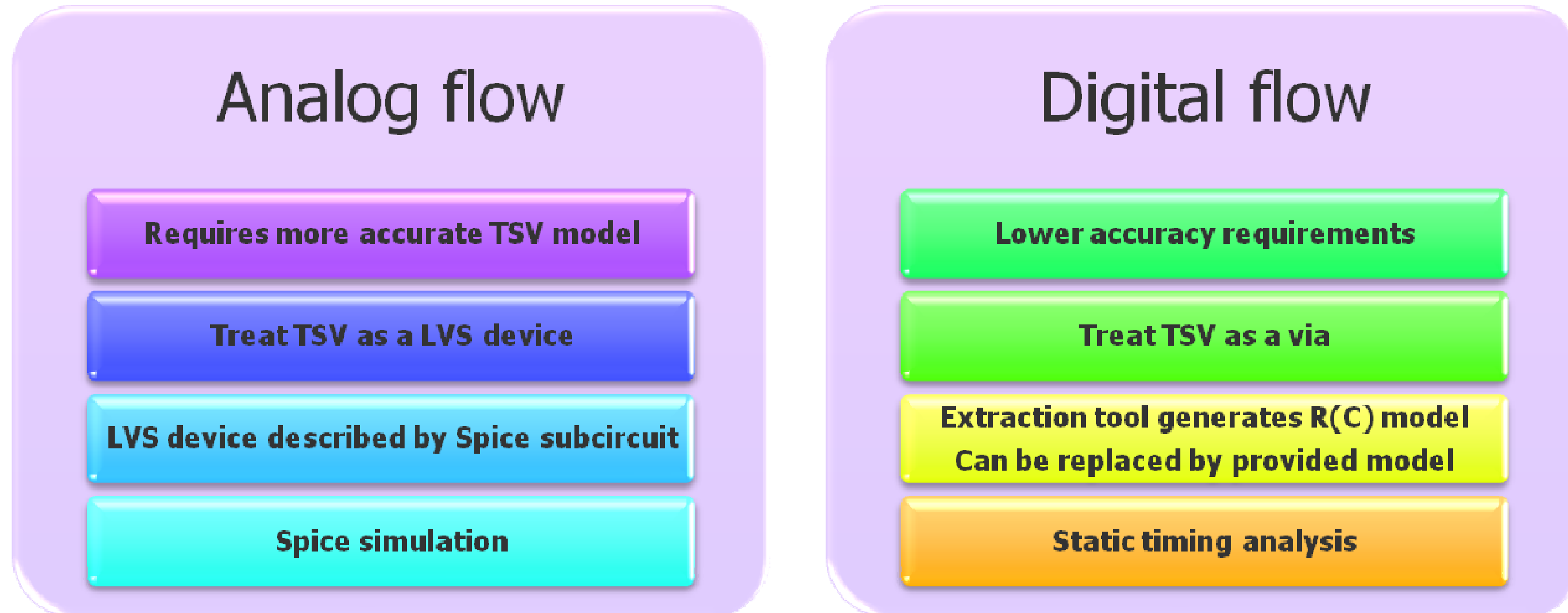
3D-IC Verification Flows: Differences

- Analog (TSV as LVS device) vs. Digital (TSV as a VIA)



- 3D vs. 2.5D Verification
  - LVS/PEX of an interposer requires additional steps in 2.5D
  - Thermal and stress issues more complex for 3D

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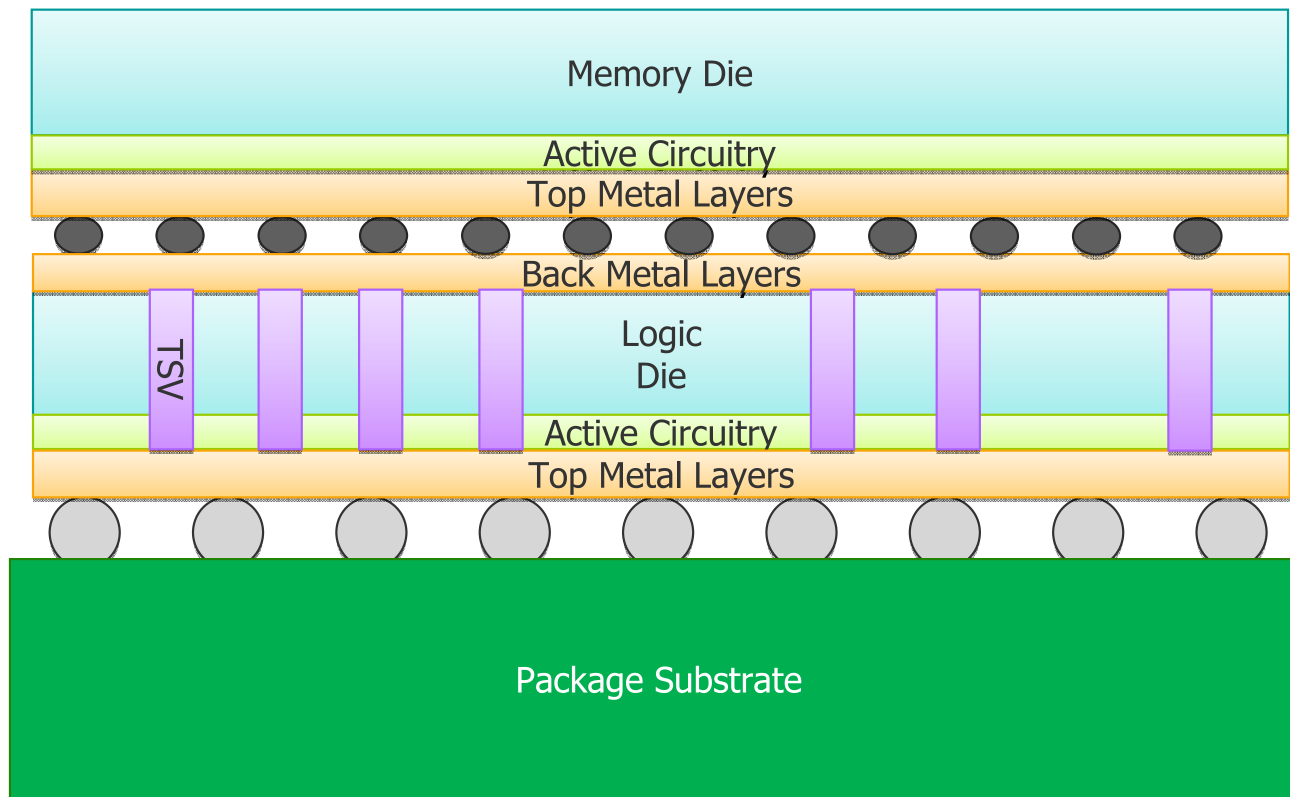
Example

- A 3D-IC was designed using a 65-nm technology, with a logic die, a memory die and micro-bumps connecting the two.



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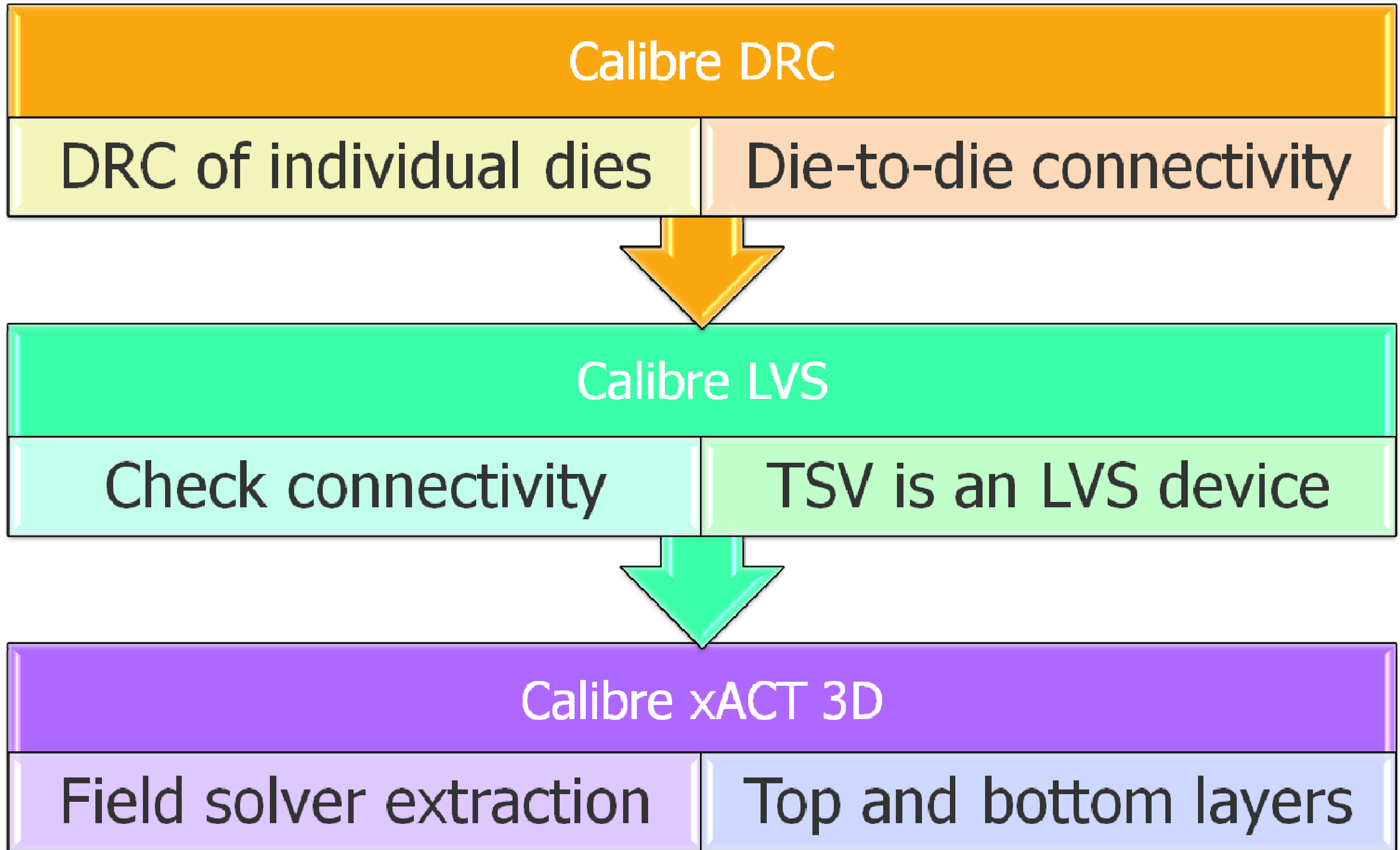
Calibre Verification



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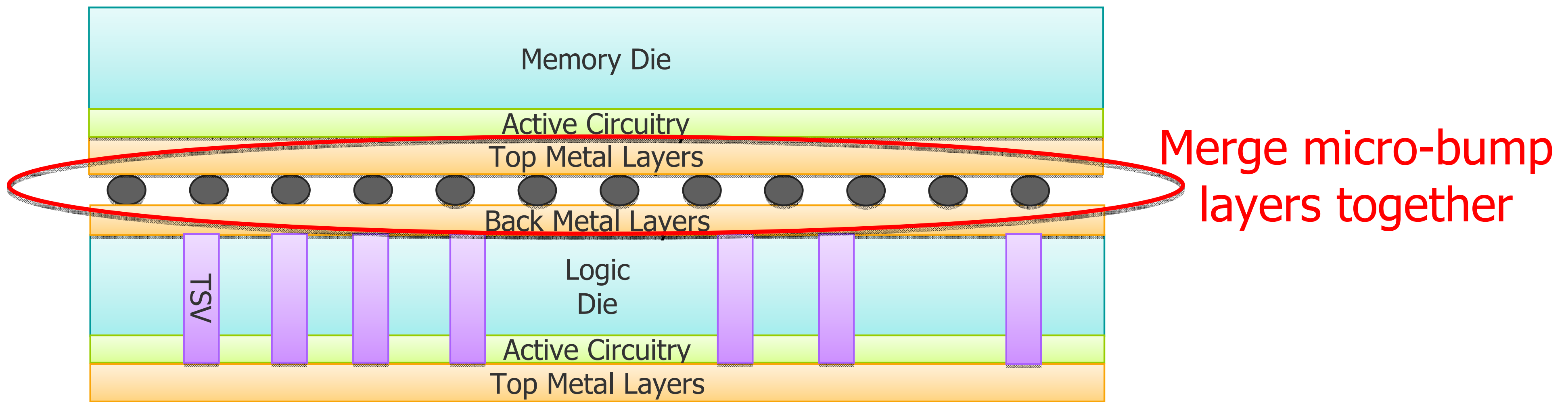
Design Rule Checking

- Step 1: Run Calibre DRC of the logic and memory dies independently
- Step 2: Merge the top metal layer of the memory die, and the back metal layer of the logic die together to check for connectivity errors.



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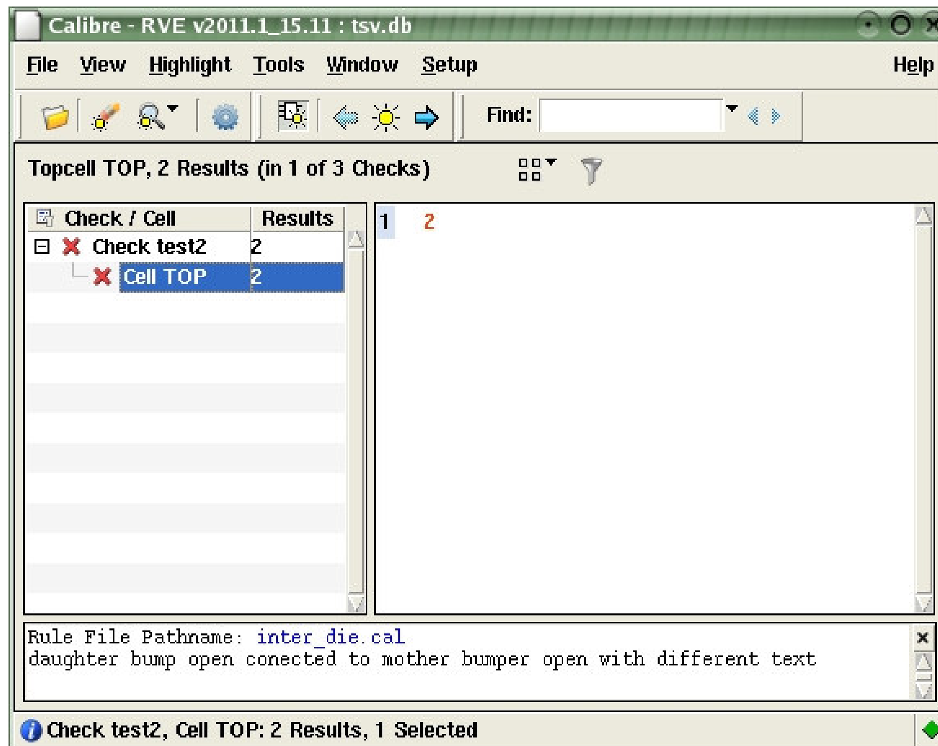
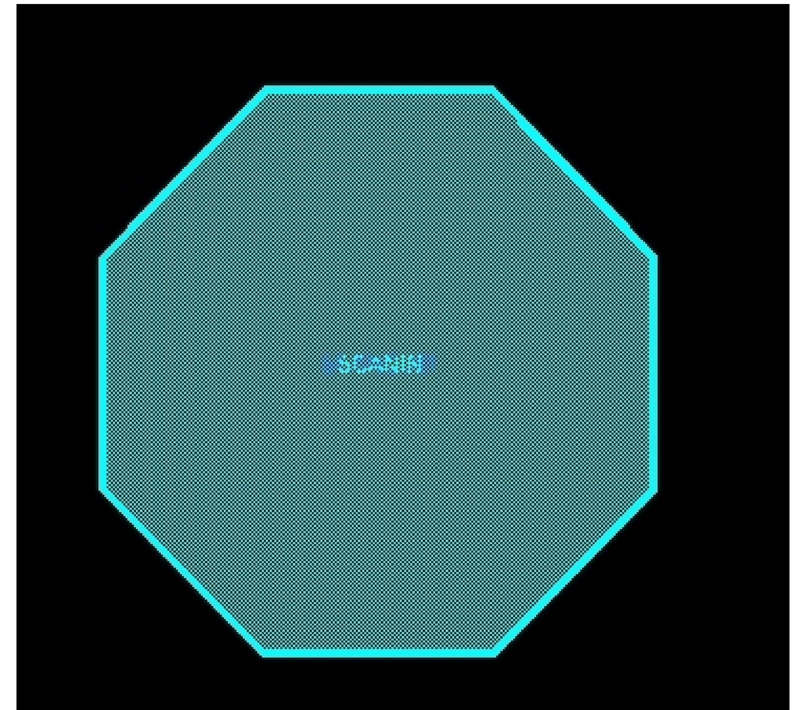
DRC for Alignment and Connectivity Check

- Step 3: Run DRC on the merged gds.
  - The landing pad for both sides of the micro-bump needs to be correctly aligned.
  - The interface connectivity was checked to ensure that the proper nets were connected through the micro-bumps and that the alignment of the logic and memory dies is correct.





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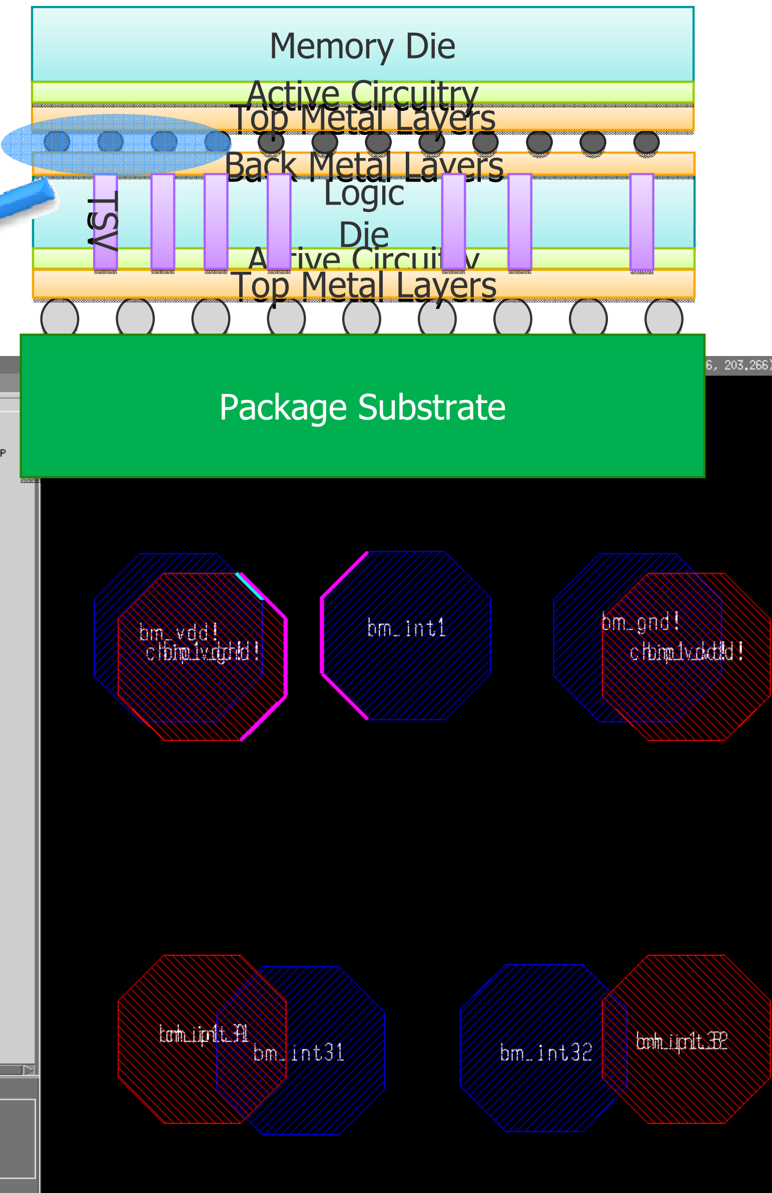
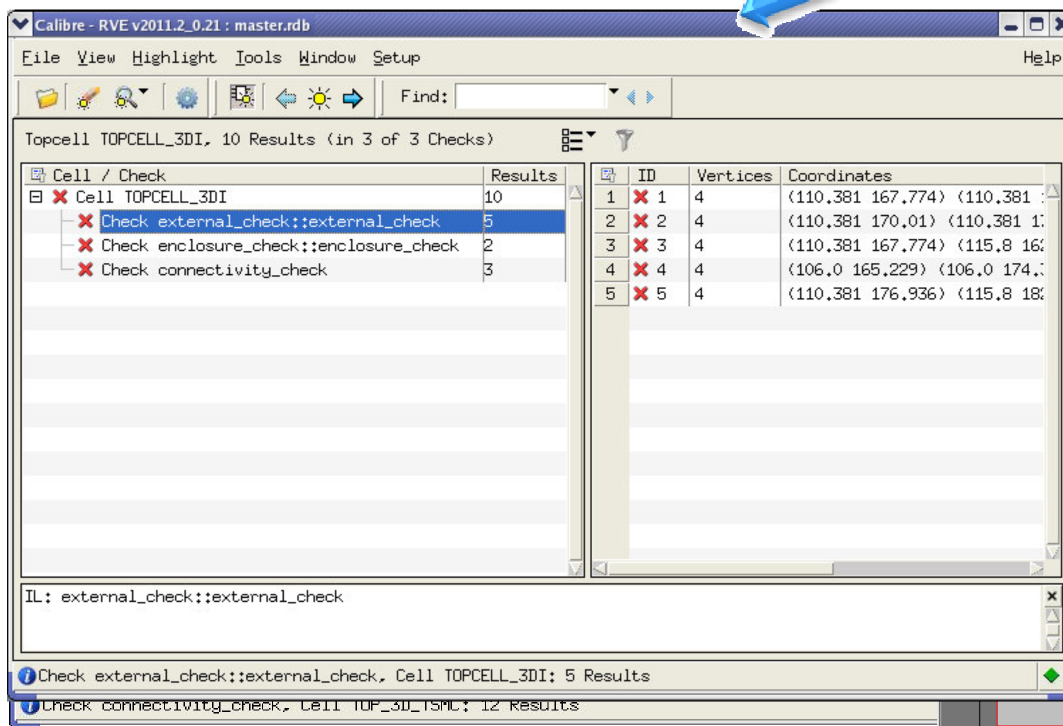
3D IC Verification Flow: Alignment violation

- DRC: verify micro-bumps physically align
- LVS: verify proper electrical connectivity





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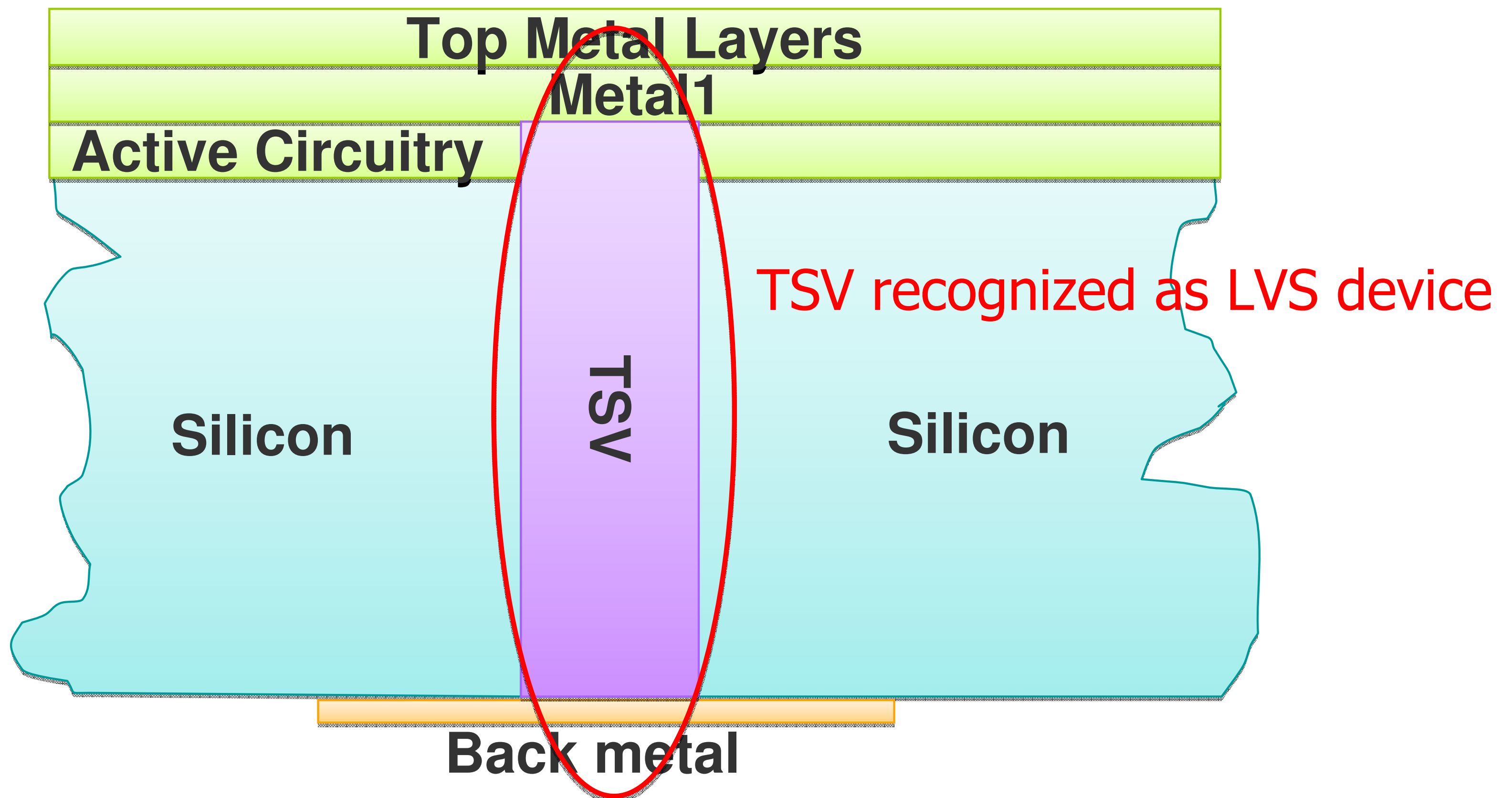
Calibre LVS

- Calibre LVS was used to check the connectivity of the logic and memory dies individually, with the TSVs recognized as intentional devices.



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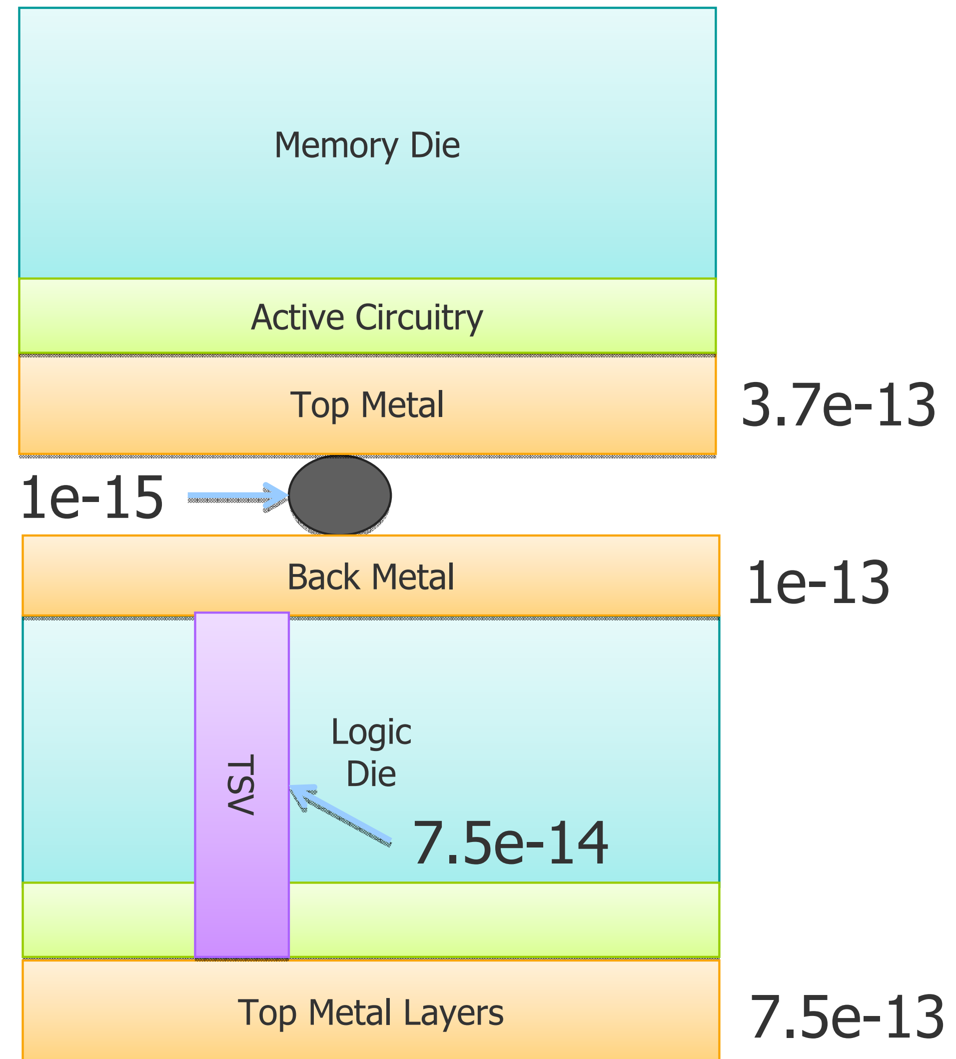
Calibre xACT 3D field solver for parasitics

- A new extraction rule file was generated with xCalibrate to include the back metal stack.
- Break down each net that is on both dies into constituent pieces to see the ratio of TSV and micro-bump capacitance versus on-chip capacitance.
- The TSV was treated as an LVS device, and a subcircuit provided by the foundry was used to model the TSV.
- The TSV-to-substrate capacitance is 75 fF.
- The micro-bump capacitance is estimated to be around 1 fF, based on a paper by Alam et al. [12].



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Capacitance Results

Capacitance (F)	Logic Top Metal	TSV	Logic Back Metal	Micro-bump	Memory Top Metal
NetA	7.52E-13	7.50E-14	1.09E-13	1.00E-15	3.70E-13
NetB	7.60E-13	7.50E-14	1.09E-13	1.00E-15	2.68E-13
NetC	7.20E-13	7.50E-14	1.09E-13	1.00E-15	8.78E-14
NetD	8.09E-13	7.50E-14	1.09E-13	1.00E-15	9.37E-14
NetE	6.91E-13	7.50E-14	1.09E-13	1.00E-15	2.66E-13
NetF	1.47E-13	7.50E-14	1.09E-13	1.00E-15	1.57E-13
NetG	1.36E-13	7.50E-14	1.09E-13	1.00E-15	1.55E-13
NetH	7.42E-13	7.50E-14	1.09E-13	1.00E-15	1.27E-13
NetI	7.60E-13	7.50E-14	1.09E-13	1.00E-15	1.87E-13
NetJ	7.23E-13	7.50E-14	1.09E-13	1.00E-15	8.71E-14

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Verification Challenges

- TSV Modeling
  - High frequency effects
  - Nonlinear effects in TSV
- Interaction modeling
  - TSV densities and need for interaction modeling
  - Coupling between the TSVs
  - Coupling between the TSVs and interconnect
  - Coupling between TSV and devices
  - Coupling between front and back side metal?
  - Die interface modeling
  - Coupling between the stacked dies?
- Multi-die Analysis
- Thermal signoff
- Stress impact on performance yield
- Flow integration

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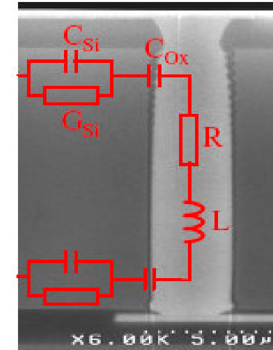
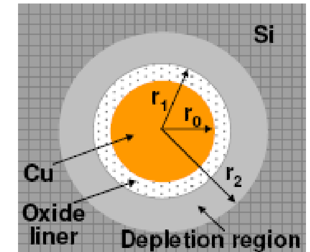
TSV Modeling

- Circuit for TSV provided
  - Obtained by S-parameter measurements and circuit parameter extraction

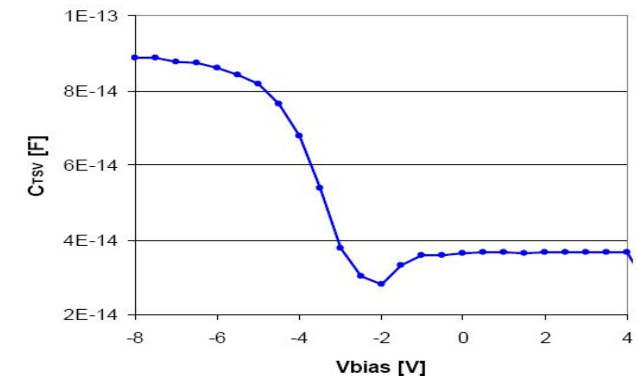


Source: LETI



Source: RPI

- TSD or TSV
  - " nonlinear behavior shouldn't be too much of a problem since it is confined mostly to the < -1V region and we really shouldn't be operating there."



- Present solutions/approaches do not and can not take into account TSV interactions

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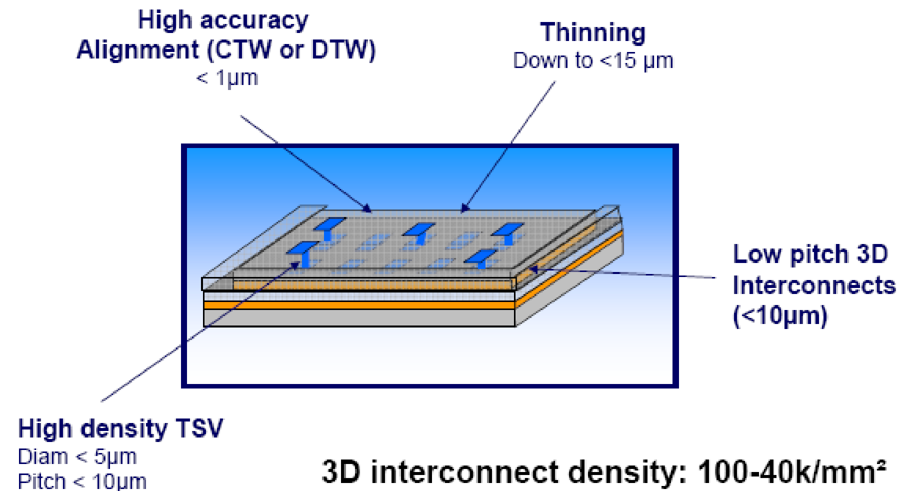
High Density TSVs

- "Via Middle" technology
  - TSV before BEOL



- Some of the communication signals are likely to be high frequency
- Each TSV will work in the skin effect regime, and all the effects are fully 3D.
- Accurate analysis might require 3D Electromagnetic approach.

  - At the end, we want these components to be extracted like other interconnections and contribute in the parasitic network : we want to take into account every RLCK interactions between TSVs, BUMPs, substrate, doping regions, RDL, ...

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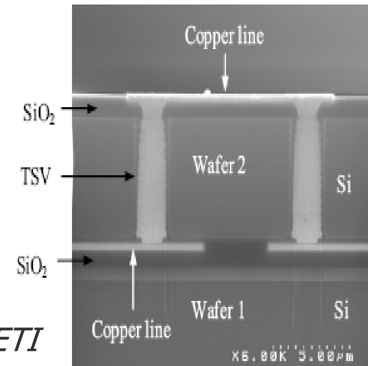
TSV Interaction Modeling

- Interactions between the TSVs
  - Capacitive and Inductive couplings
  - Interaction among TSVs will be predominately magnetic



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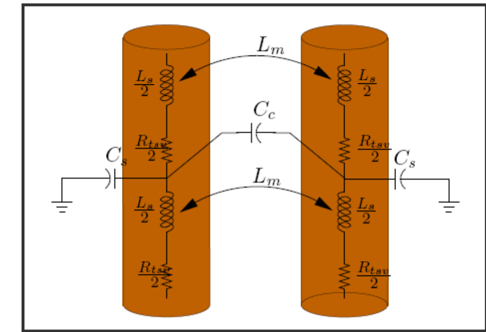
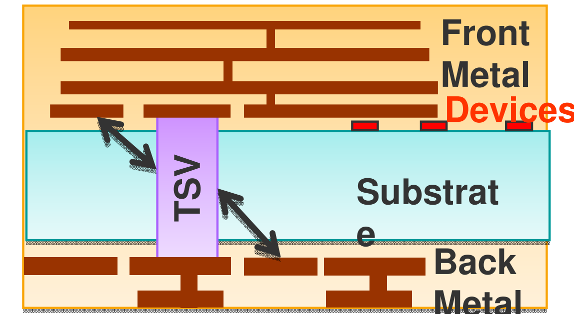
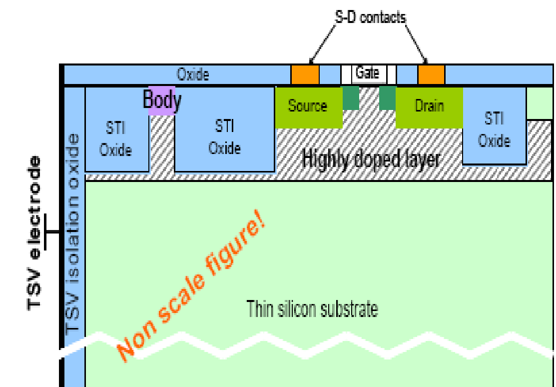


Source: RPI

- Interaction between TSV and interconnect
  - Interactions with RDL and metal1



- Impact of TSVs on device performance
  - Proper substrate description and modeling is needed



Source: LETI

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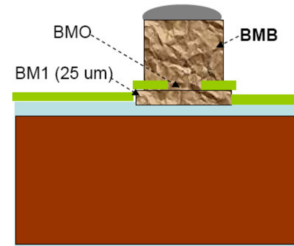
Dies Interface modeling

- Bump modeling



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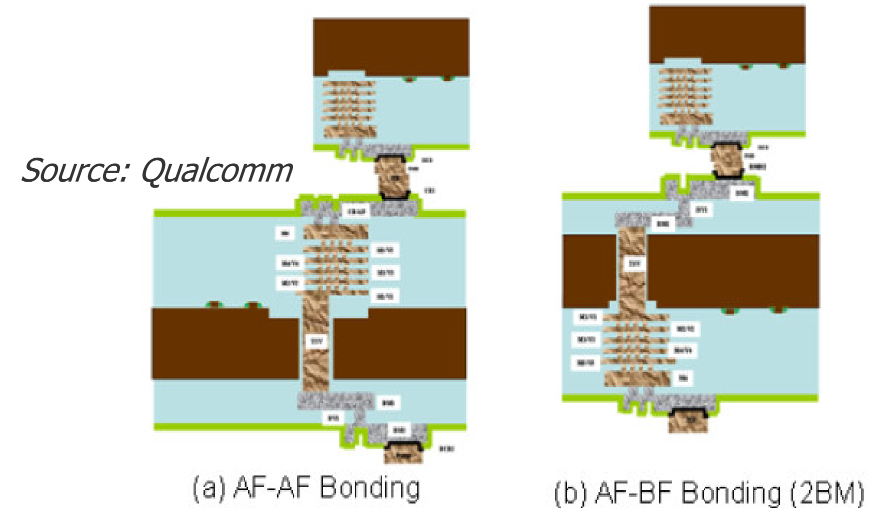
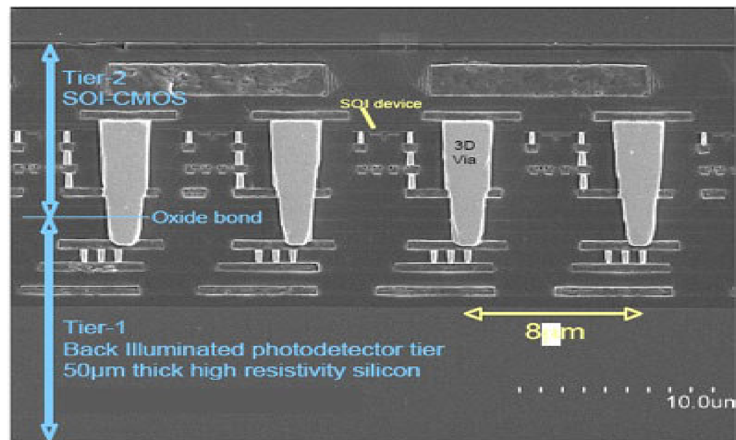


- Bump interactions and shielding
- Other bonding techniques



Oxide Bonding – MIT Lincoln Lab

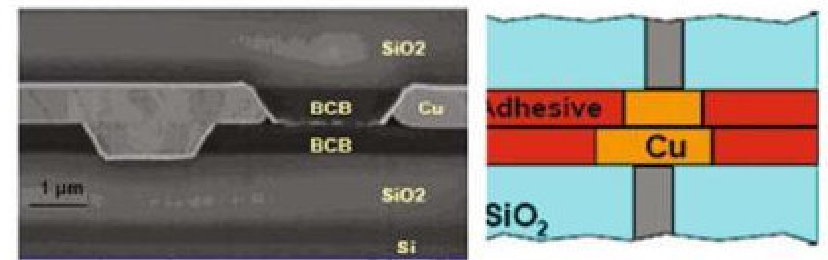


Fig. 1.35 A die-Stack using a combination of Cu-Cu and BCB adhesive bonding at RPI [14]

Cu-Cu Bonding

Source: RPI

Different bonding scheme have different impact on parasitics

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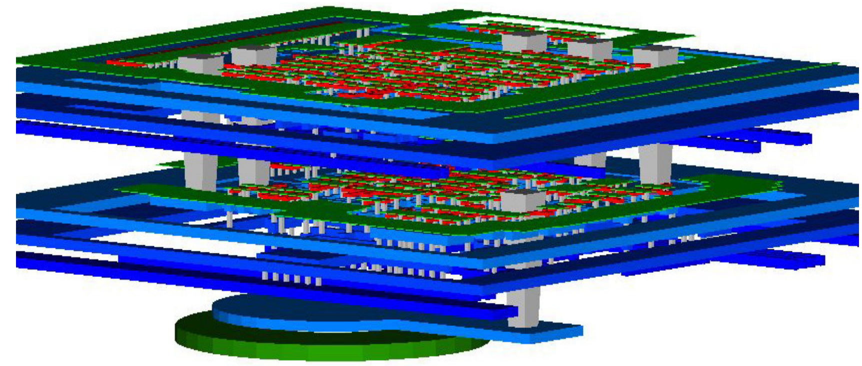
Inter-die interactions

- Capacitive coupling might not be negligible between the dies, especially in Face-to-Face connection
- Magnetic coupling between the dies
  - The dies are getting closer together
  - Overlapping loops between the dies



Source: Fermilab

- Full stack IR drop is needed
  - As number of TSVs is increasing the interactions are becoming stronger and IR drop analysis has to be done simultaneously for the entire stack
- The paths go across the dies and LVS, extraction and simulation have to go across the dies.

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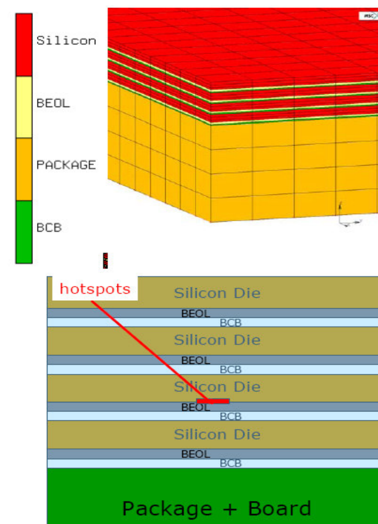
Thermal signoff

- Thermal effects more pronounced in 3D then 2.5D
- Electro thermal interactions have to be taken into account
- Variability in device parameters
- Thermal analysis and signoff needed



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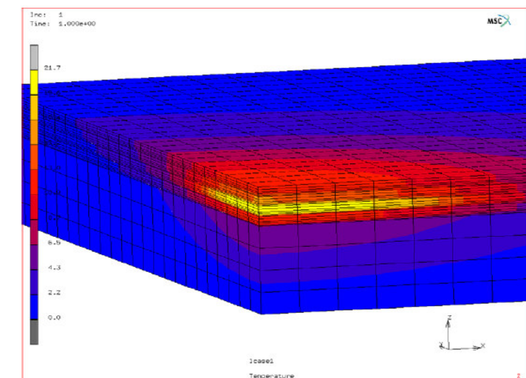

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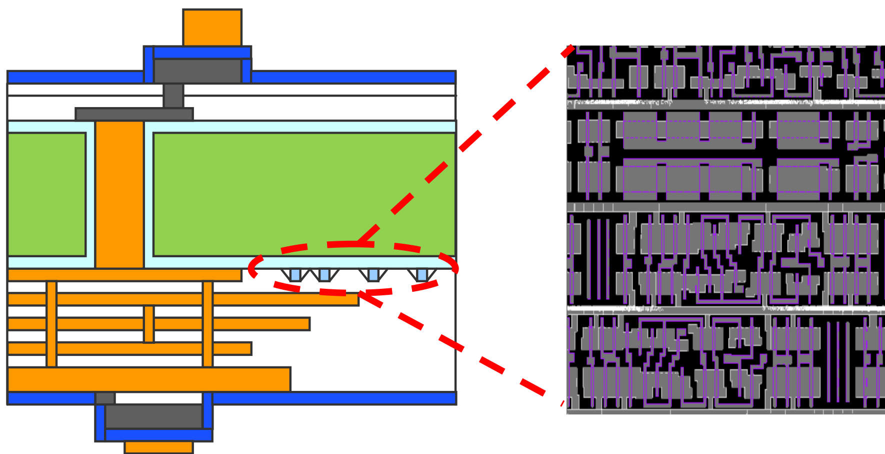
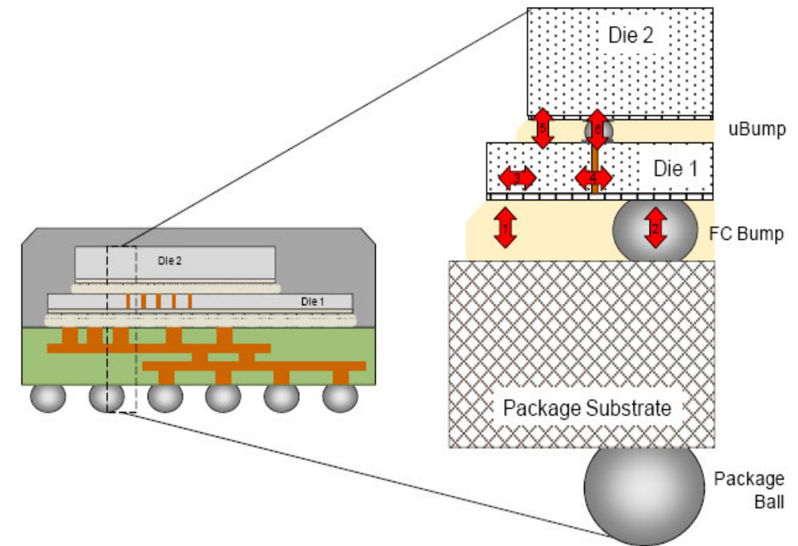
Strain-induced variations: 3D stack effects



Source: V.Sukharev



- In TSV-based 3D-IC technology an additional inside transistor stress variation caused by a global load generated by the TSVs, die thinning and assembling should be taken into account
- Long-range character of the stress propagation makes a prospective gate-to-gate stress variation more pronounced.

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Conclusions

- Existing 3D-IC verification approaches satisfy present 3D system needs
  - — DRC/LVS/PEX of the individual dies and interposer
  - — TSV modeled as LVS devise or Via; Foundry TSV model provided
  - — DRC and connectivity validation of 3D stack interfaces
- Challenges come with increased densities and operating frequencies
  - — Need for accurate TSV extraction
  - — TSV interaction modeling
- Thermal and stress aware verification
  - — More difficult in 3D then in 2.5 D stacking
- True 3D LVS/PEX
  - — Will be needed in 3D-ICs with logic divided across the dies

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