INVENTIVE

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3D-IC/TSV Design

EDA Software Requirements

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EDPS 2011

An Inconvenient Truth
"Cost is the New Driver"

Yield and Manufacturability

2005	2006	2007-2008	2009-2010
90 nm	65 nm	45 nm	32 nm

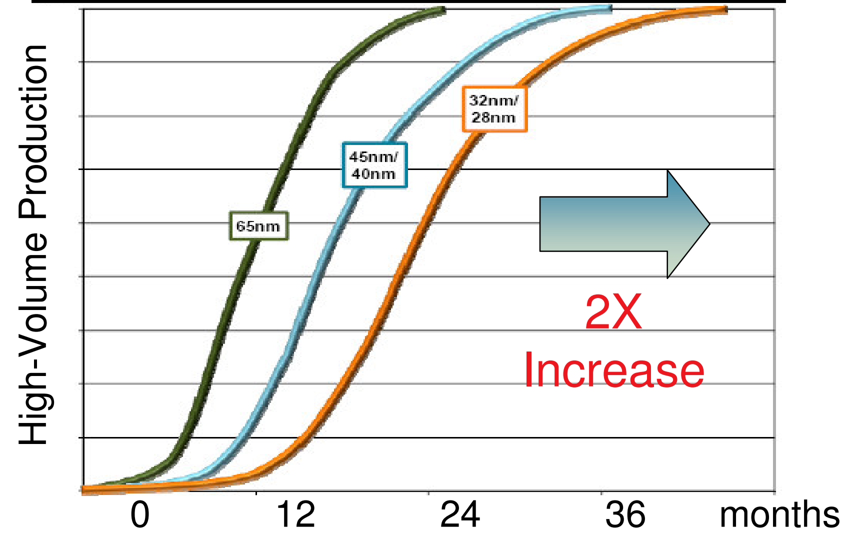
	90nm	65nm	45nm	32nm
Performance & SI	●	●	●	●
Area	●	●	●	●
Power	●	●	●	●
DFY (Particle Defects)	○	●	●	●
Variation (Device and Interconnect)	○	●	●	●
CMP and Litho		○	○	●
Stress and Etch			○	●
Temperature			○	●
New Devices				○

Design, manufacturing and R&D costs

	45-nm node	32-nm node
Fab costs	$3B	$5B-10B
Process R&D	$2.4B	$3B
Design costs	$20M-50M	$75M
Mask costs	$9M	NA

Source : IBS

Predictability/Convergence



6 month delay
causes $5B
in profits!

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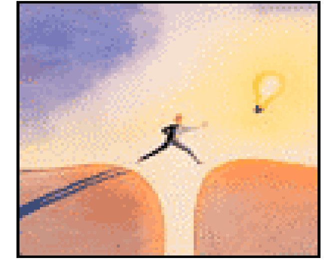
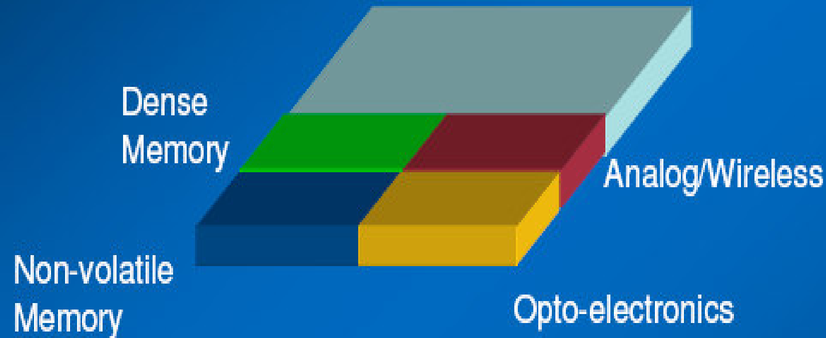
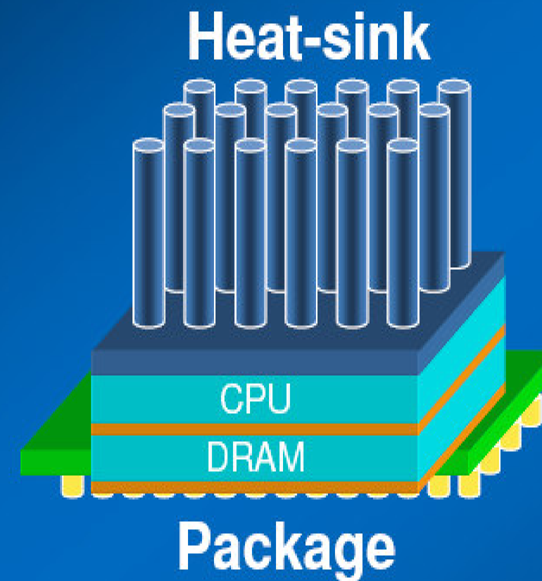
Why 3D Stacked Dies/TSV?



Integration of Heterogeneous Technologies





Power and IO signals go through DRAM to CPU

Thin DRAM die

Through DRAM vias

Source: Intel

3D technology will help:

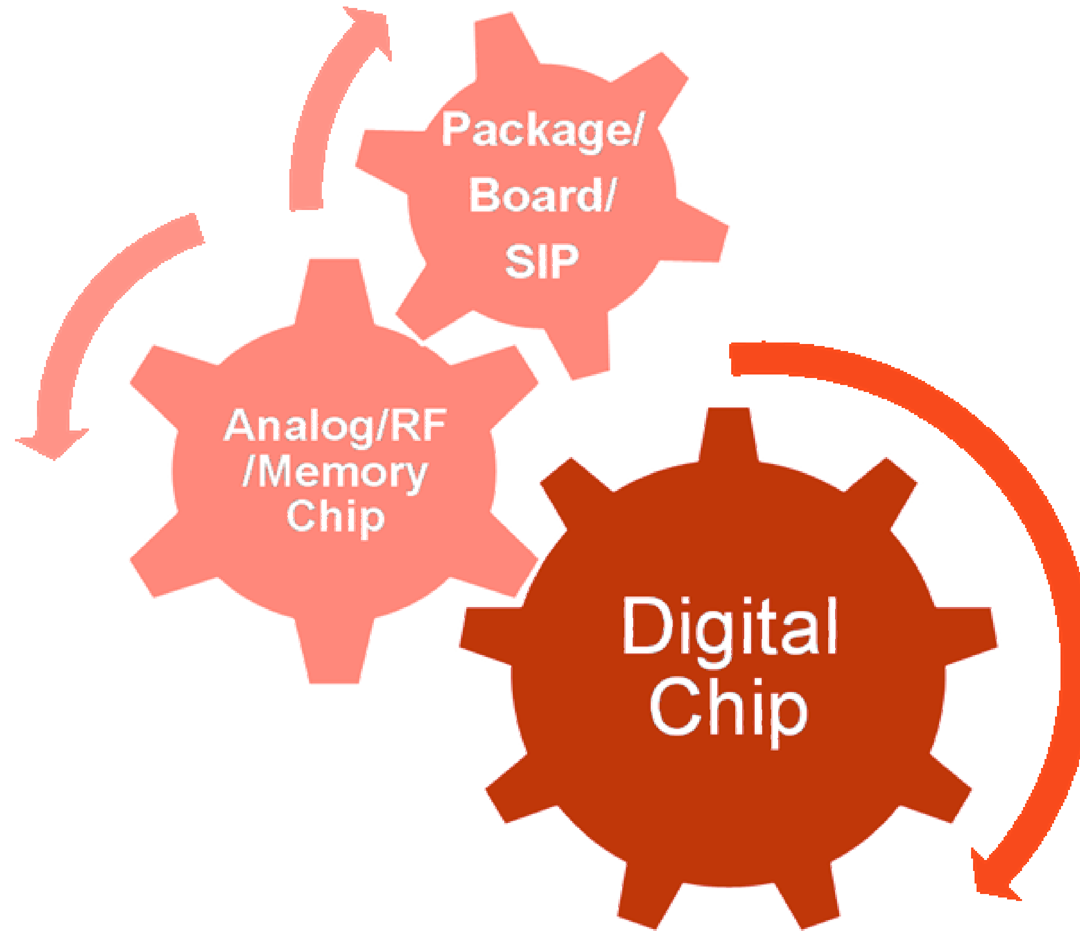
1. Integration of heterogeneous technologies
2. Lower interconnect power
3. Lower system cost

Do not want to end up like this!

3DIC : It is a Heterogeneous Stack

Co-Design of Digital, Analog and Package is Key

Enabling Heterogeneous System



Closer IC Integration through OA

Co Design is Most essential

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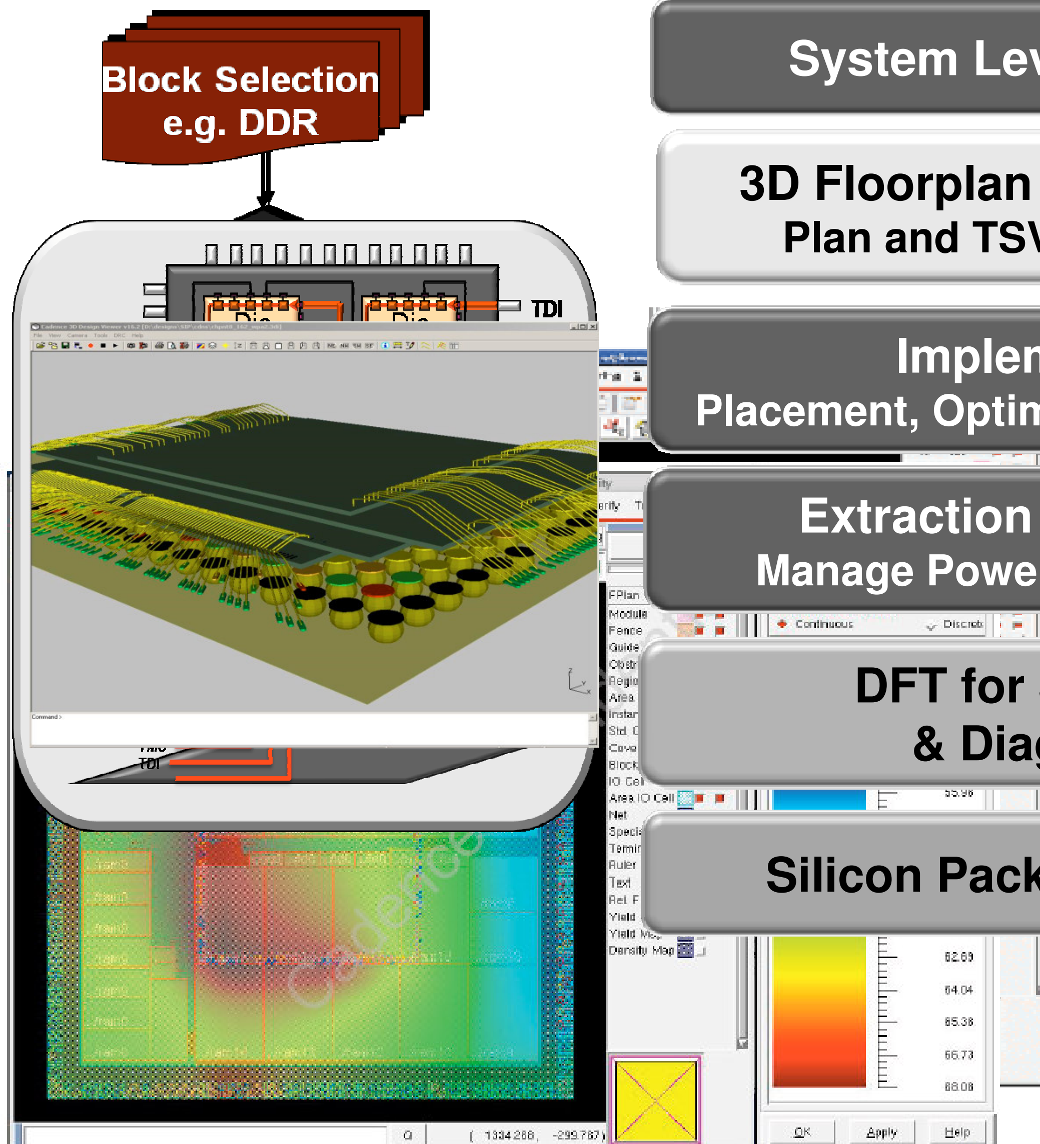
3DIC Design Flow Challenges

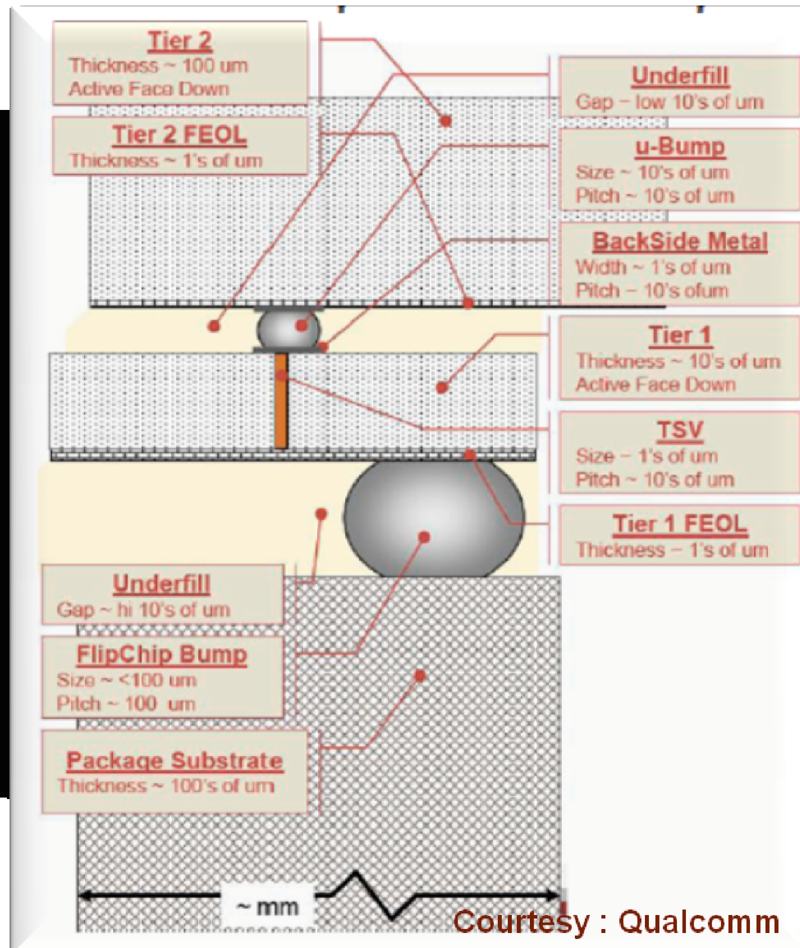
New 3DIC Design Flow Challenges



- System Level Exploration
- 3D Floorplan – Optimized power Plan and TSV/Bump locations
- Implementation
  Placement, Optimization and Routing
- Extraction and Analysis
  Manage Power, Thermal and SI
- DFT for 3DIC Stack & Diagnostics
- Silicon Package Co-Design

So what changes in the EDA world?

Revamped EDA requirements



- **New Layout Rules** (e.g. alignments)
- **New Layout Layer** (e.g. Back Side RDL)
- **New Layout & Electrical Feature** (e.g. TSV)
- **New Floorplanning & Blockage Rules (TSV)**
- **Thermal & mechanical constraints**
- **New Models, Rules**

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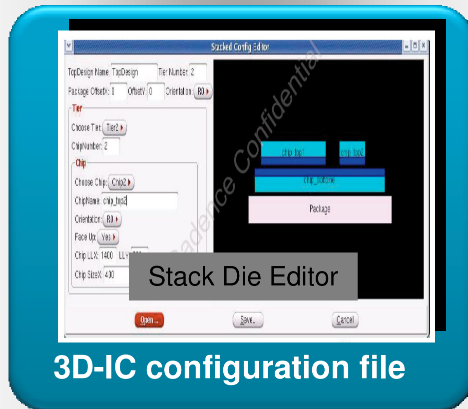
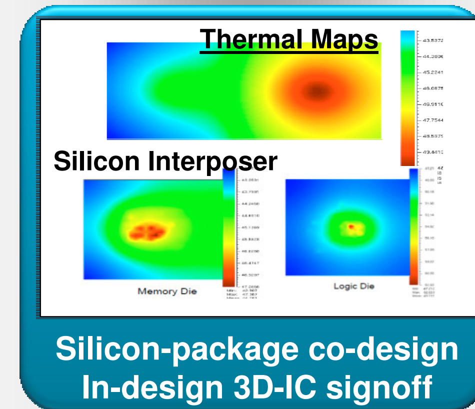
Cadence 3DIC Silicon Realization

INTENT



ABSTRACTION

CONVERGENCE



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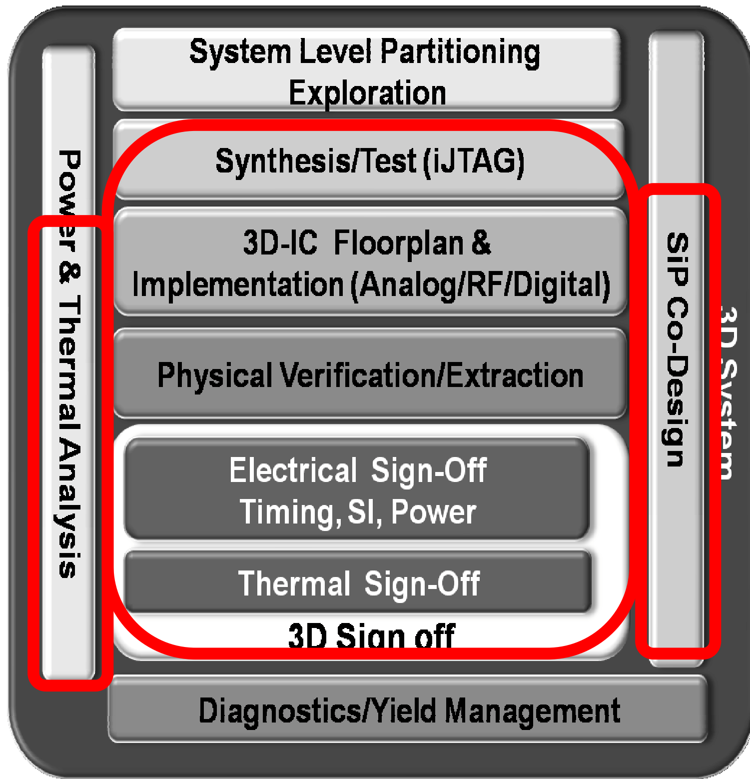
3D-IC EDA Design Tools

Plan->Implement->Test->Verify



Cadence 3D IC Flow

3D Stack Die Editor

3D Floorplan – Optimized power Plan and TSV/Bump locations

TSV /Bump RDL Routing

Virtuoso for custom shape editing

Interposer

3D IR Drop Analysis

•Die1

•Die2

3D Thermal Maps

Silicon Interposer

Memory Die

Logic Die

IC-Package Co design flow
Back-side Bump Management

3D view of system in package tool

Back-side bump reading in CDNSIP

3D-IC: Qualcomm + Cadence

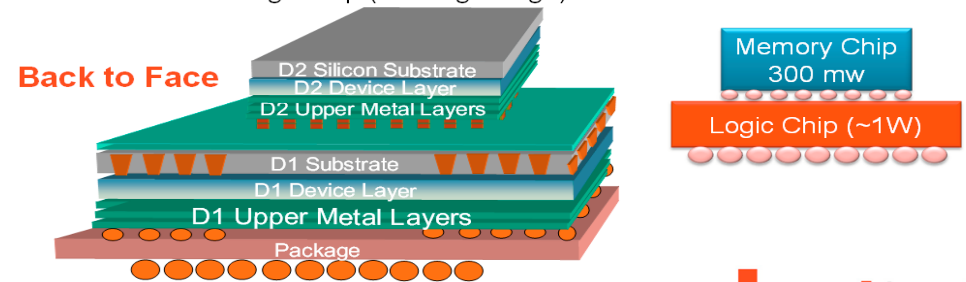
Source: RTI 3D conference 2009 proceedings

Thermal Design Objectives in 3D IC

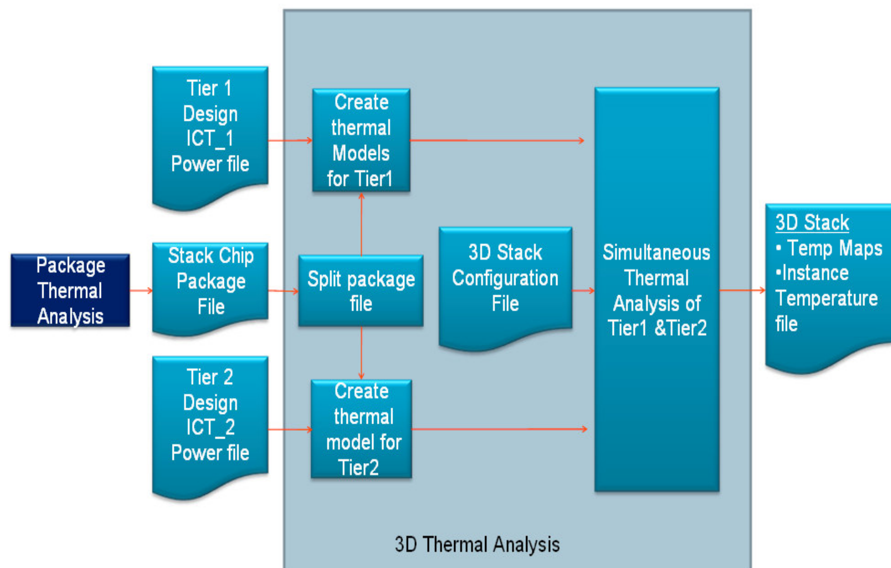
- Communication chip design uses low power techniques (~ 1 Watt). Will stacking low power chip together produce thermal hot spot.
  - We know that microprocessor's power consumption is at least in the 10's of Watts. Stacking with high powered devices have been reported to have thermal challenges in 3D IC.
- If the low power stack does exhibit thermal hot spots:
  - Can regular thermal optimization improve hot spots.
    - Example: Thermal TSV, thermal micro-bumps, better inter-chip material.
    - By how much?
  - Examine other areas to improve on thermal management.

Construction of a Two Chip Stack Design

- EDI (Encounter Digital Implementation) System is used to construct the following stack for thermal management experiments.
  - Memory Chip (Black Box Physical Model)
    - 4 Quadrant of memory banks
    - Four quadrants of micro-bumps.
  - An SOC logic chip (existing design)

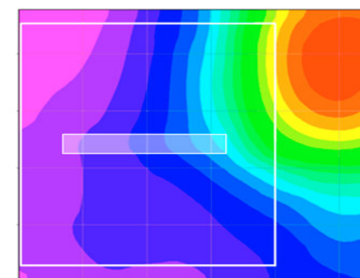


Thermal Analysis Flow For Two Chip TSS

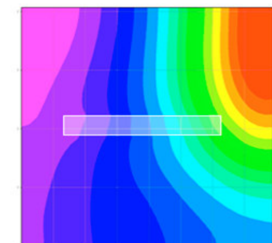


Thermal Gradients

- Significant Thermal Gradients seen across both die
  - 5C to 20C delta across Tier 1 die depending on power scenario
  - Hot spot due to high power block on Tier1 die
  - T1 hot spot vs T2 hot spot temp 3C to 10C depending on power case
    - Thermal coupling between die is very good



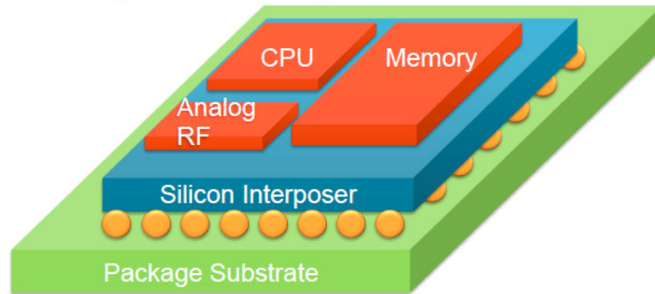
Tier 1 Die



Tier 2 Die

3D-IC: STMicroelectronics + Cadence

Source: RTI 3D conference 2010 proceedings



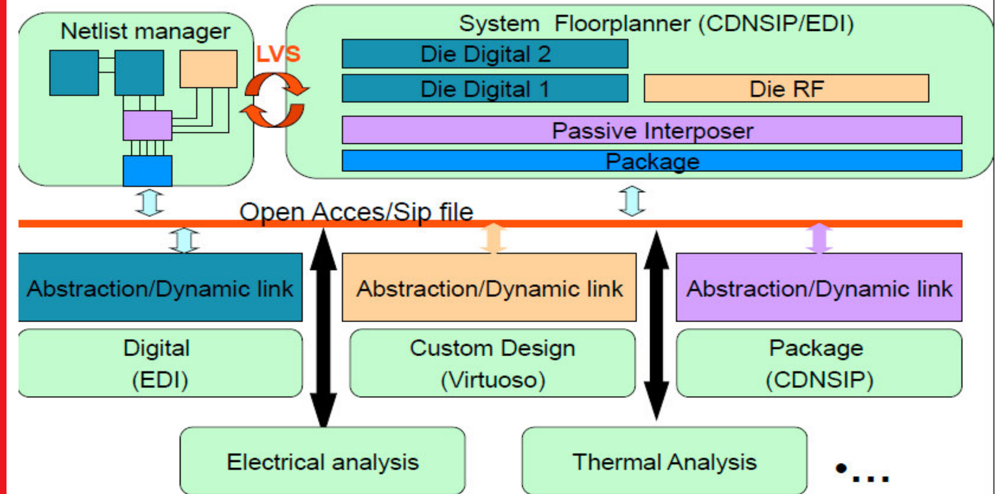
Three chips are placed faced down on top of silicon interposer.

Silicon interposer : 4-9 levels of high density Interconnect.

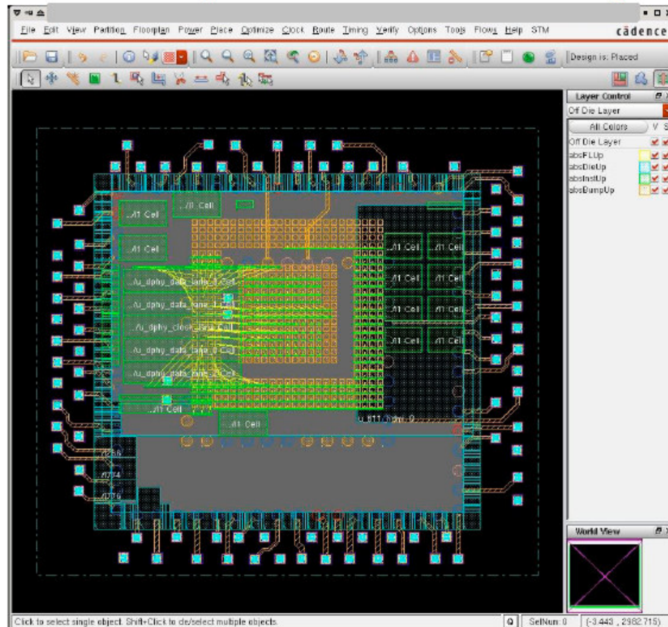
- No active areas.
- Passive devices like metal capacitances.

Challenges: Physical design, electrical analysis, power distribution and analysis and thermal management.

Cadence based ST 3D Solution overview

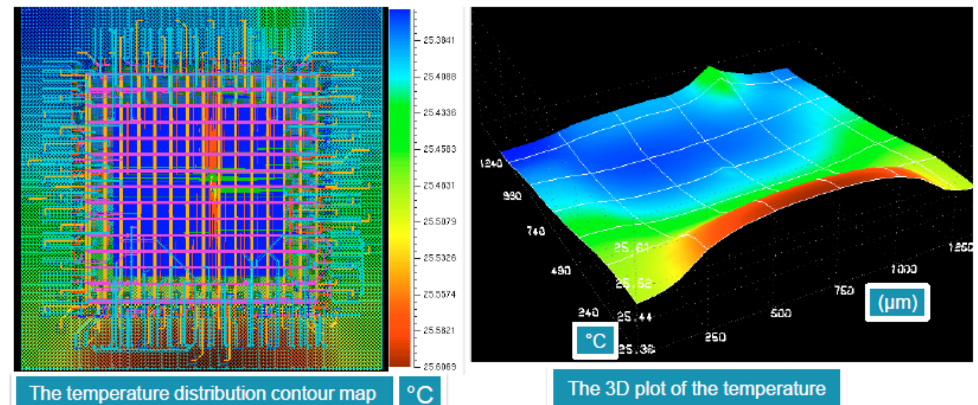


Top view of interposer with TOP die in ghost view



Thermal Analysis Results

- Thermal Analysis Provides a Rich of Thermal Data
  - 2D Thermal contour can be displayed on each chip.
  - 3D Thermal Map.
  - Thermal values per layer and per x,y coordinates.
- The example below has small power consumption ➔ thermal gradient is small

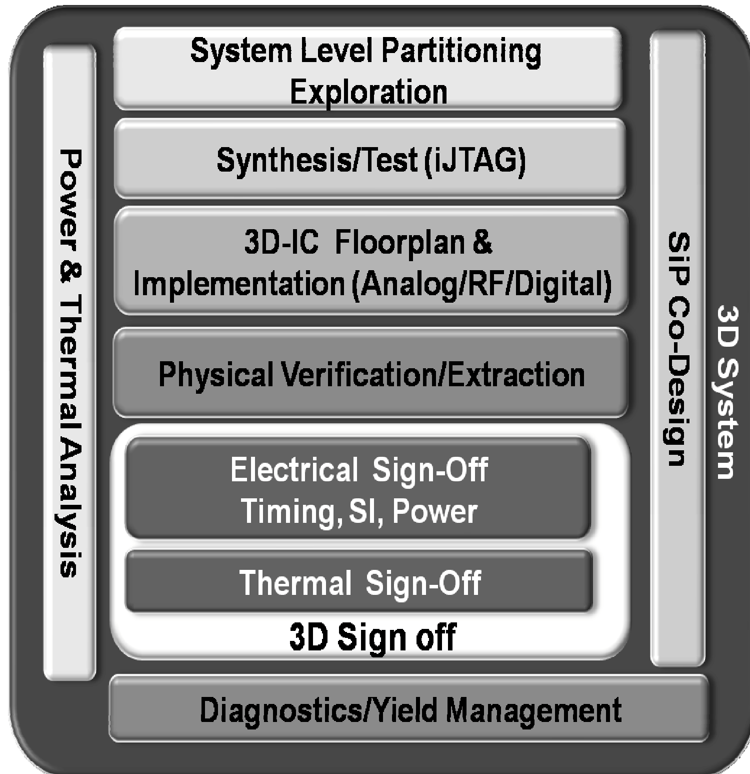


The temperature distribution contour map

The 3D plot of the temperature

Cadence Silicon-Proven 3D-IC Solution

Enabling 3D-IC Silicon Realization



- **Complete, integrated 3D-IC solution**
  - Tools : Plan->Implement->Test->Verify
  - 1st to market 'wide I/O memory controller'
- **Developed in close partner-collaboration**
  - Leading foundries and customers
- **Multiple 3D-IC tapeouts**
  - Memory over logic (28 nm), logic over analog, logic over Logic, 3-stack dies
  - Production design mid-2011 tape-out

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