GSA Global Semiconductor Alliance

Paradigm Shift to 3D and its Impact on our EcoSystem, Standards and EDA Tools

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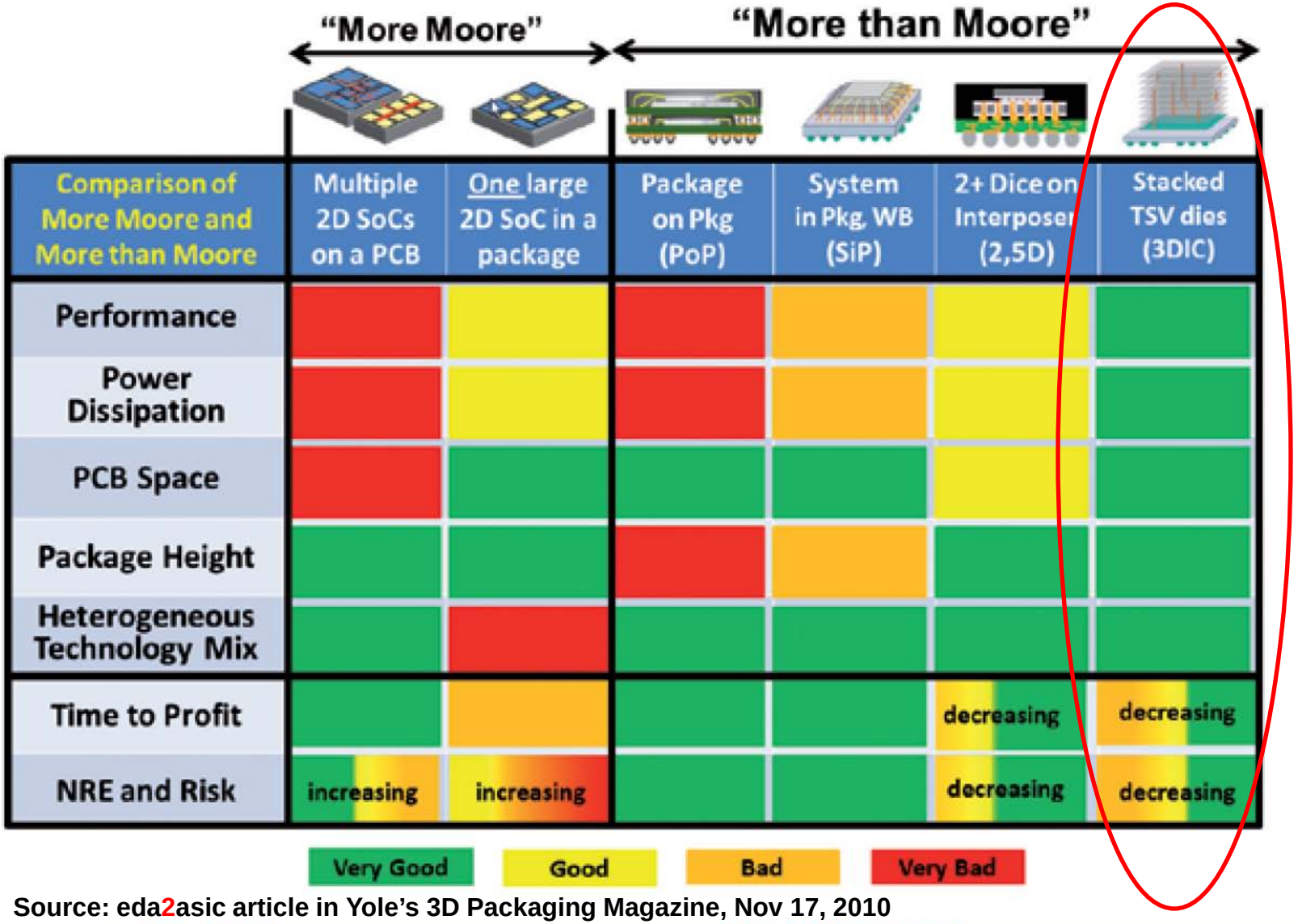
Chair of GSA 3D TSV Programs
EDPS, Monterrey, April 2011

Agenda

- "2D ICs" slow innovation for small & medium volumes
  - Need EcoSystem changes to enable many of us to continue innovating
- 3D demands closer cooperation AND new standards
  - Data exchange formats & tools interoperability foster cooperation
  - Higher packing density demands more rules (condo vs 50 ac ranch)
- 3D technology offers new opportunities for EDA
  - 3D is a SYSTEM integration technology, not limited to IC design
  - Wide range of EDA opportunities from making proven 2D tools "3D aware" and multi-level modeling tasks to solving complex system-level hardware and software challenges with new concepts
- Discussion, conclusions, action items

Major Implementation Alternatives

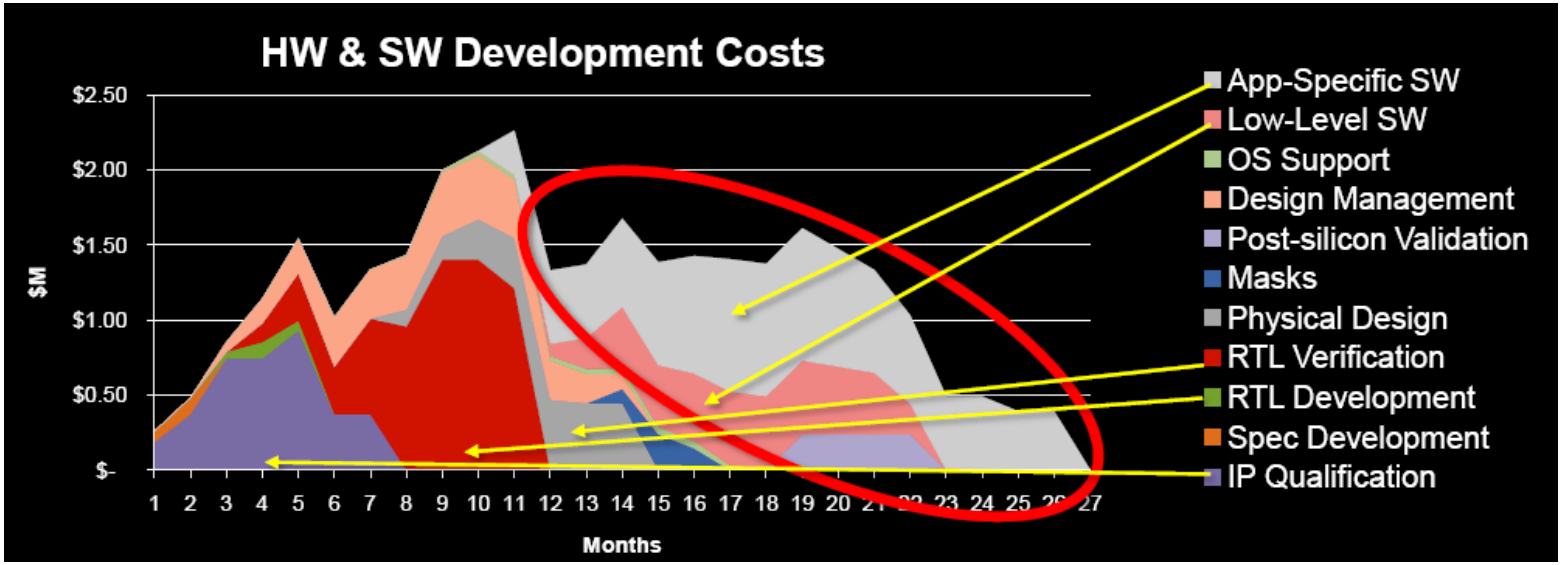


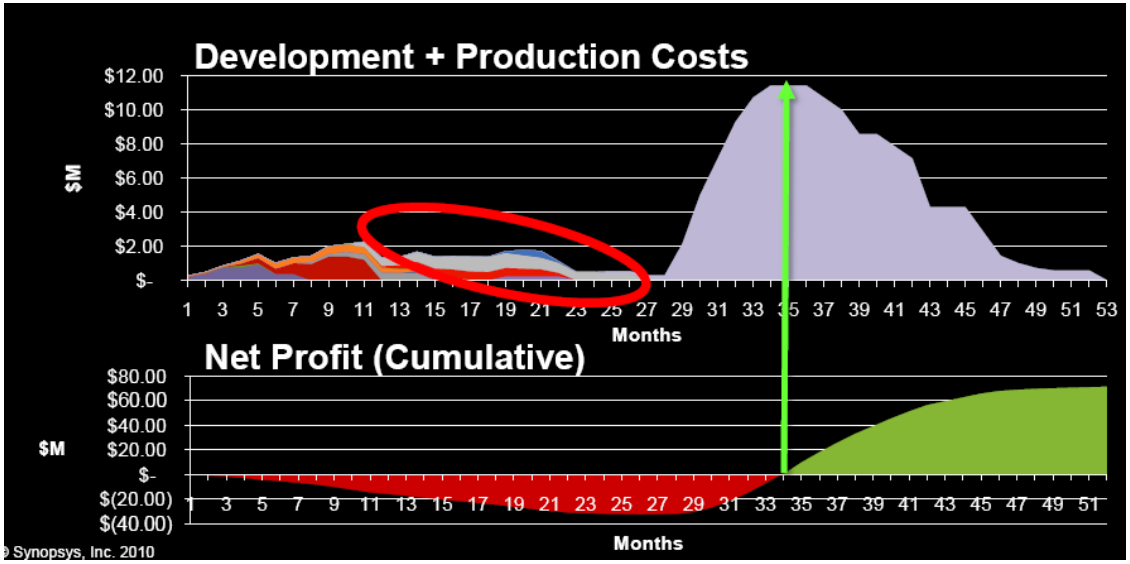
Source: eda2asic article in Yole's 3D Packaging Magazine, Nov 17, 2010

Semiconductor EcoSystem

- **Characteristics of our EcoSystem today**
  - ICs, packages and PCB are designed (almost) in isolation
  - Monolithic “2D ICs” hit economical and technical limits
  - Modular PoP, PiP, SiP,… are in production today
  - 2½D and 3D variations are emerging as new **alternatives** for IC-level and **system-level integration**
- **What do most of our customers want from us**
  - Smarter, faster and lower cost systems with longer battery life
  - Following the latest trends right away
- **How can we meet these requirements**
  - Architect for 3D implementations (wide I/O, analog, MEMS, passives)
  - Higher levels of integration reduce power and increase speed
  - Lots of software improves “smarts” and user friendliness
  - IP reuse and modularity reduce development time and –cost
  - Standards simplify cooperation and drive economies of scale
  - Investment in design- and manufacturing infrastructure

Challenges with the proven 2D SoCs

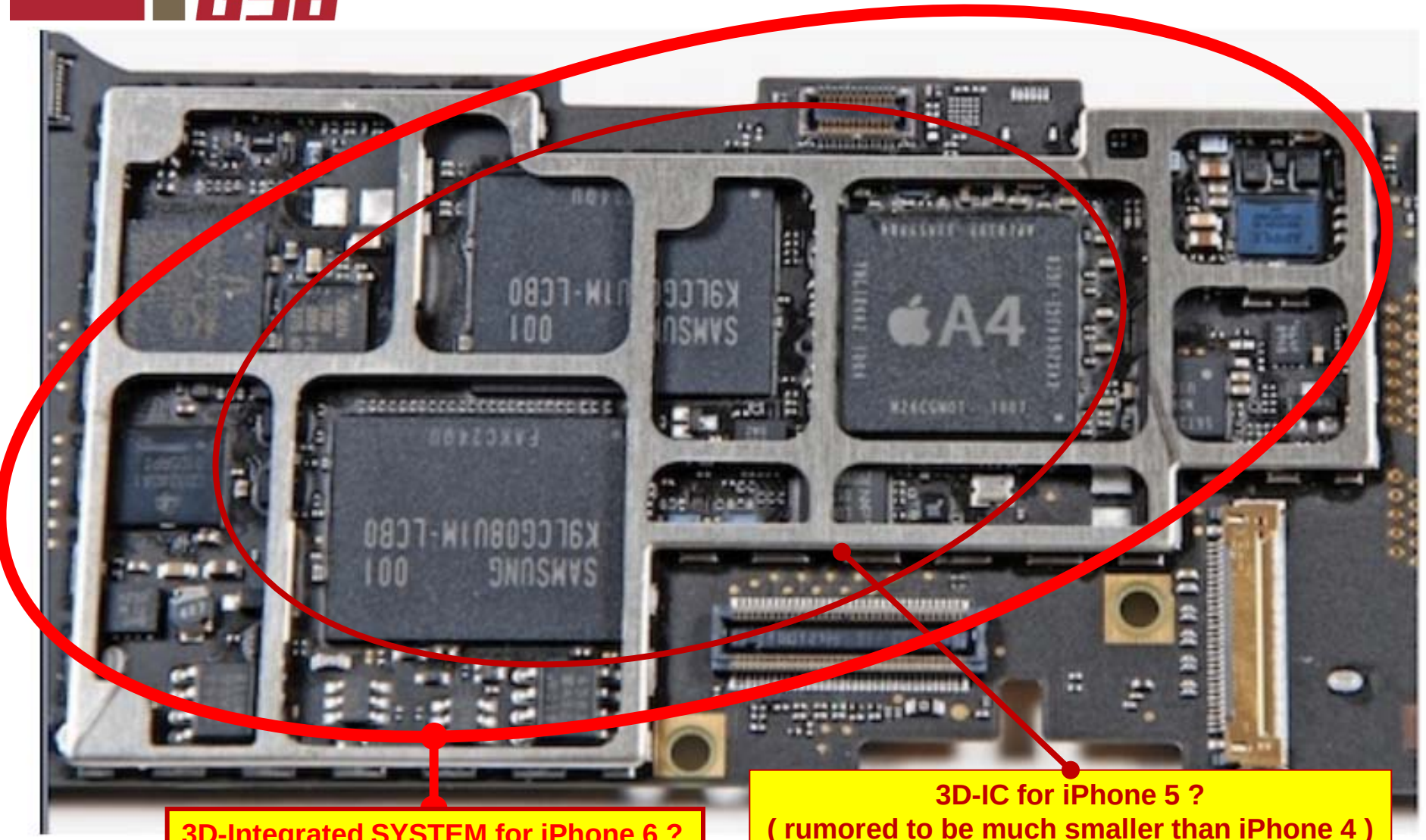




- 2+ years development time
- Software is ~ ½ of the TTM
- NREs of $ 100M and more demand very high volumes to reach breakeven point
- RISKs: Design error
  Market changes
  Competitor moves 1st

Synopsys Keynote, LSI, Oct 6, 2010

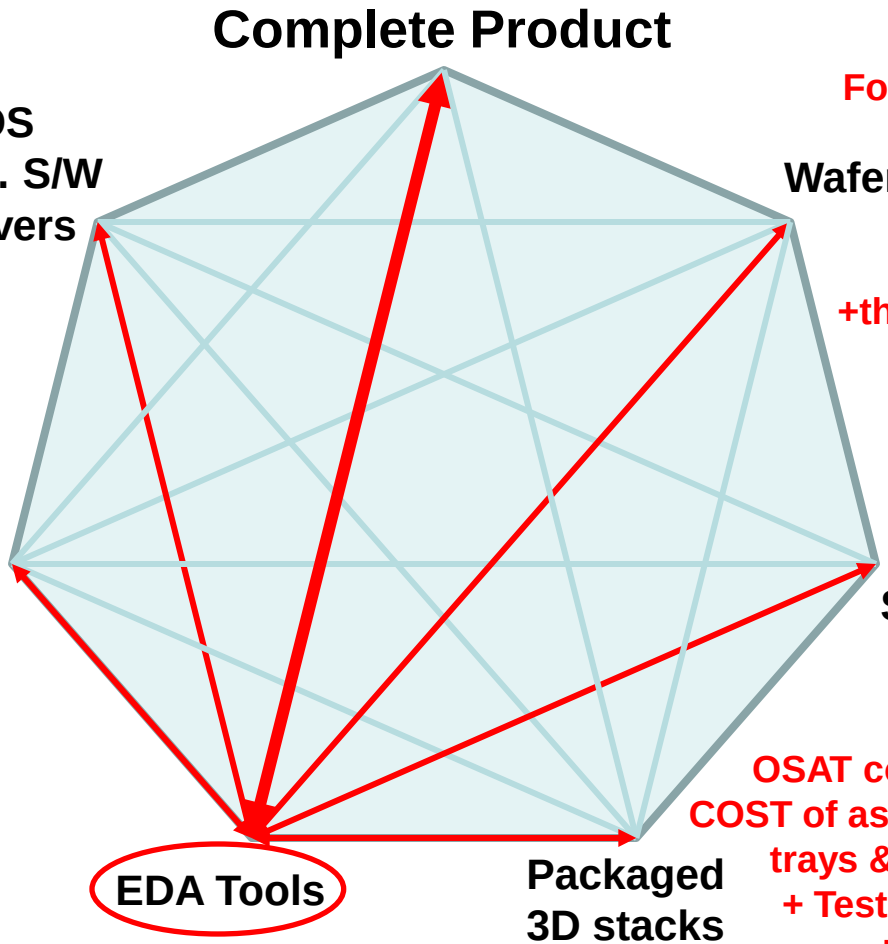
GSM iPhone 4 Circuit Board



http://news.cnet.com/8301-31021_3-20028619-260.html?part=rss&subj=news&tag=2547-1_3-0-20

Cooperation Within the "Food-Chain"

Fabless/light vendor: Idea, architecture, targets for COST, Power, Performance, FormFactor, …



Software Partner:
H/W & S/W
co-design needs
+memory footprint
+performance
+power diss.
+…

Foundry contributes:
"2D" PDK
+die COST
+TSV models
+TCE data
+thermal conductivity
+ …

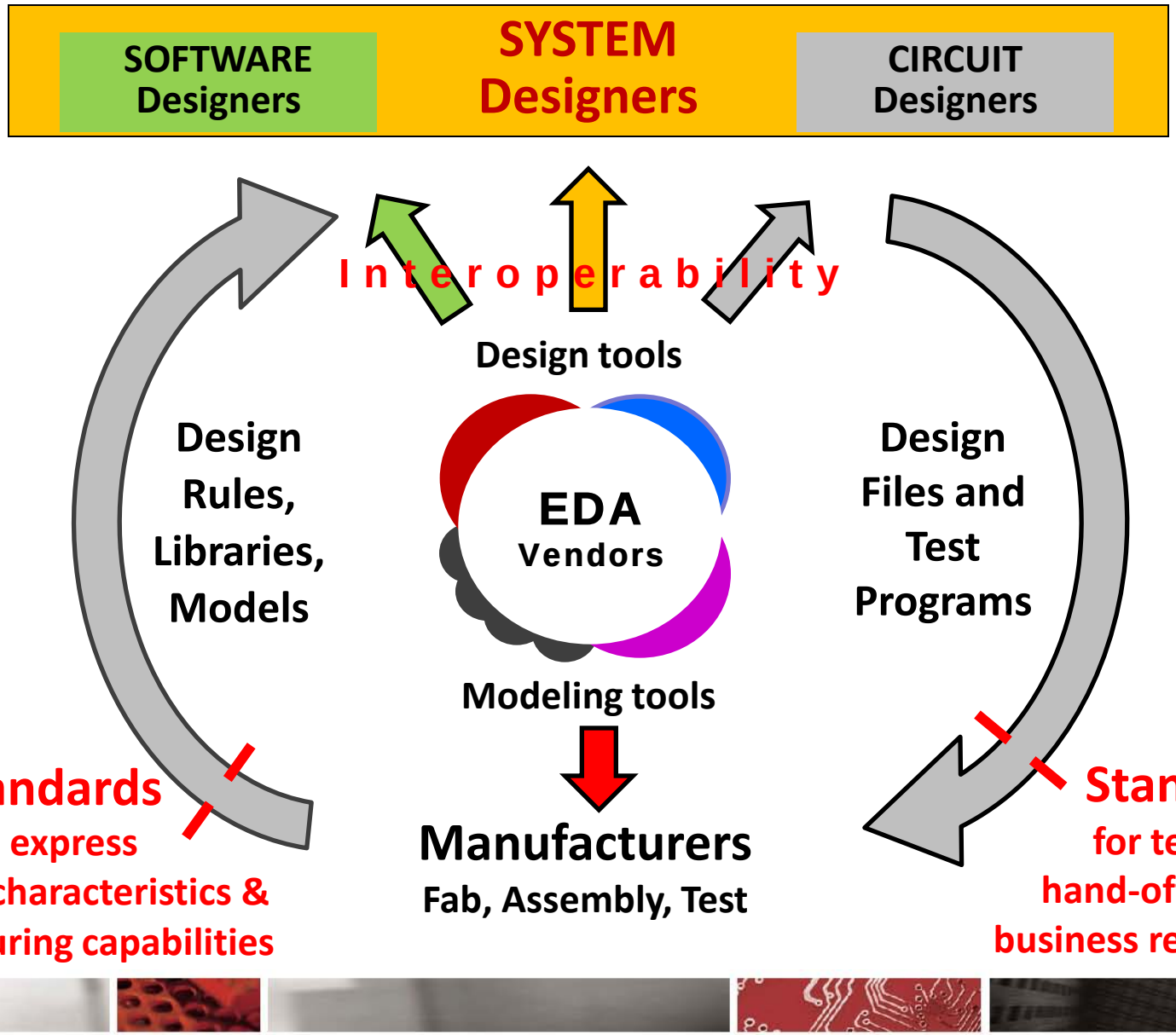
Materials vendor:
COST
+Pkg dimension
+TCE data
+thermal
conductivities
+ …

IP Partner contributes:
"2D" license & royalties
+ models of IP blocks
+3D license & KGD cost
+die-level models
+ …

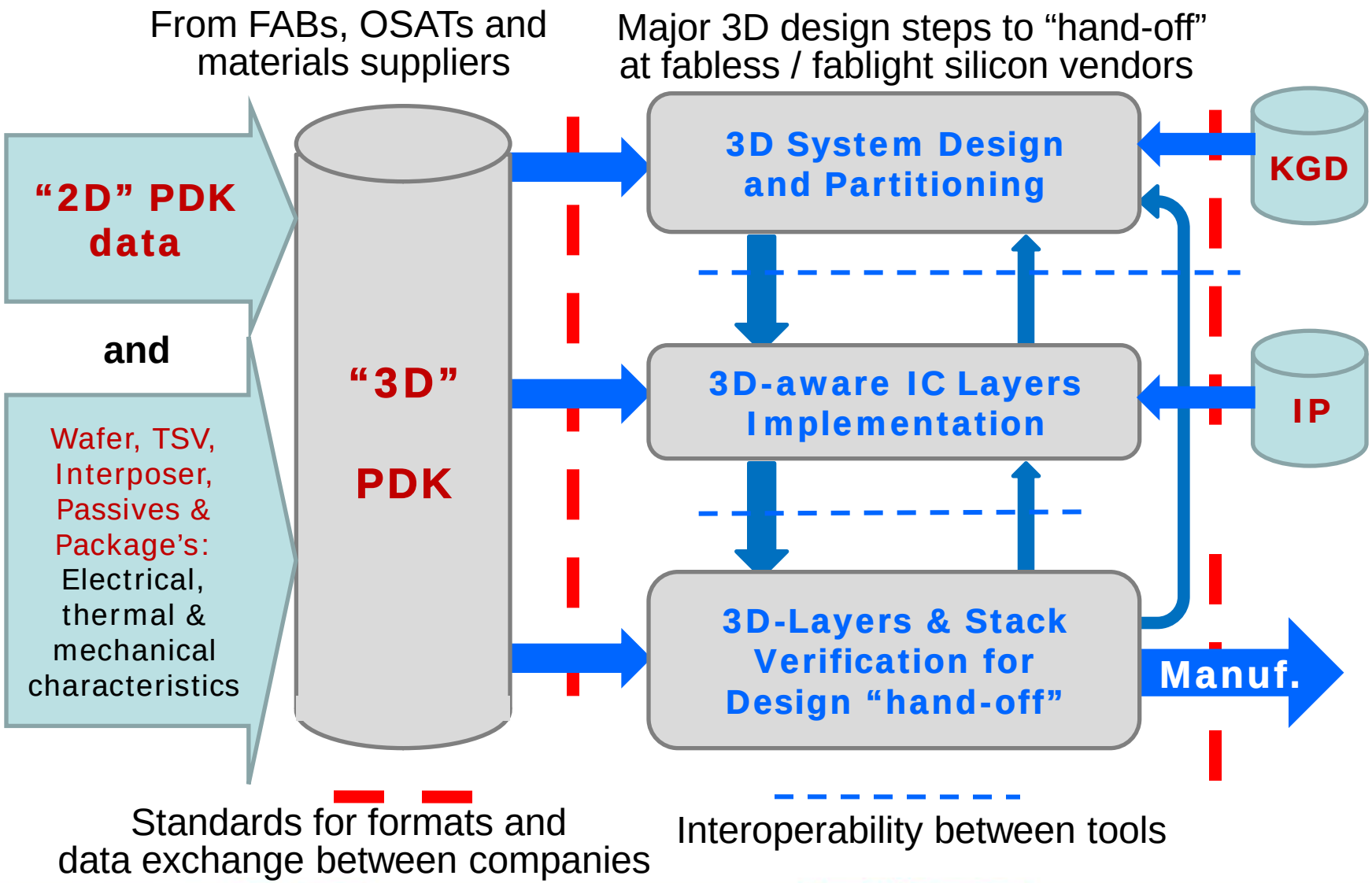
OSAT contributes:
COST of assembly & test,
trays & shipping
+ Test program
+ …

EDA can play an essential role in building the 3D EcoSystem!

The Case for Standards in 3D Design



3D / TSV Modeling & Design Steps



New EDA Opportunities in 3D EcoSystem

H/W Dev. Tools for:

MODELING

- System Planning & Partitioning Including die-level IP Reuse
- Logical & Physical 3D-aware Implementation of new design portion(s)
- Verification of new design portion(s) and entire system. Test program development
- Hand-off to manufacturing

CO-DESIGN

S/W Dev. Tools:

- Operating System
- Applications Software
- Drivers
- Field Updates

EDA Opportunities in 3D Design

- **Modeling tools/flows** to create "3D PDKs" incl. 2D PDK data
  - Capture electrical-, thermal-, magnetic-, mechanical characteristics,…
- **Modify** proven **2D tools** to make them "**3D aware**"
  - PI, SI, noise, temp analysis, TSV strain, P & R ?,…
- Create **tools for 3D specific new challenges**
  - 3D DFT, die+stack+I/P+passives+pkg co-design, warpage, magnetics,…
- Create **system-level H/W planning and partitioning** tools
  - Pathfinding for lowest cost, lowest power, smallest formfactor,…
- Create **system-level hardware and software co-design** tools
  - System partitioning in H/W and S/W, emulation, debugging, updating,…

- Create tools for **OS, applications S/W & drivers dev. & debug**
  - Multi- and many-core, handling of very wide busses, error recovery,…

A closer look at EDA Challenges

- System tools have to be **application specific** and utilize a high-level of abstraction to offer high productivity
- Developing application-specific tools requires **very good cooperation** with the actual users at the EDA customers
- The **number of system designers** is much **smaller** than the number of circuit designers

Valid concerns, but keep in mind:

- As system complexity and value increase, the **need for system-level tools increases** beyond RTL , C++, TLM ➔ large opportunity for EDA !
- Higher abstraction level tools will increase **number of system designers**
- Today's EDA tools sell per seat for the contract period. Their **price is not tied to the value** they create ➔ New business model for system tools?
- System designers who implement large "2D SoCs" will benefits from 3D system tools as well ➔ **increases user base** and revenues !
- Systems' **software content is increasing** and extends systems' useful life significantly ➔ Tools for H/W & S/W co-design and S/W development !

2 ½ + 3D Commercialization Schedules

Company	2½D with Interposers		3D with TSV	
TSMC	2H 2011	[2]	2012-2013	[3]
UMC			2H 2011	[4]
GlobalFoundries			2013	[5]
IBM	2011	[6]		
Samsung			2012	[7]
Elpida			2H 2011	[4]
Micron			2012	[8]
Nanya			2011-2012	[9]
ASE	2012-2013	[10]		
STATSChipPAC			2013	[11]
Amkor	2H 2011	[3]		
SPIL	2011	[12]	2012	[12]
Qualcomm			2013	[12]
Nokia			2012-2013	[12]
Xilinx	2H 2011	[2]		
Dell			2012	[13]

= **this** year

Dr. Phil Garrou, YOLE http://www.i-micronews.com/lectureArticle.asp?id=6351

Discussion Topics

- Is 3D TSV and 2½D technology **here to stay** ?
- Which applications will use 3D/TSVs first ?
- Should **EDA** jump into the **3D drivers** seat ?
- If not now, **when** ?
- Can a different **business model** increase EDA support for 3D ?
- Can we agree on **jointly defined EDA standards or** do we want to waiting for de-facto **(proprietary) standards** ?
- **What else** - if not 3D - **can grow the EDA industry** ?
- **NEXT** technologies: 3D monolithic ICs and Carbon Nanotubes

Thank You !