GARYSMITH EDA

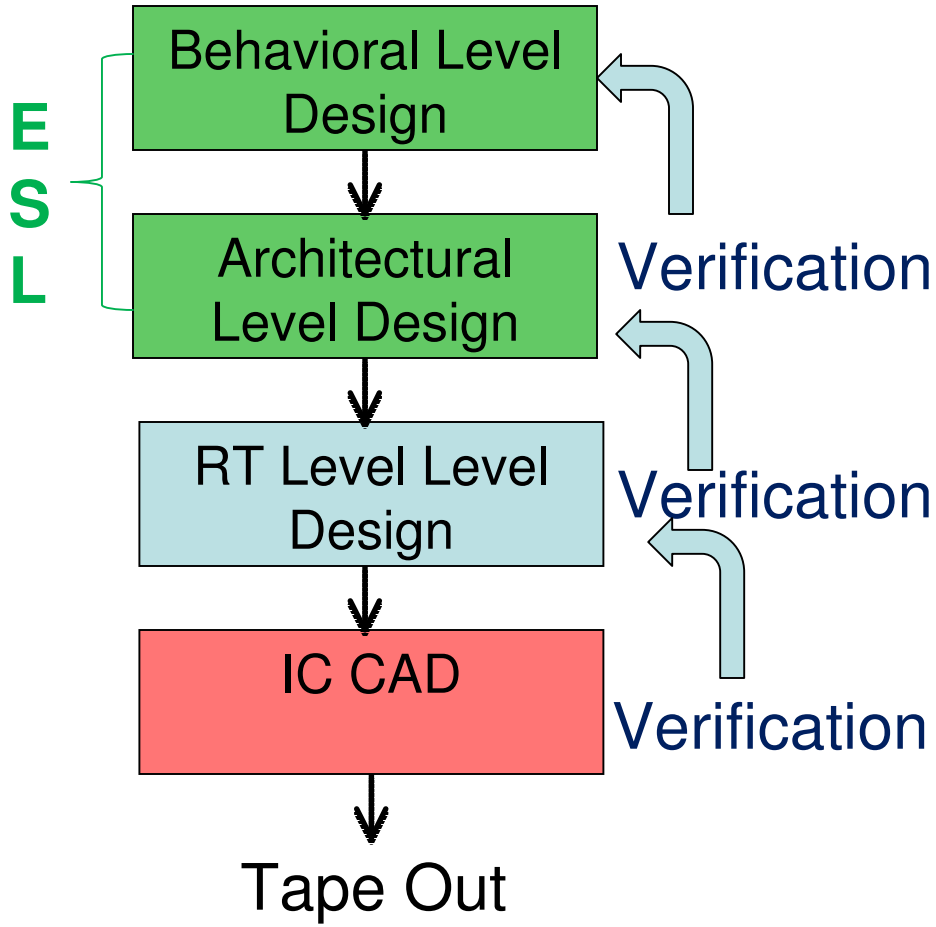
CONSULTING IN ELECTRONIC DESIGN

Reality and Responsibility in the EDA Market *(EDP 2011)*

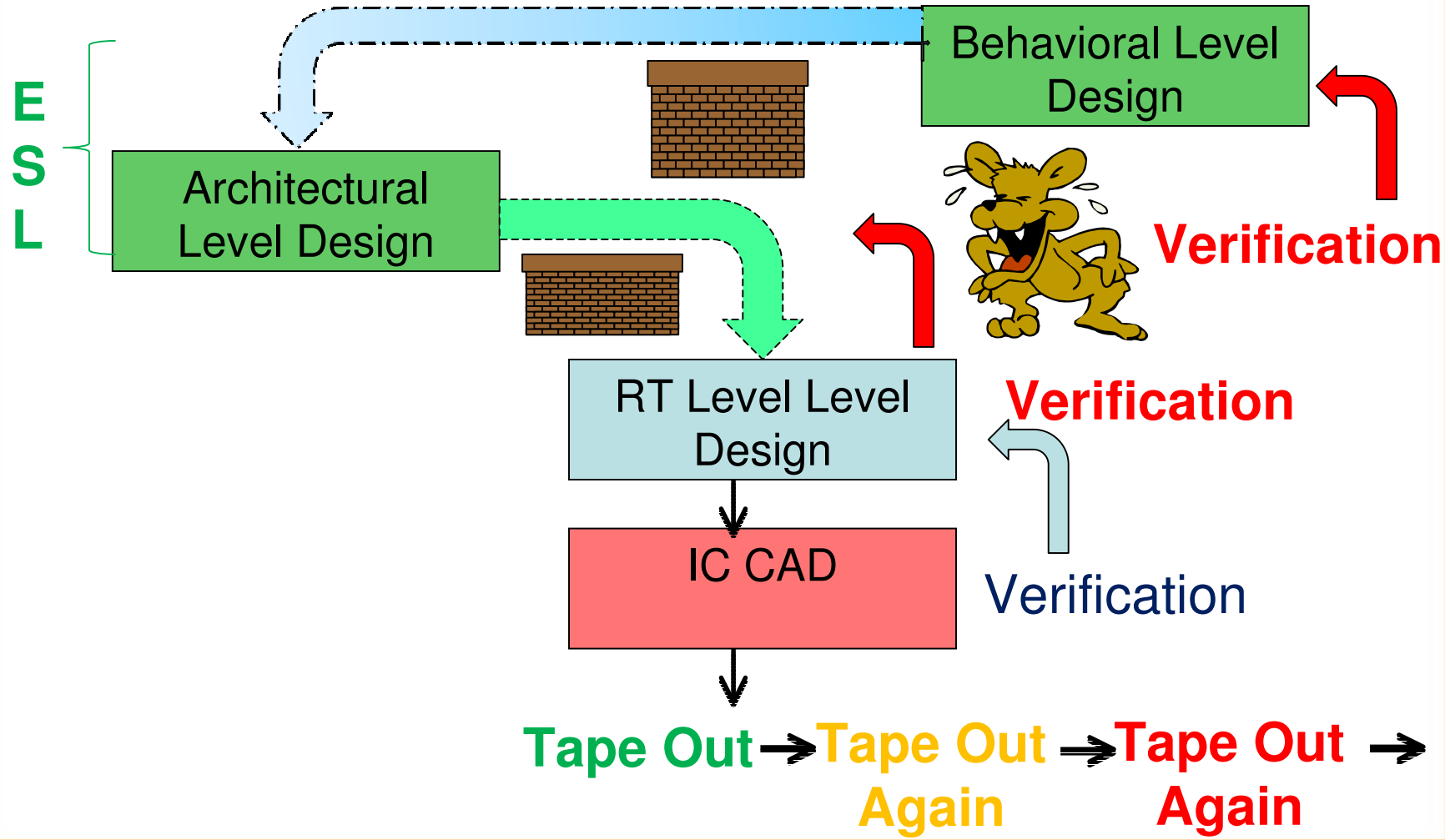
ELECTRONIC DESIGN STRATEGY & MARKET ANALYSIS

www.garysmithEDA.com

Has anyone actually seen this flow ?



Or is this more like it ?



Let's break the Design Flow into its parts

- In the beginning you have a Platform
- That gives you 70% to 90% of your gates
- Then you design the remaining 40 or 100 million gates
- Which brings up the subject of IP

Platform Based Design

- You didn't really think you started a 400 million gate SoC from scratch did you ?
- Your Platform is usually your last design.
- Oh you don't have one ? Then you buy one from your friendly Semiconductor vendor (i.e. TI's OMAP, Qualcomm's Snapdragon, or NVIDIA's Tegra).

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LESSON #1

Platforms are either Developed In-House Or Provided by Semiconductor Vendors

That gives you 70% to 90% of your gates

- The Platform is the “known” part of the design.
- Therefore that is the major IP market (you need to “know” the design before you can make an IP for it).
- That is the foundation of your design, it doesn’t give you competitive advantage.

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LESSON #2

Semiconductor companies, whether they buy the Platform or develop it In-House (from previous designs), make the money. The rest get the leftovers.

Then You Design the Remaining 40 or 100 Million Gates

- 100 million is a lot of gates to design !
- So it isn't just gluing a bunch of IP together after all.
- Processer IP sells here, which is why ARM is the #1 IP supplier.
- As does library based IP, which is why Synopsys is #2.

LESSON #3

This is where the competitive advantage is developed !

So this is where the money is !

Which brings up the subject of IP

- ITRS 1997 – Small Blocks
  - 2,500 gates to 74,999 gates
- ITRS 1999 – Large Blocks
  - 75,000 gates to 1,000,000 gates
- ITRS 2007 Very Large Blocks
  - Over 1,000,000 gates

Which brings up the subject of IP #2

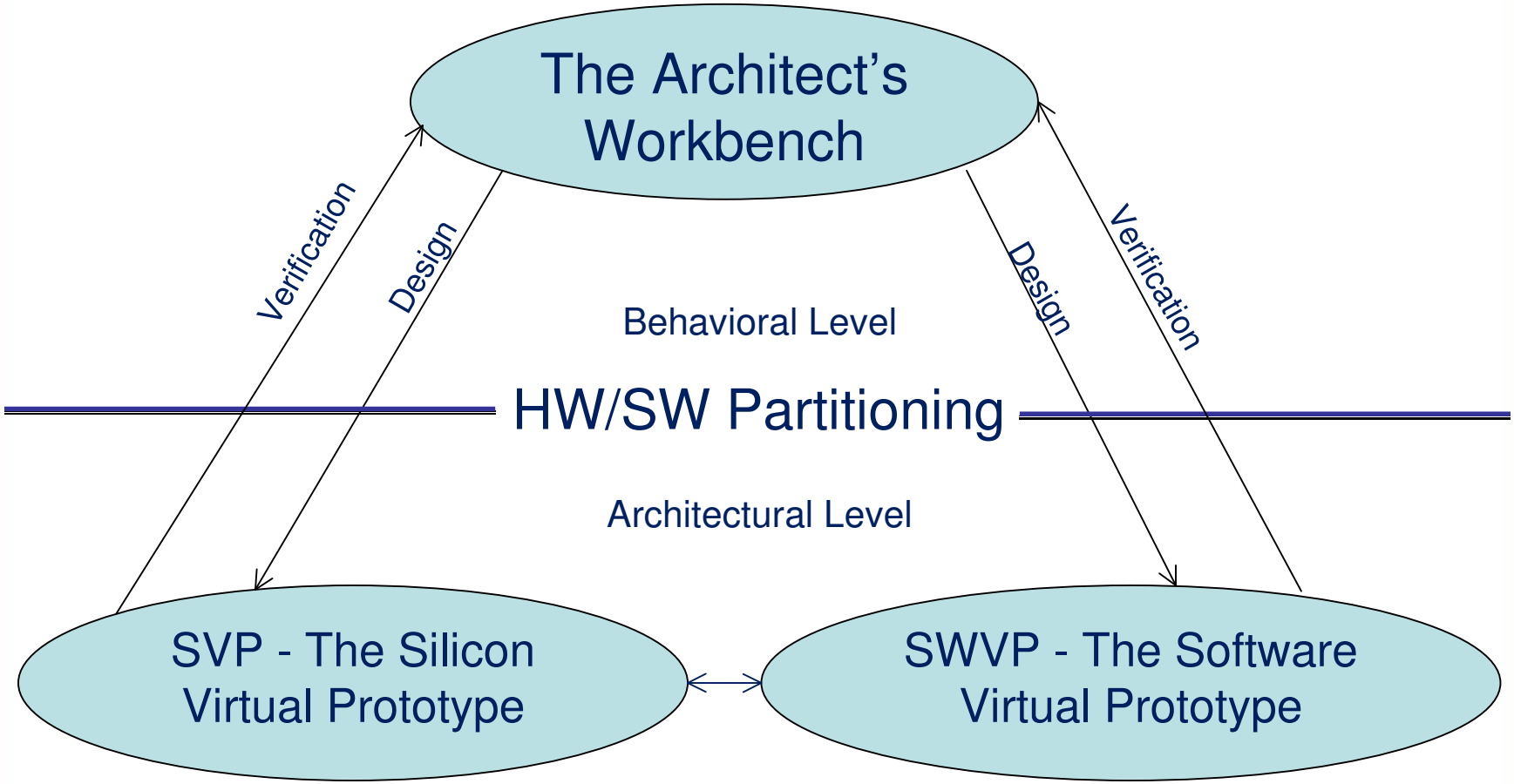
- Small Blocks
  - Sold primarily as libraries, with the exception of some analog blocks.
- Large Blocks
  - Some blocks are reconfigurable, for example memory.
- Very Large Blocks
  - Most blocks are “Modifiable” (you can add or remove Large Blocks without affecting the verification of the remaining blocks).
  - A high percentage of the Very Large Blocks are designed In-House, not by 3rd party IP providers.

Getting Back to The Flow

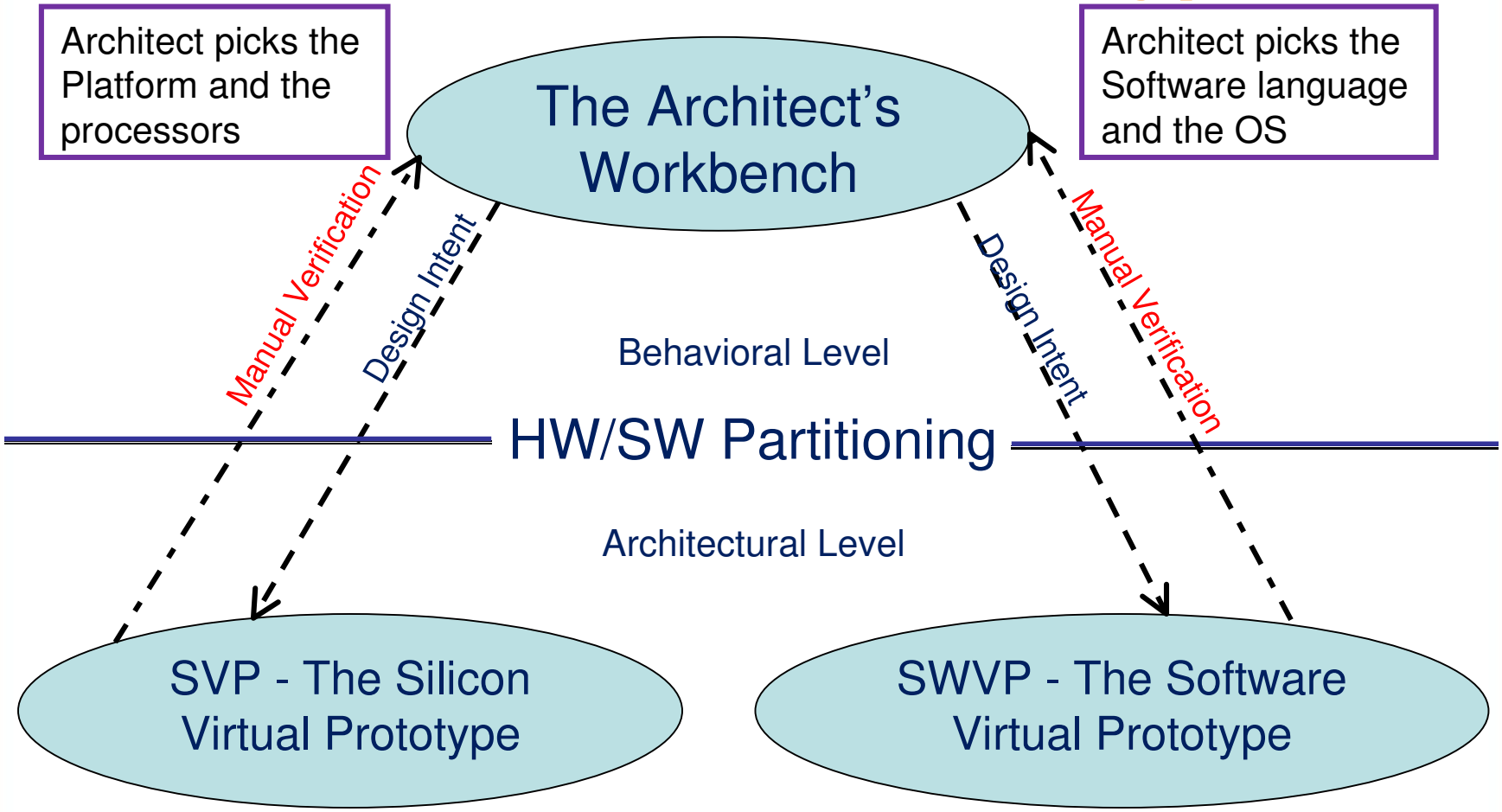
- So there are two flows
  - The design of the Platform
  - The design of the new block that gives you the competitive advantage.

- The Flows look the same but are either done by different design teams (Purchased Platform) or at a different time (In-House developed Platform).

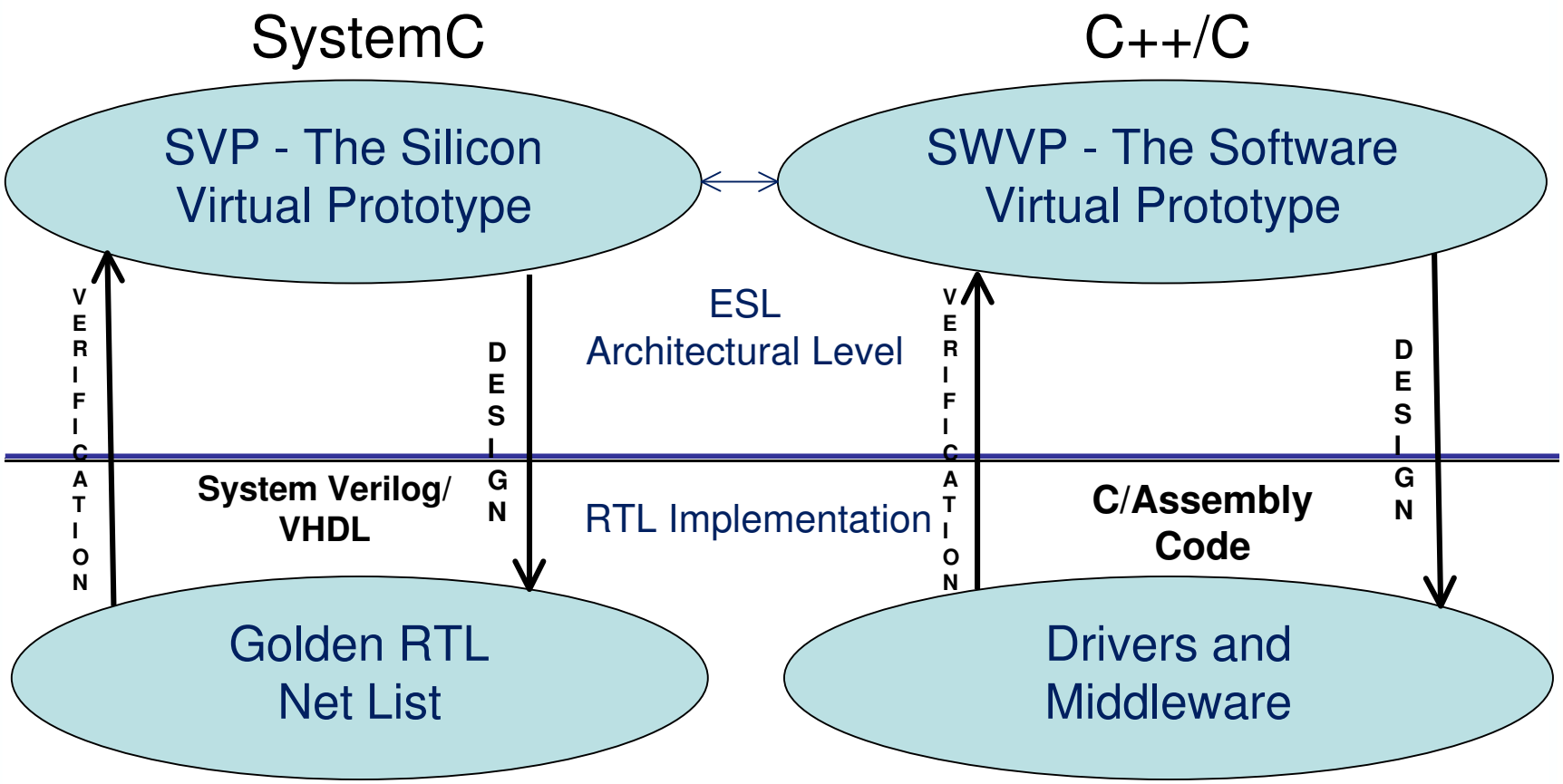
The Basic ESL Flow is The Three Virtual Prototypes



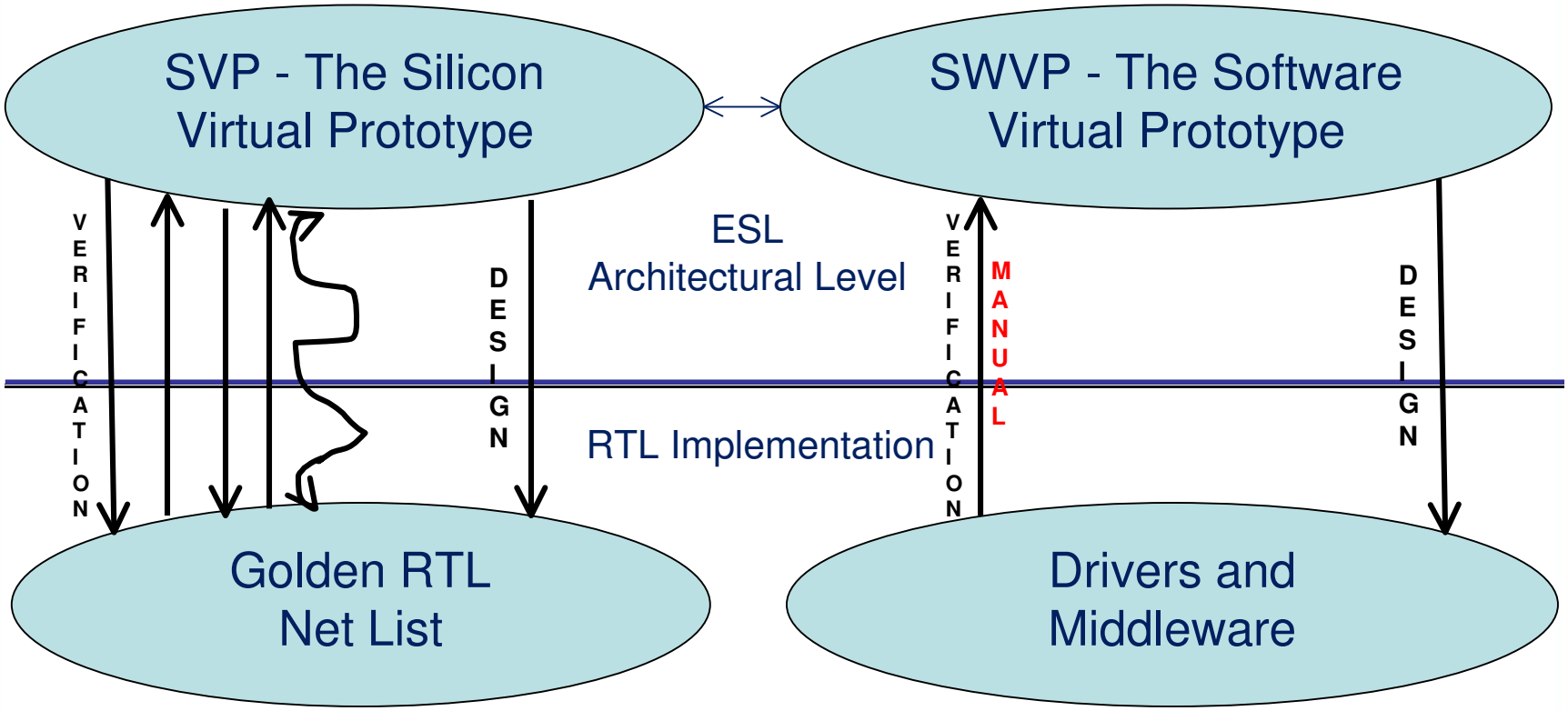
This Looks Better
The Three Virtual Prototypes



Then Down to RTL and real Code



Or This



Verification = Down, Add Assertions, Up – Down – Up – etc.

Responsibility

Responsibility - the Short Form

- Lucio Lanza's IC CAD speech
- All of the members of the Semiconductor Infrastructure have their individual responsibilities.
- We are all being measured by Moore's Law.

EDA's Responsibility

- EDA is responsible for developing the design tools that enable the IC design process.

EDA's Responsibility

- EDA is responsible for developing the design tools that enable the IC design process.

- Or -

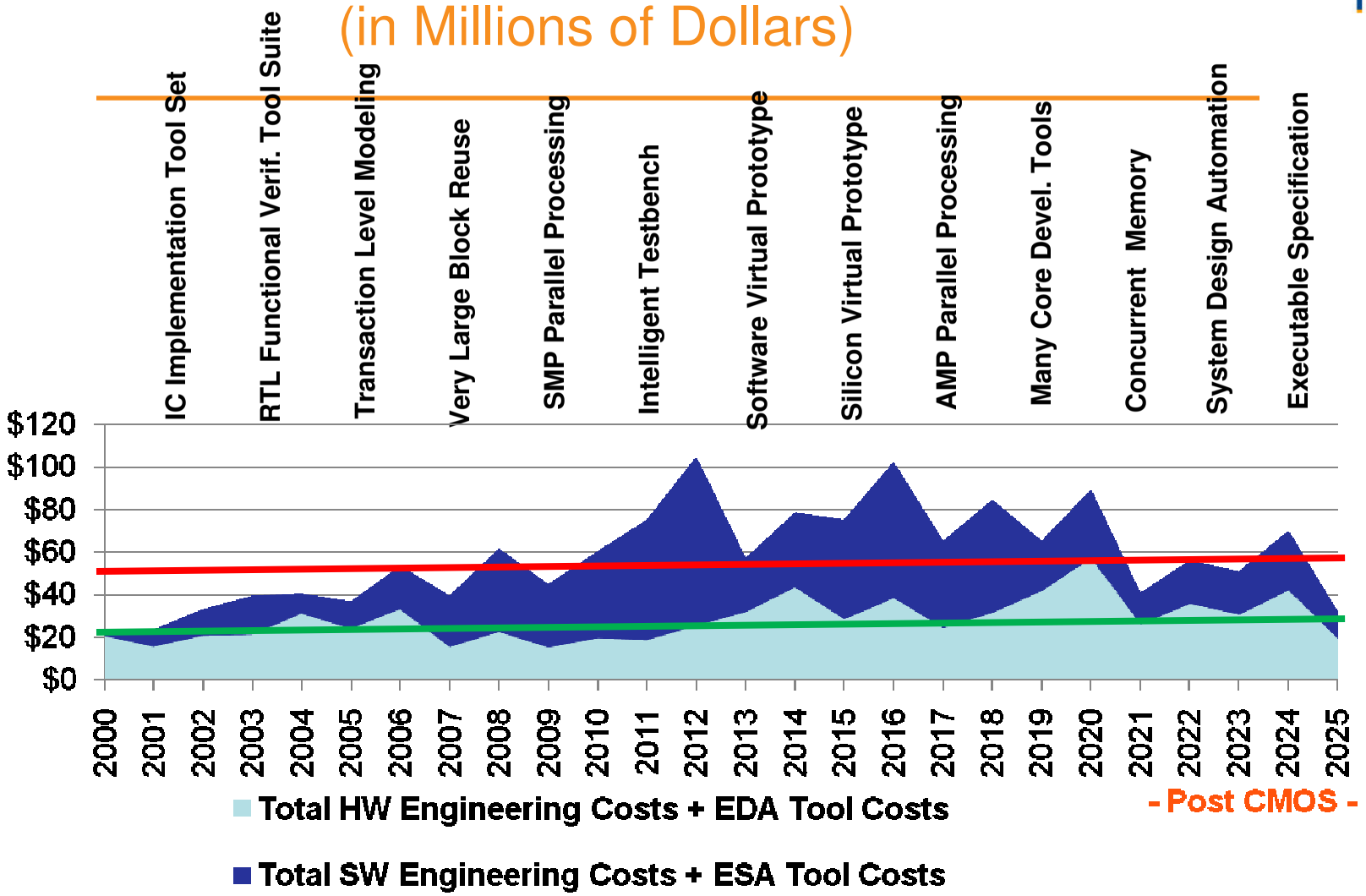
- EDA is responsible for developing the design tools that enable the IC design process, at a design cost that allows the ecosystem to operate at a profit.

What I'm not Saying

- This is not about the cost of EDA tools; that's lunch money.
- What I'm talking about is the level of automation. The costs are in the engineers needed to do the design.

ITRS Cost Chart 2010

(in Millions of Dollars)



Green: Start-Ups stop red: most SoC design stops

Source: Gary Smith EDA, April 2010

LESSON #4

The EDA Industry is responsible not only for enabling the design process, it is responsible for developing a level of automation that allows the design process to be affordable.