## Power Management Challenges

Bhanu Kapoor, Ph.D. Consultant/Owner, Mimasic EDPS 2011, Monterey, CA, 04/07/11 bkapoor@mimasic.com



## ISSCC, Feb. 2001, Keynote



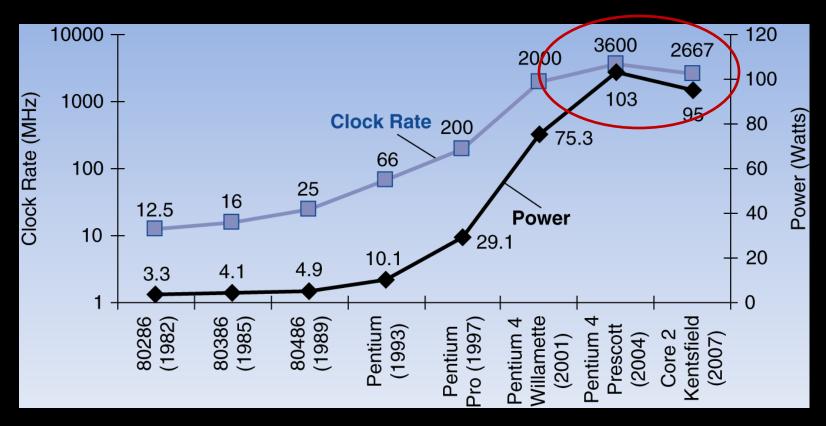
Patrick P. Gelsinger Senior Vice President General Manager Digital Enterprise Group INTEL CORP.

"Ten years from now, microprocessors will run at 10GHz to 30GHz and be capable of processing 1 trillion operations per second -- about the same number of calculations that the world's fastest supercomputer can perform now.

"Unfortunately, if nothing changes these chips will produce as much heat, for their proportional size, as a nuclear reactor...."



## **Power Trends**

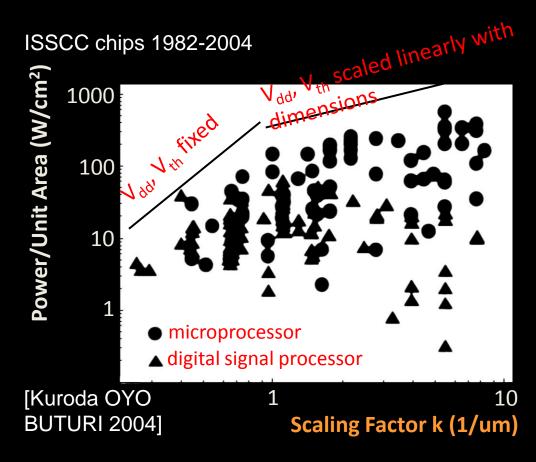


D. Patterson and J. Hennessey Computer Organization



#### **Increasing Power Density**

- As device dimensions
  (W, L, Tox) scaled down
  by a factor k, for high
  performance
- $V_{dd}$  and  $V_{th}$  fixed  $\rightarrow$ power/unit area  $\propto k^3$
- $V_{dd}$  and  $V_{th}$  scaled down linearly  $\rightarrow$  power/unit area  $\propto k^{0.7}$

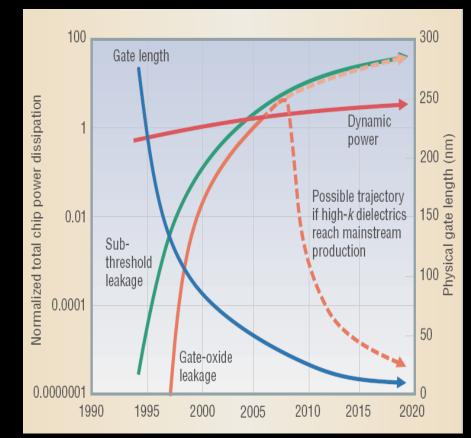


Chinnery and Keutzer, DAC 2005



# **Power Trends**

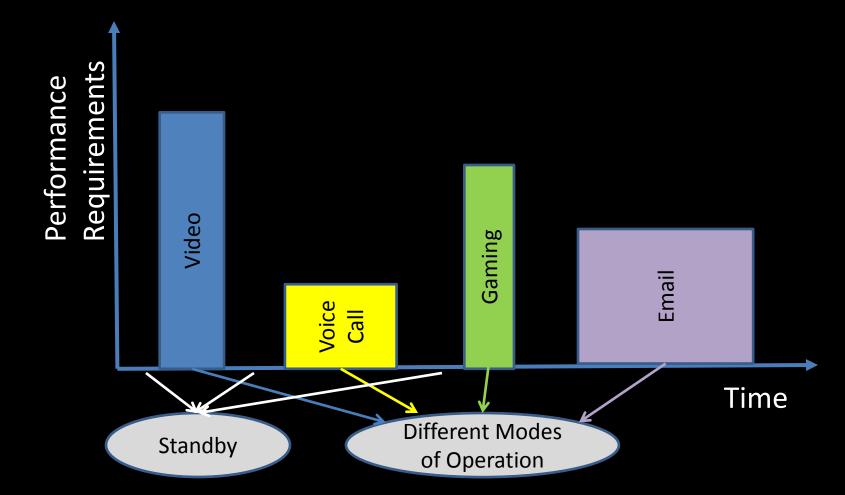
- **Power:** Dynamic , Leakage
- Dynamic: Activity, Frequency, Capacitance, Supply Voltage (V)
- Dynamic Power  $\alpha V^2$
- Leakage : Sub-threshold , Gate-Tunneling
- Leakage Power  $\alpha V$ , e<sup>-Vt</sup>
- Manage: Dynamic, Active Leakage, Standby Leakage



Power Trends, IEEE <u>D&T, 2003</u>\_\_\_\_\_

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## Power Consumption in a Mobile Phone



Voltage is the key variable to manage power in all modes



## **Power Types Targeted**

			Power Being Managed				
Technique			Standby Leakage	Active Leakage	Dynamic		
Power Gating	PG						
Retention with PG	RPG						
Multiple Supply Voltages	MSV						
Dynamic Voltage Scaling	DVS						
Adaptive Voltage Scaling	AVS						
Multi-Threshold CMOS	MTCMOS						
Adaptive Body-Biasing	ABB						

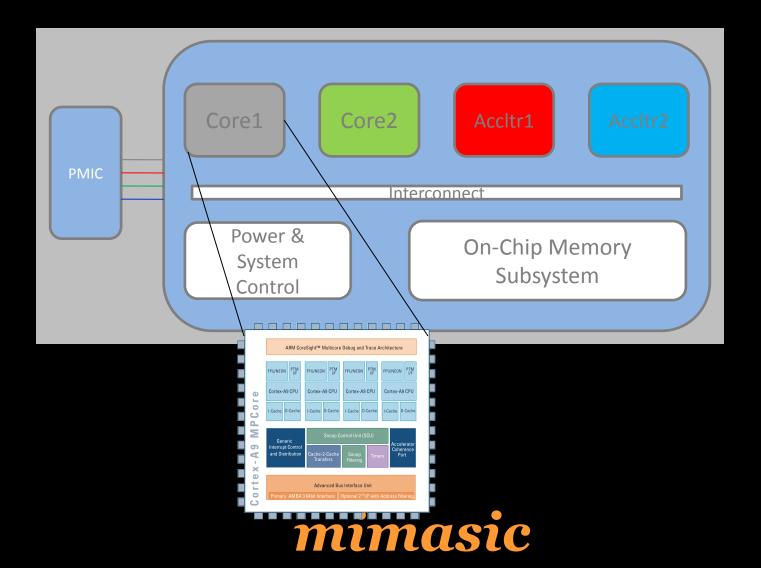
Primary

Secondary

**Verification Impact** 



## **Typical Power Managed SoCs**



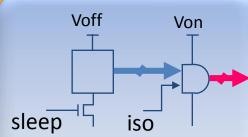
## Infineon Baseband Processor – ISSCC06

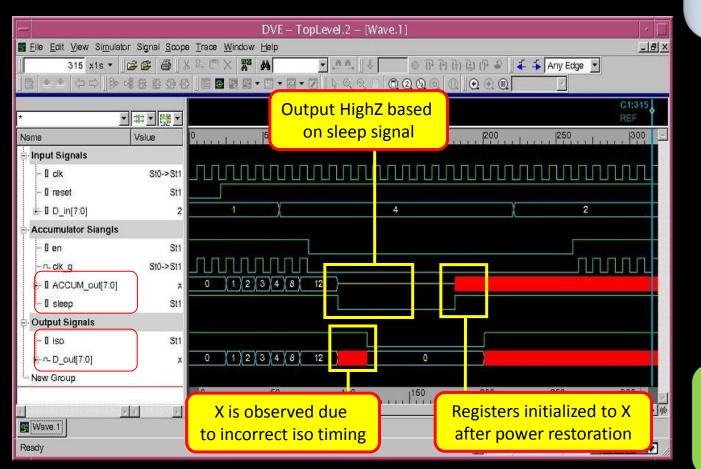
Application	Settings	ARM926 MHzX26	DSP MHzX26	Combo*	Peripheral Bus 1	Peripheral Bus 2	Analog	Standby Domain
GSM Voice	6.60-AMR	f1	f2	On	Off	Off	On	On
GSM Voice	6.60AMR+Handsfree	f1	f2a	Off	Off	Off	Off	On
GSM Idle	Sleep Mode	0	0	On	Off	Off	On	On
GSM Idle	Paging	f1	f1	On	Off	Off	On	On
Data Down.	HSDPA 3.6Mbps	f4	0	On	On	Off	Off	On
Data Down.	UMTS PS 384 kbps	f2	0	On	On	Off	Off	On
Data Down.	E-GPRS	f2	f3	On	On	Off	On	On
Video Enc.	MPEG-4 20fps QVGA	f5	f2	On	On	On	On	On
Video Tel.	MPEG-4 15fps QCIF	f3	f2b	On	On	On	On	On
Music Repl.	MP3	f1	f1	On	Off	Off	On	On
Music Repl.	MP3 + Paging	f2	f1	On	Off	Off	On	On



## **Challenge: Power Verification**

#### Incorrect Isolation Sequence Synopsys VCS





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**Intended Behavior** 

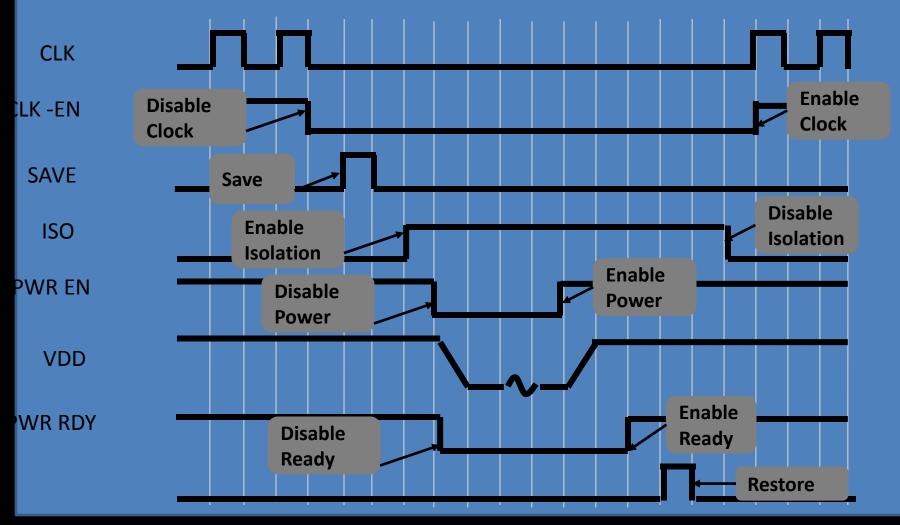
- 1. Gate the clk
- 2. Assert iso to 0
- 3. Assert sleep to 0

**Actual Behavior** 

- 1. Gate the clk
- 2. Assert sleep to 0
- 3. Assert iso to 0

Control signal sequence error is discovered due to X propagation

## **Power Verification**



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## ITRS Process Technology Roadmap

#### Planar Bulk CMOS

Supply	24 22	2 20	18	17
	.9 0.87	7 0.84	0.81	0.78
Threshold 0.29 0.29 0.29 0.2	29 0.29	9 0.29	0.3	0.3

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UTB FD MG i.e., FinFETs

## Challenge: Power Management Techniques

- Active Power: Voltage Scaling and Multi-Vt
- Limited/Reduced performance from fixed Vt, and doubling number of transistors per node
- Power density becomes a bigger issue
- Variability makes leakage management difficult [i.e., 20% of chips with higher leakage]



# **Challenge: Power Modeling**

- System-level modeling is key to optimization
- System-level modeling is difficult
  - Power dependent on physical knowledge
- Regular structures help (FPGAs)
- More efficient utilization of existing PM techniques requires system-level design/ visualization
- Hardware/Software partitioning, Low Power Software



## Low Power Software Development

- Power gains due to parallelization much better than performance gains: assumes voltage scaling – power corollary to Amdahl's Law
- Parallel software is a challenge
  - Amdahl's Law [Sky is falling!]
  - Programming has its own challenges
- Parallel software is the key to low power software
  - Slow and steady wins the (LP) race
  - Parallel software with voltage scaling controls



# Summary

- Doubling of the cores per generation becomes an issue given limited voltage scaling
- Power management techniques challenged in scaling scenario
- Power modeling remains a challenge
- Low Power Software is a key to power management going forward

