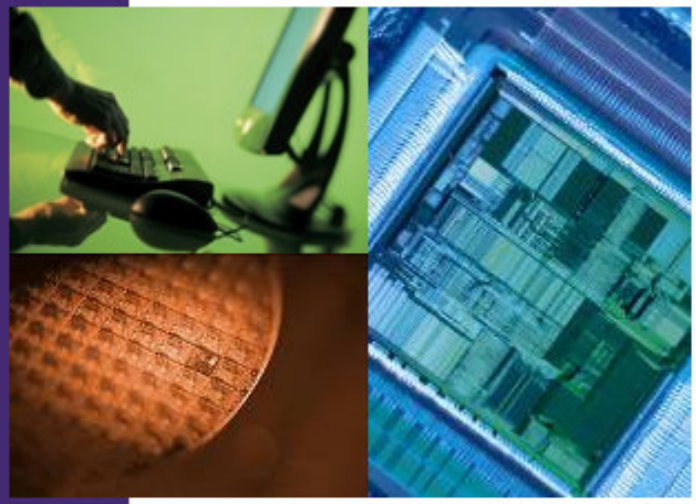
Challenges in the pattern information-transfer channel



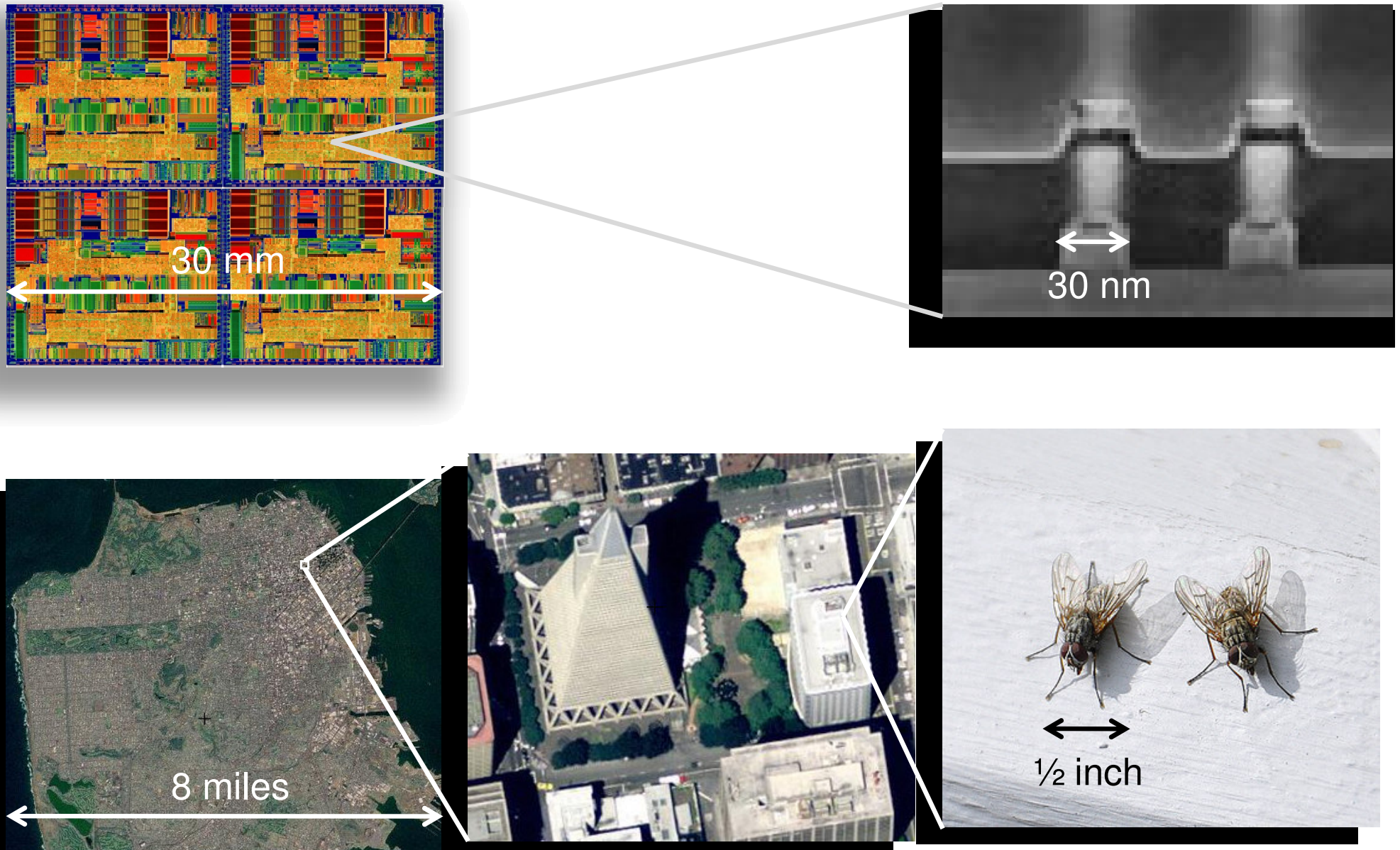
Mike Rieger
Hillsboro, OR

SYNOPSYS®
Predictable Success

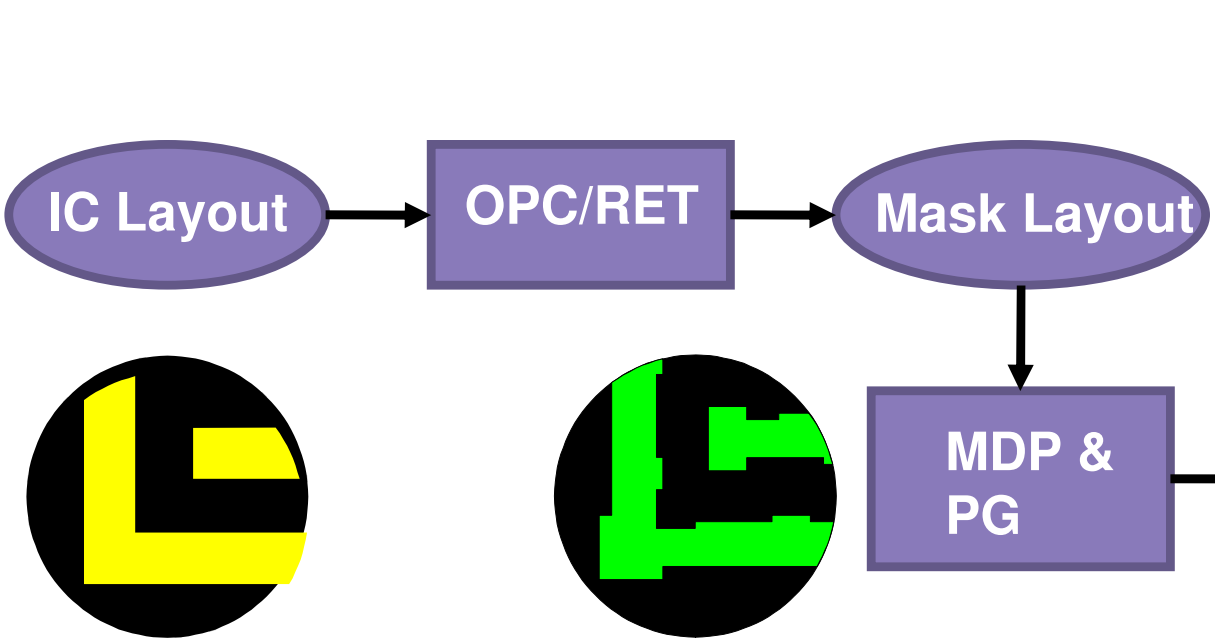
Outline

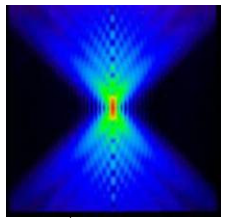
- The challenges:
  - Smaller features.
  - Higher feature density.
  - At decreasing cost / function.
- Survey new lithography & process technologies to address those challenges.
- Focus on information density (not just linewidth)
- Outline layout constraints required to enable lithography innovations.

Information density in a microlithographic image

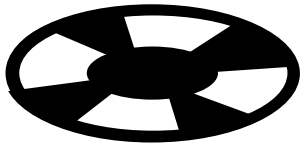


The pattern communication channel

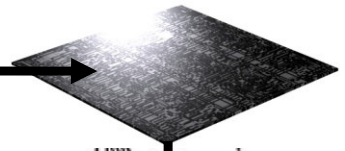




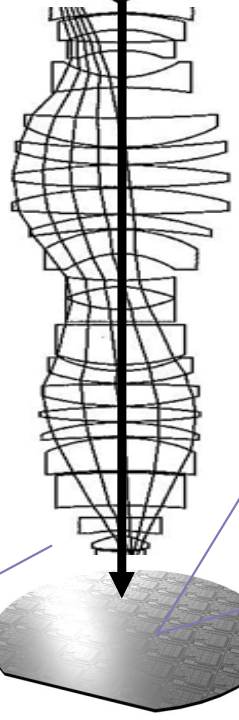
Light



Source



Mask



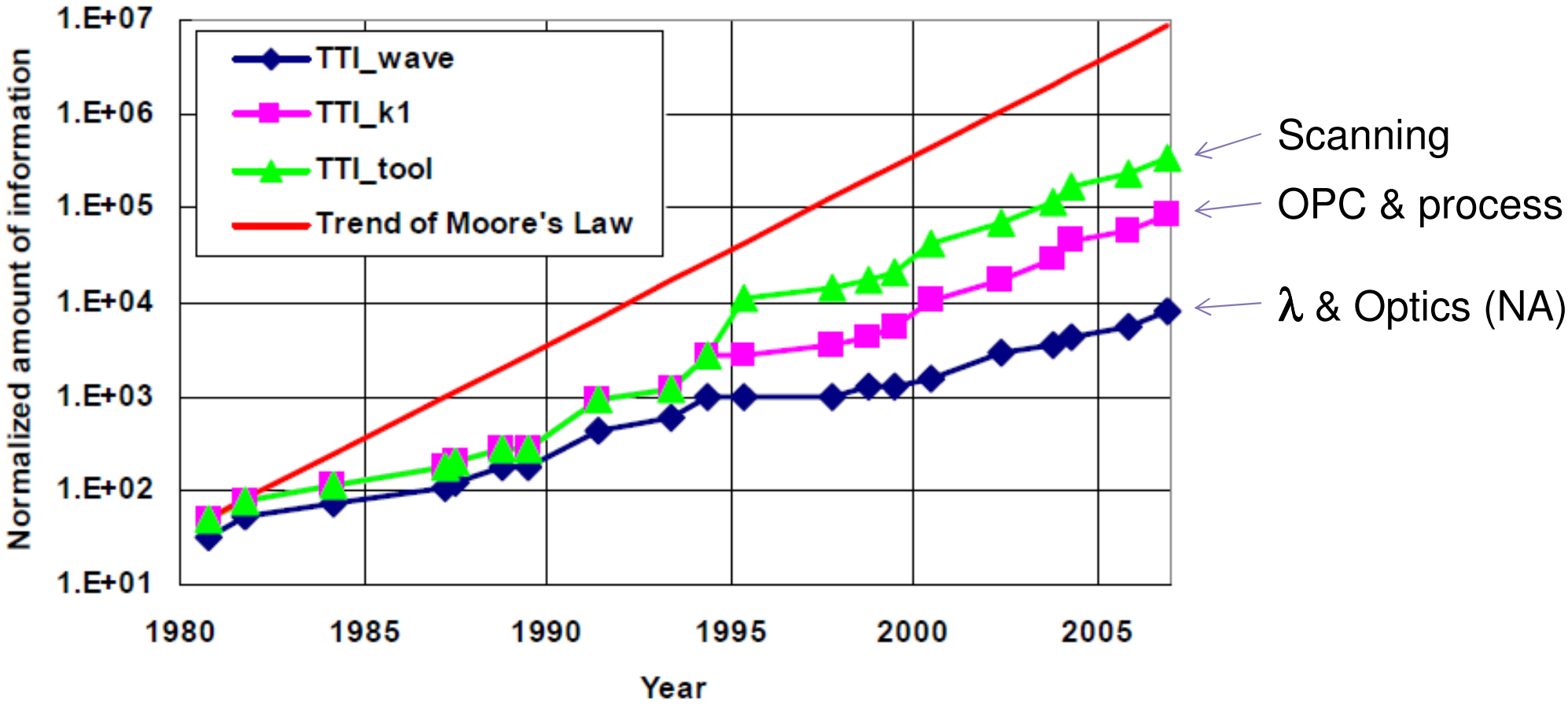
Lens

Modern scanner lens
- *f*/ 0.55
- 5000lp/mm
- 26mm field

http://www.zeiss.com/

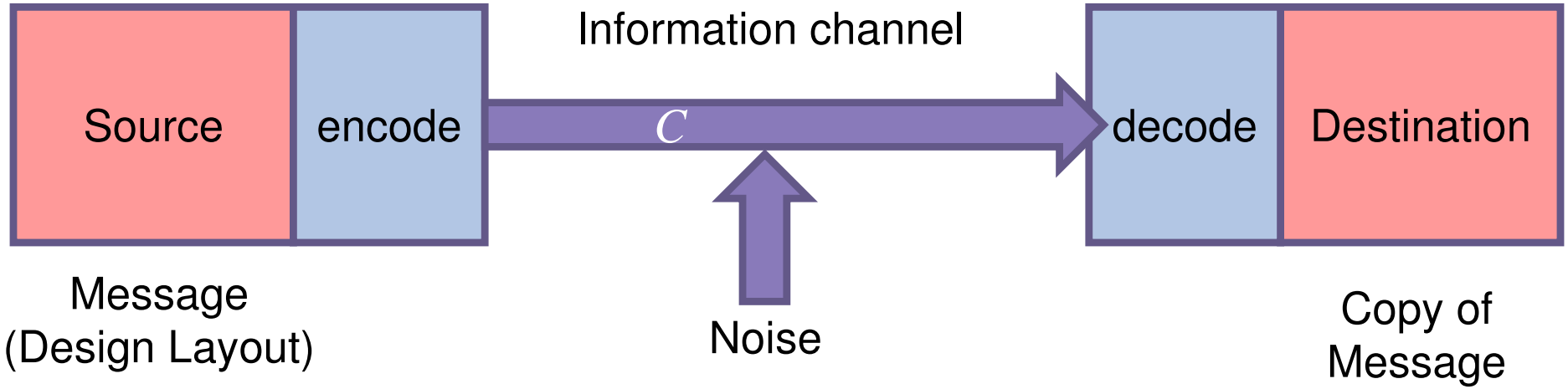
Wafer

Information capacity of the lithography channel is growing more slowly than Moore's Law



Tomoyuki Matsuyama, *et al*, Nikon, 2006

Information theory perspective

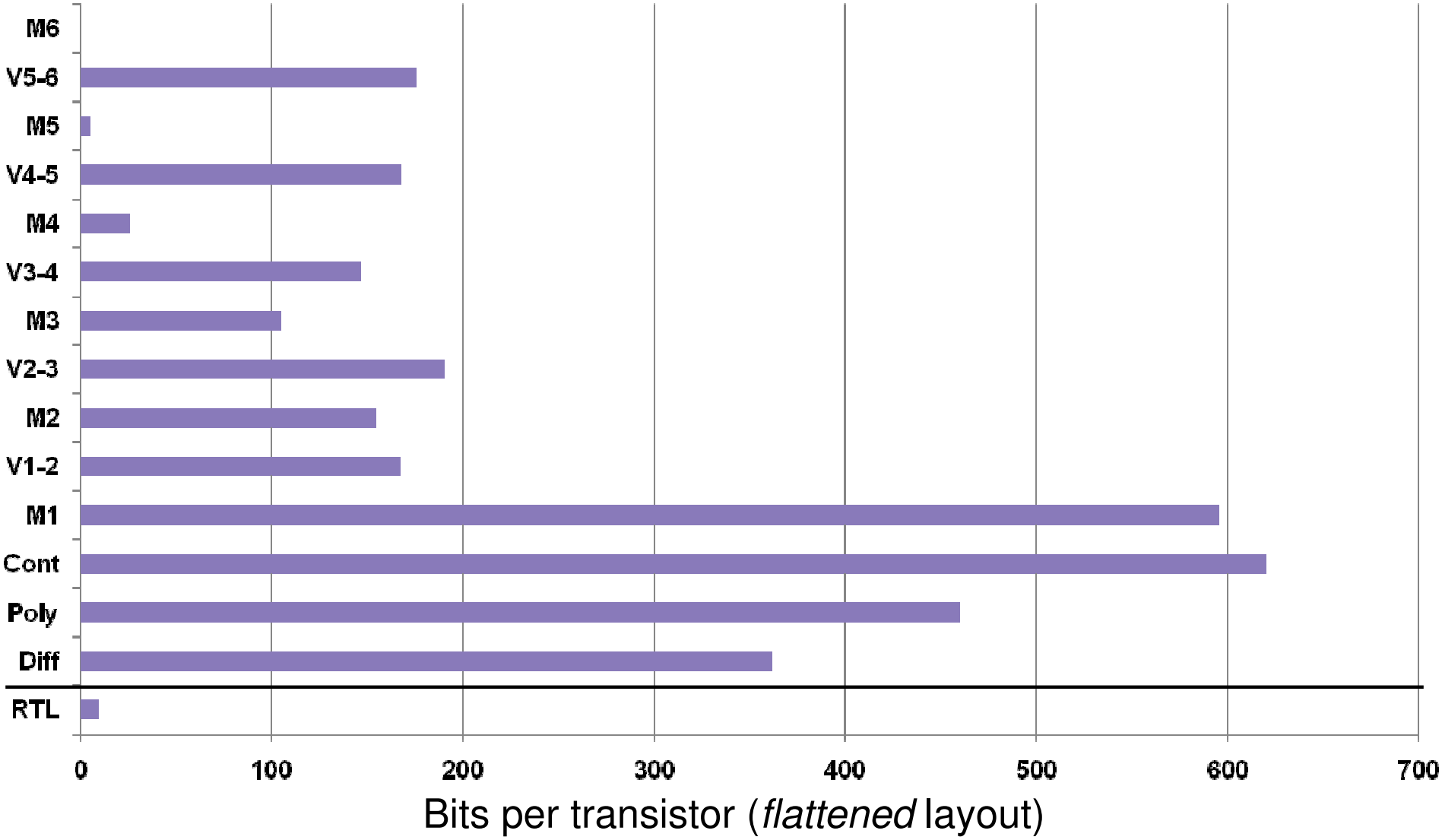


Channel capacity is fundamentally limited by the bandwidth and the signal to noise ratio.

$$C \propto BW * Log(S/N)$$

from C.E. Shannon, *A Mathematical Theory of Communications*,1948

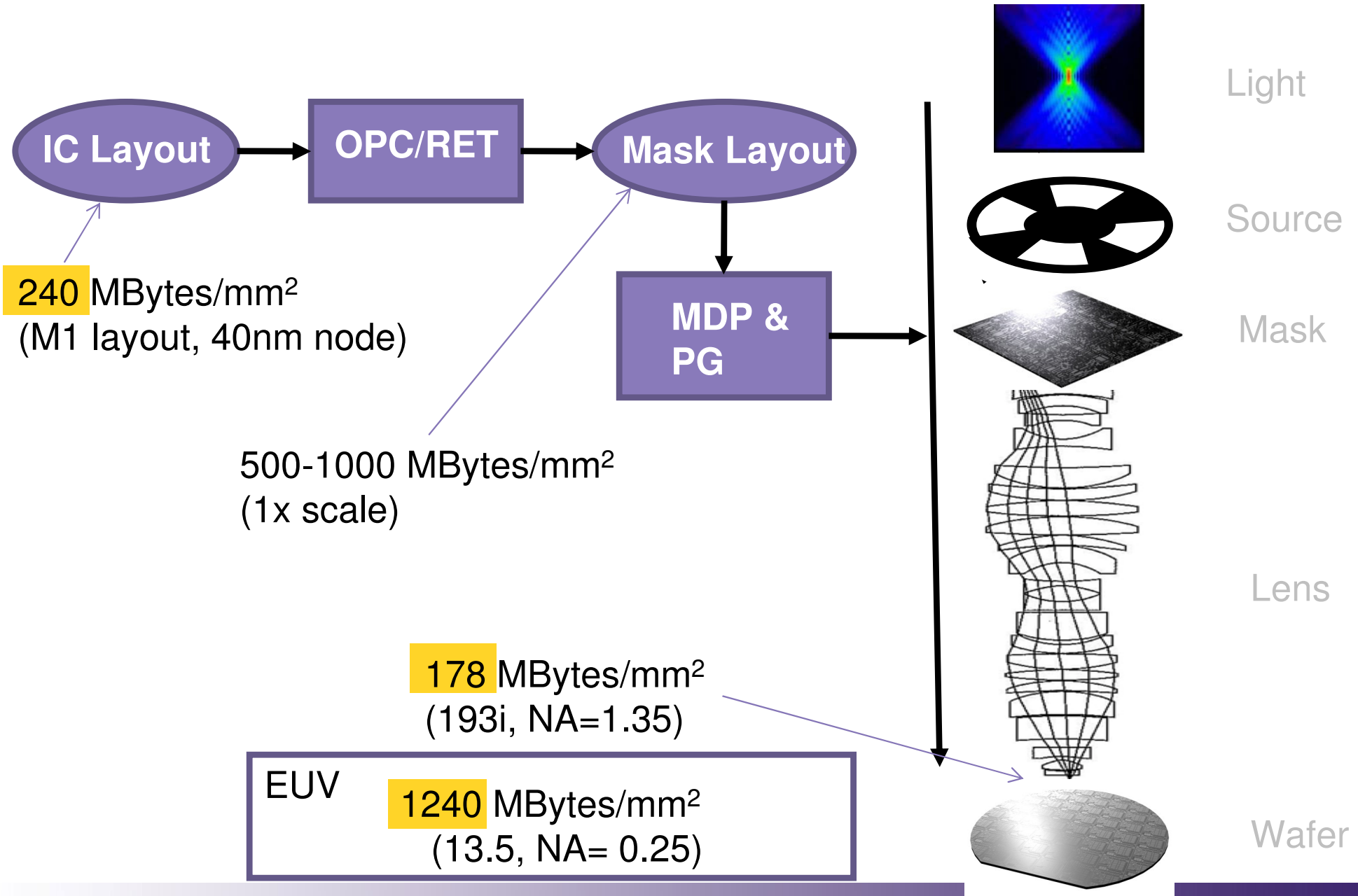
Information contained in a sample design layout (logic, 40nm node)



- Transistor density = 3.2 M transistors/ mm^2

Assumption: 32 + 32 bits per polygon vertex.
RTL (9-bits/transistor) is hierarchic

Information density in the channel



SYNOPSYS® Predictable Success

Improving Channel effectiveness

Four options:

1.Increase spatial bandwidth

- Optics & illumination

$$BW \leq \frac{2\,NA}{\lambda}$$

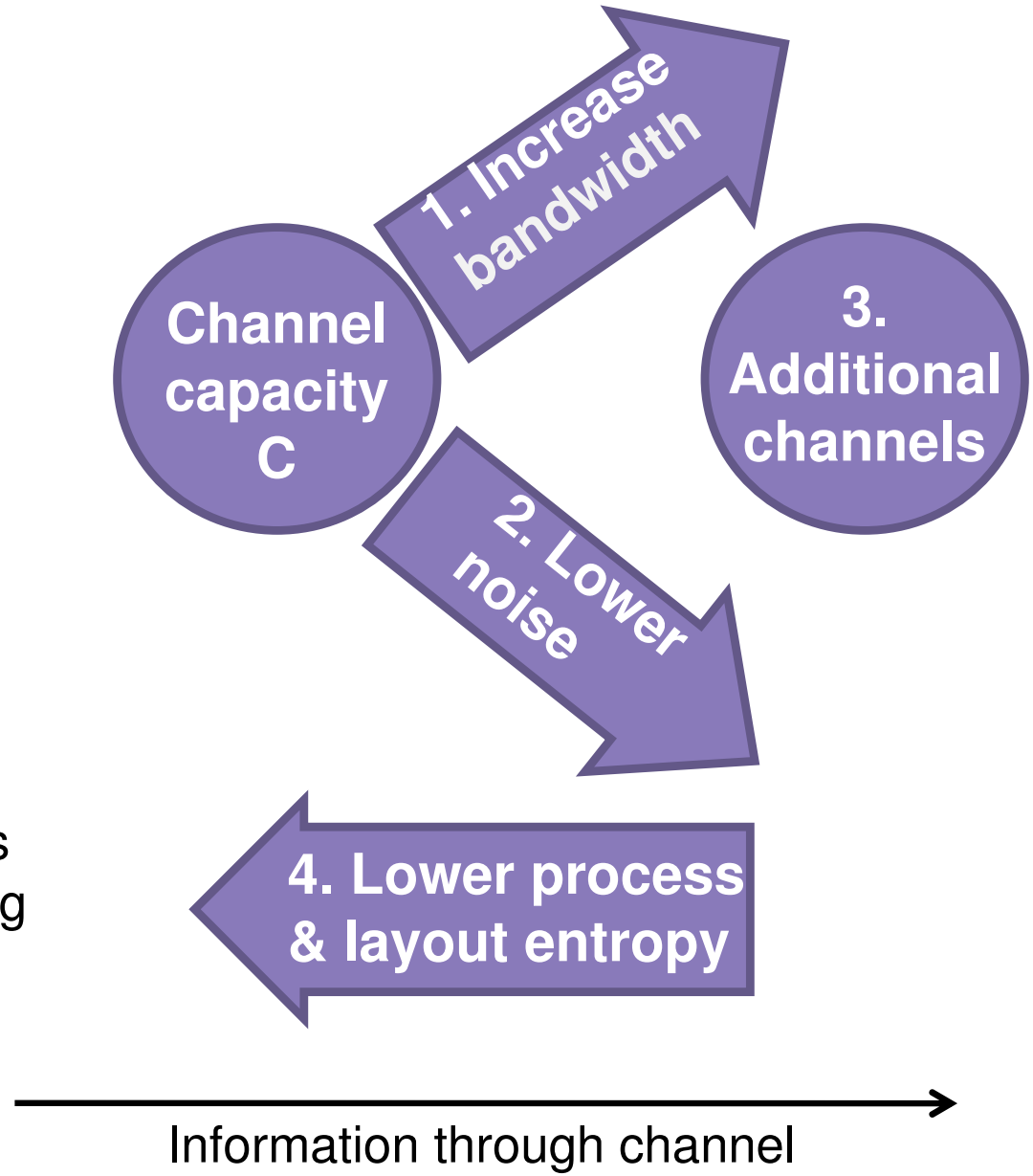
2.Increase Signal to Noise ratio in channel.

$$C \;\alpha\; BW * Log(S/N)$$

3.Add more “parallel” channels.

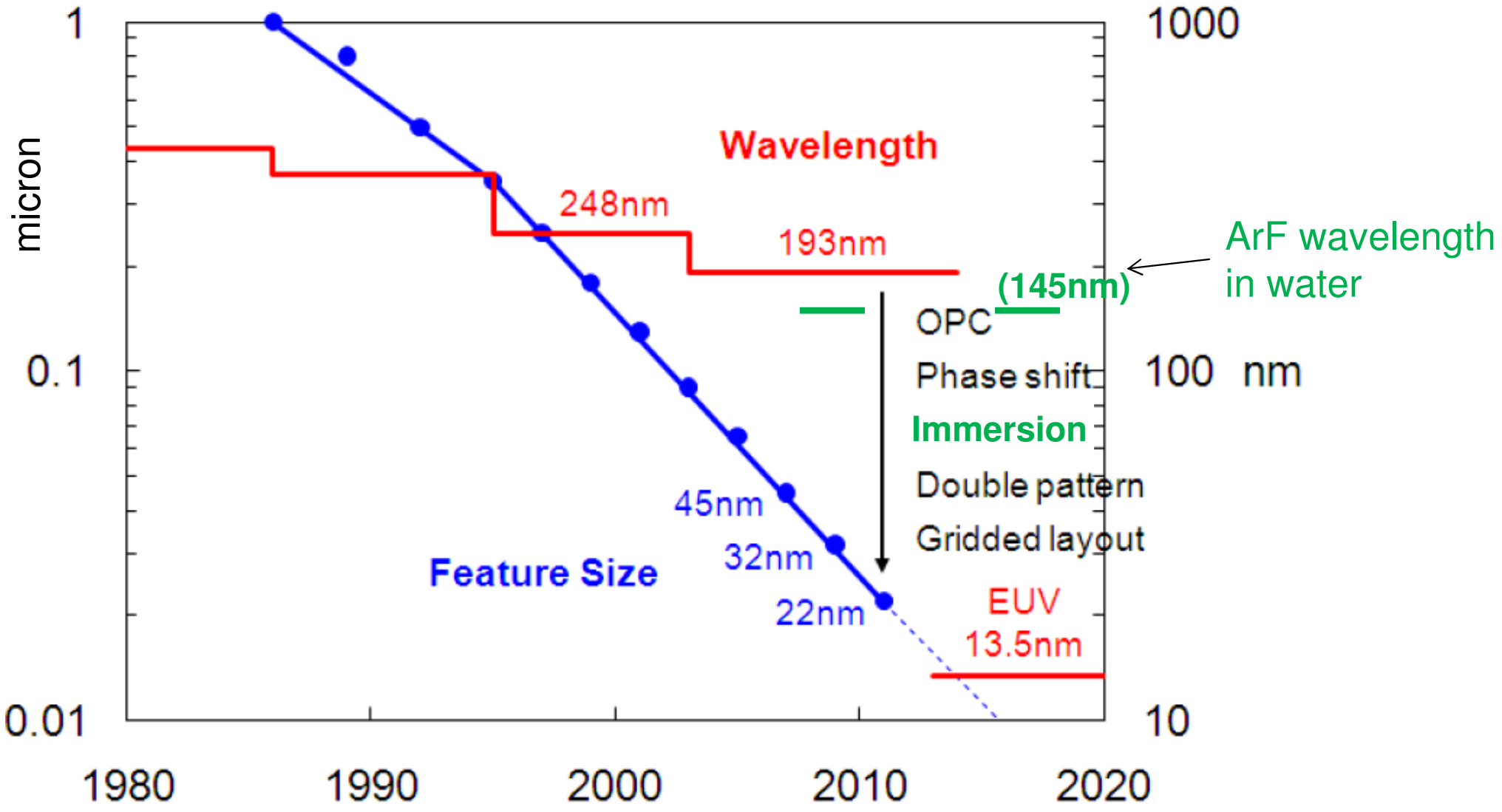
4.“Compress” information:

- Use lithography and process innovations to supply missing information, thus lower process entropy.



Increase bandwidth: wavelength & optics

$$C \propto \underline{BW} * Log(S/N)$$

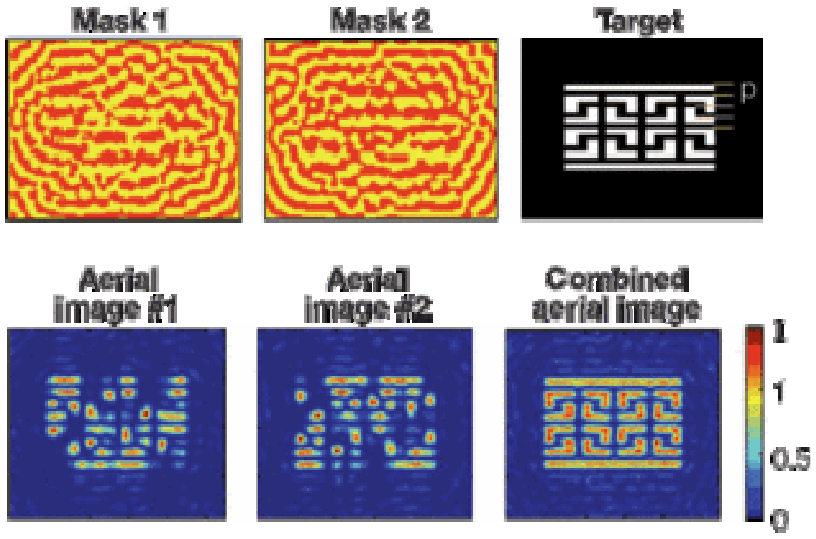


(adapted from) Mark Bohr, SPIE 2011

Increase bandwidth: Multiple exposure strategies

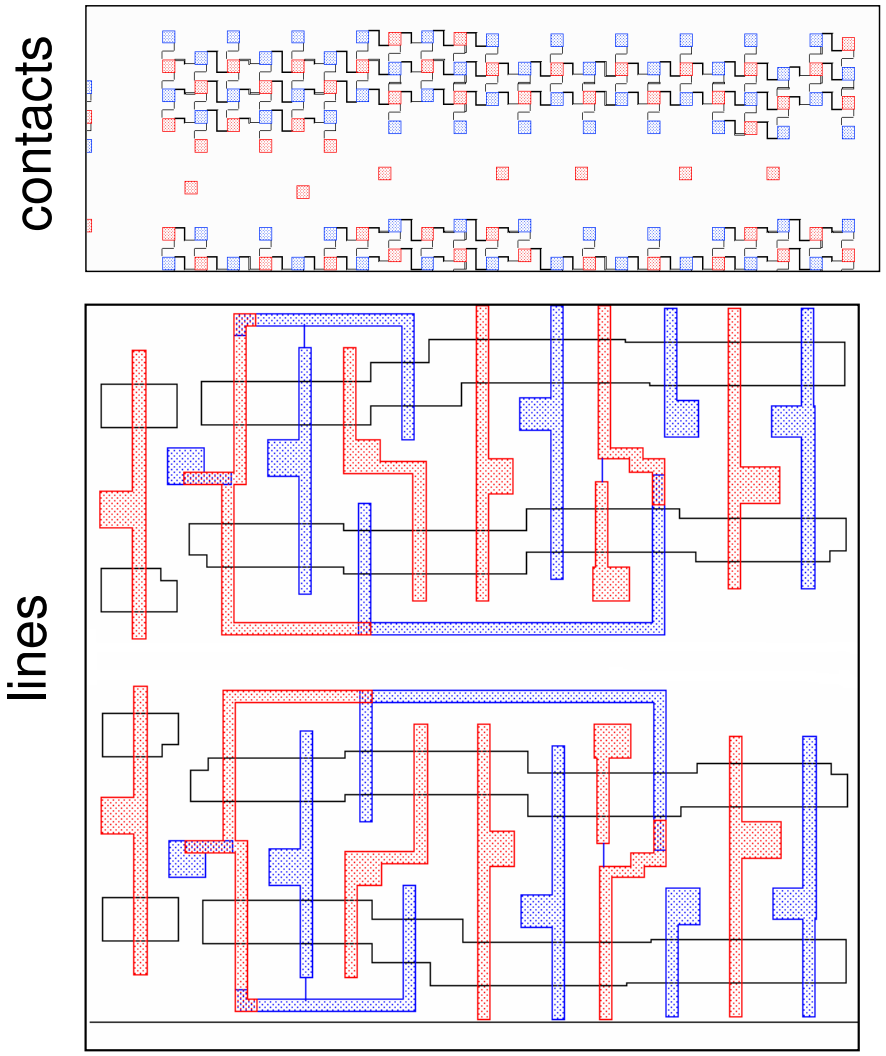
$$C \propto \frac{N}{} * BW * Log(S/N)$$

Double exposure lithography



Amyn Poonawala, Computer Engineering Department, U. of California, Santa Cruz **Yan Borodovsky**, Portland Technology Department, Intel Corp. **Peyman Milanfar**, Electrical Engineering Department, U. of California, Santa Cruz

Pitch splitting



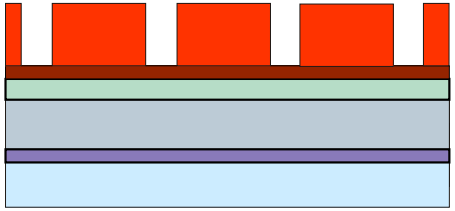
Layouts courtesy of IMEC; coloring by Synopsys

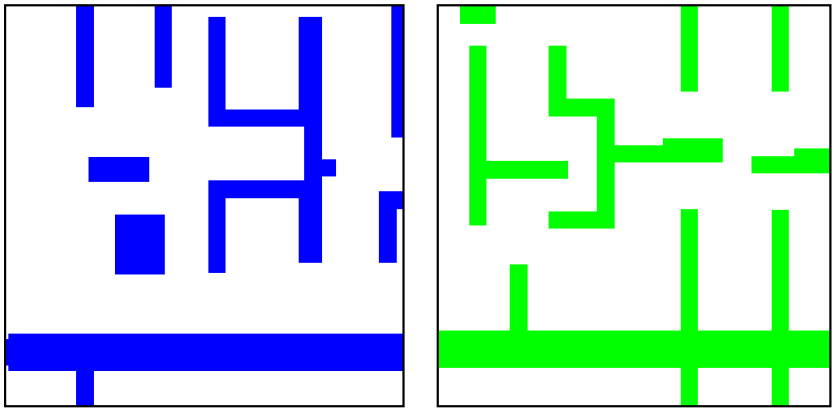
Costs of multiple exposure methods:

- Reduced litho throughput.
- Increased mask cost
- Layout “colorability” restrictions.

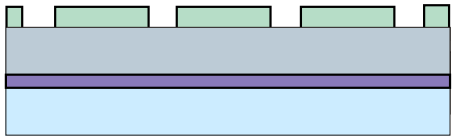
Double Patterning – LELE pitch splitting

1st trench imaging

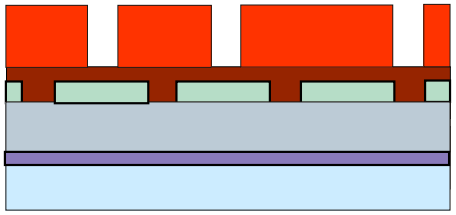


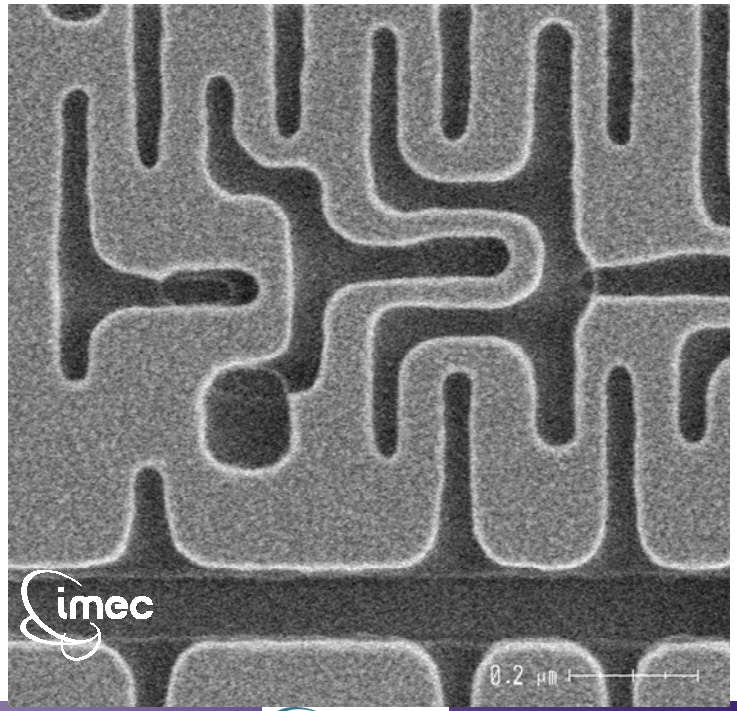


Hard Mask etch
Resist/BARC strip

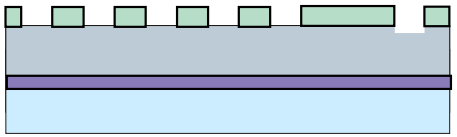


2nd trench imaging

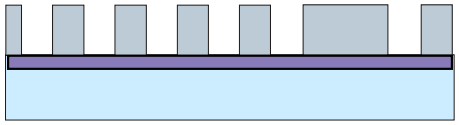




Hard Mask etch
Resist/BARC strip



transfer
to dielectric



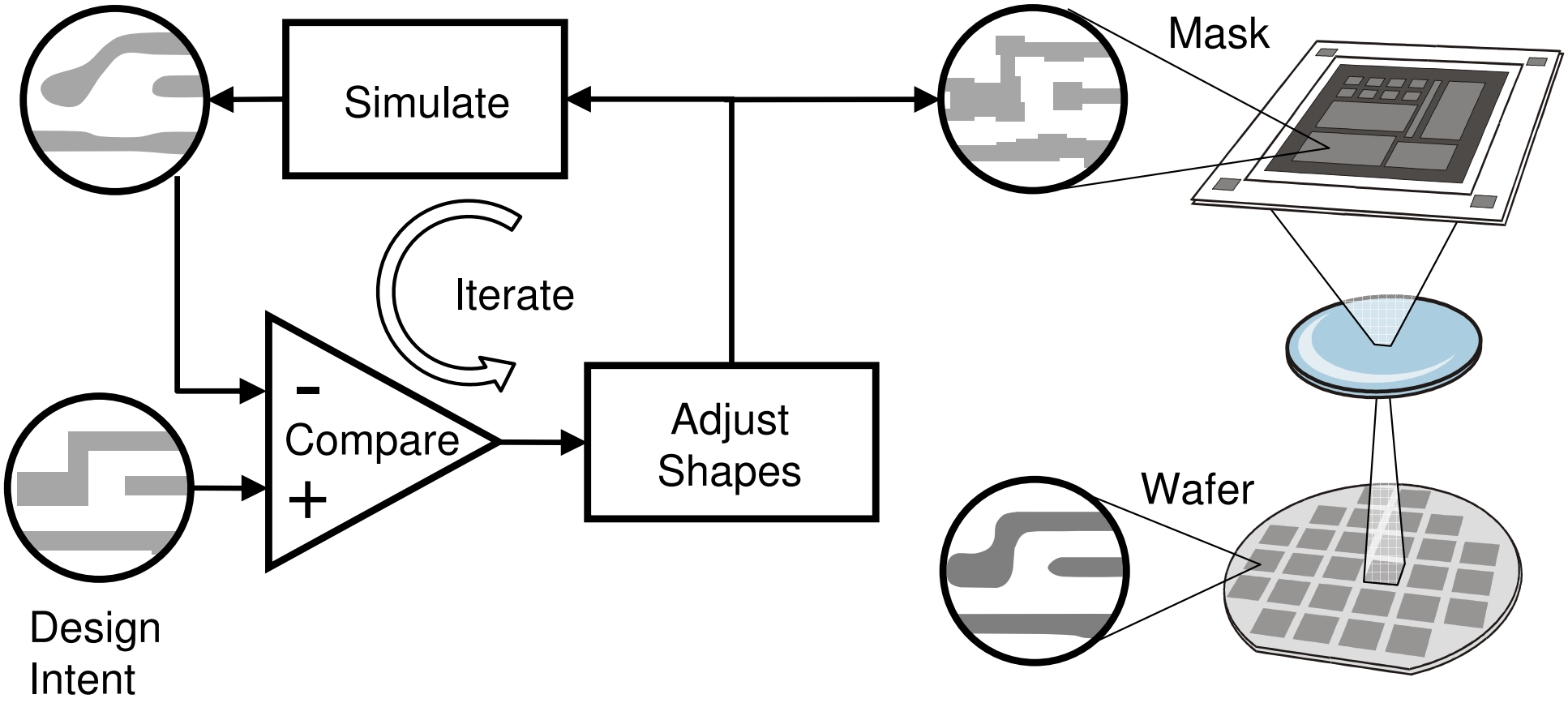
V. Wiaux, et. al. SPIE Vol. 6924-08, 2010

imec

SYNOPSYS®
Predictable Success

Lower systematic noise with OPC

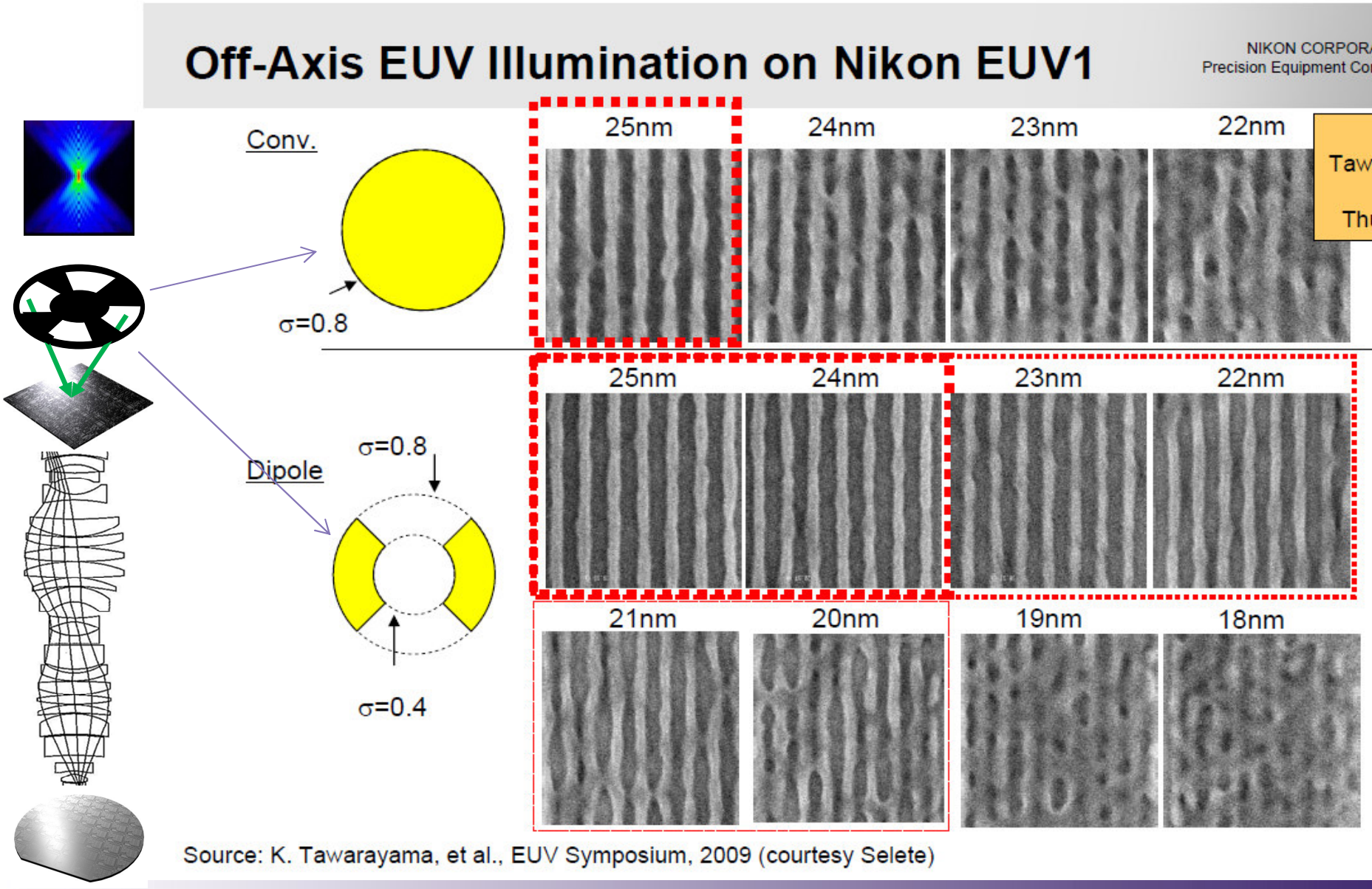
$$C \propto BW * Log(S/N)$$



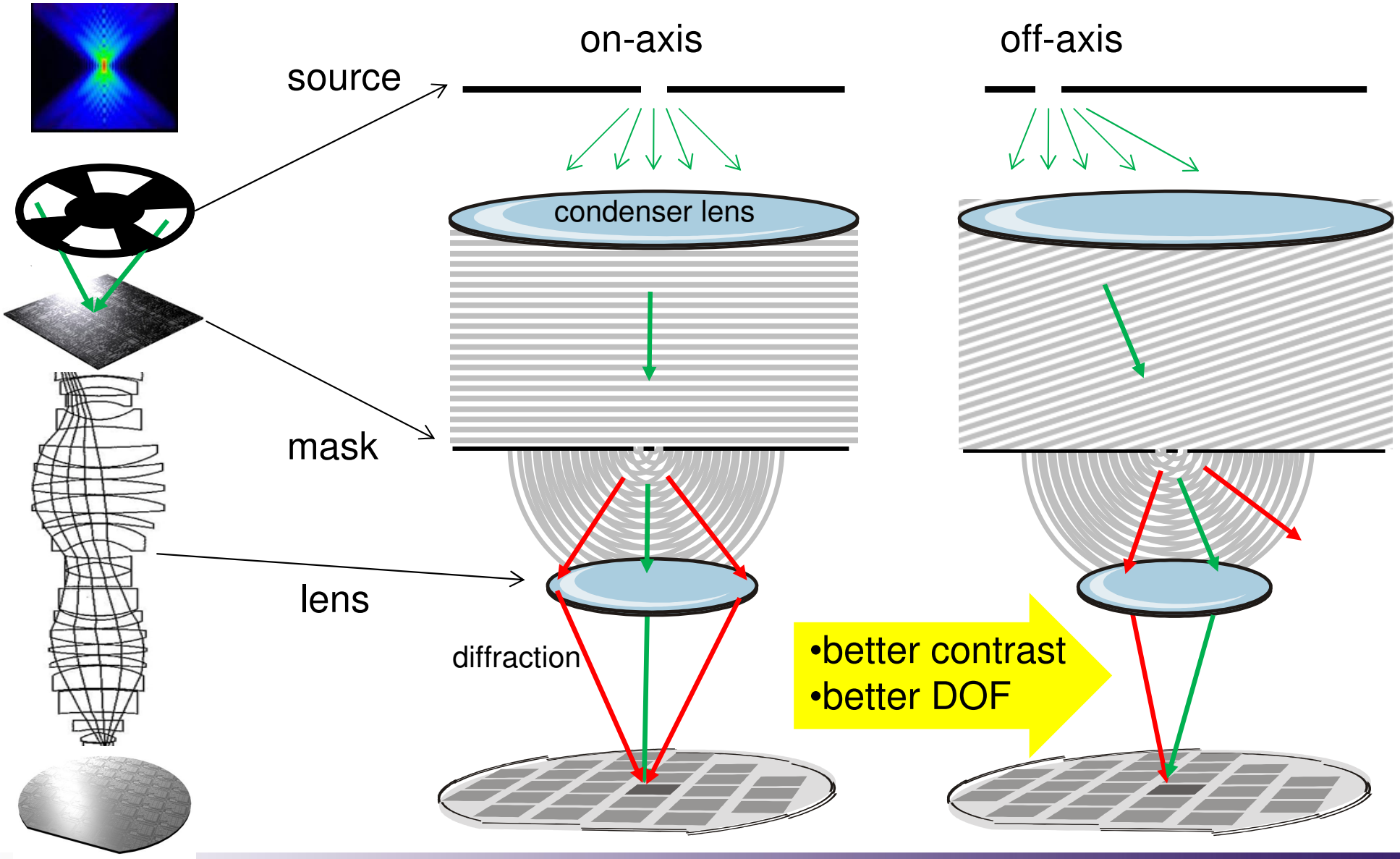
OPC removes predictable, localized feature distortions

Lower random noise with source optimization

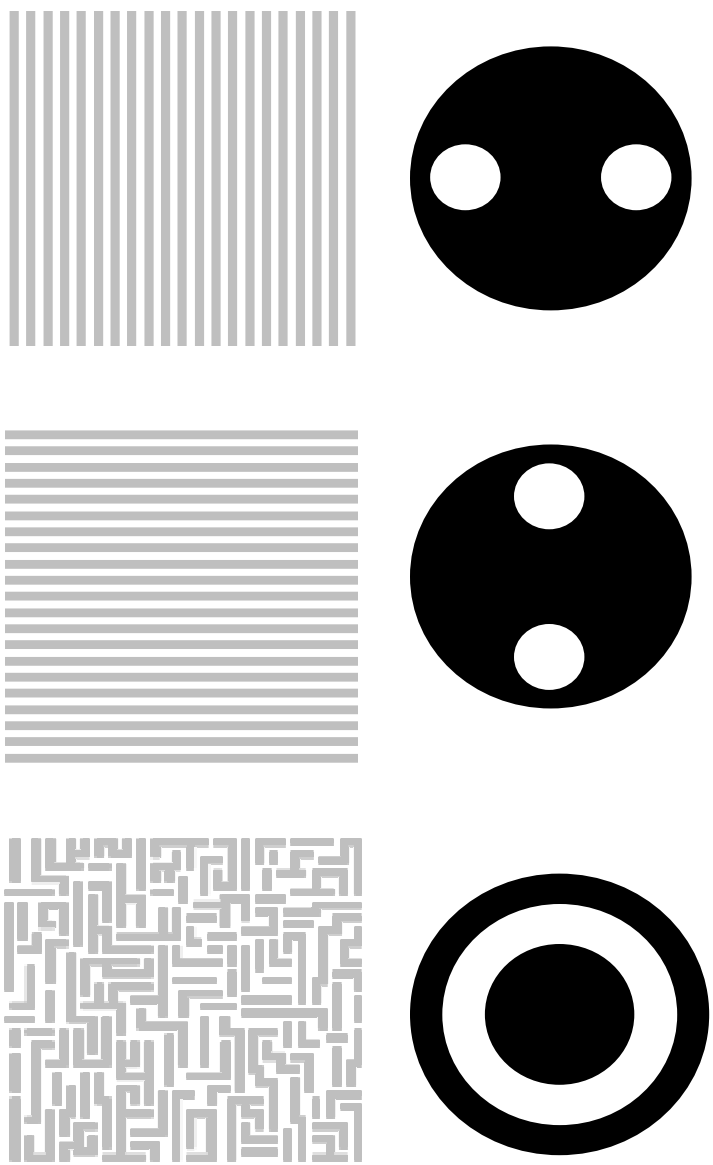
$$C \propto BW * Log(\underline{S/N})$$

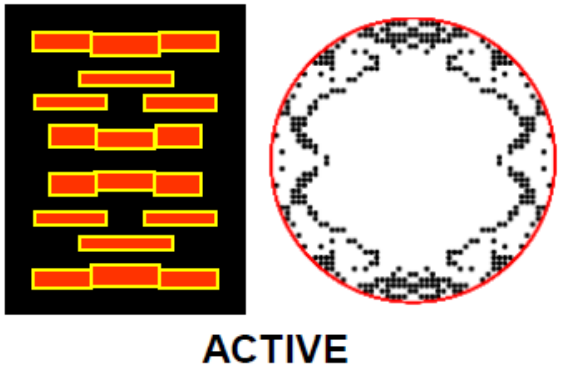


Effects of off-axis illumination

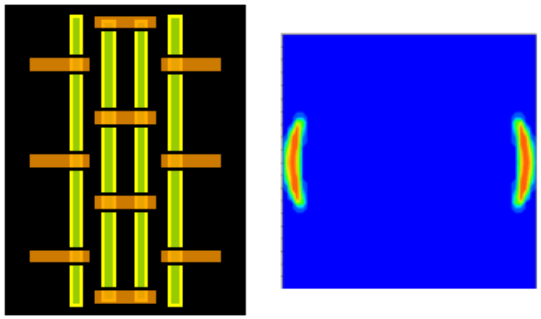


Optimizing sources for design layout pattern

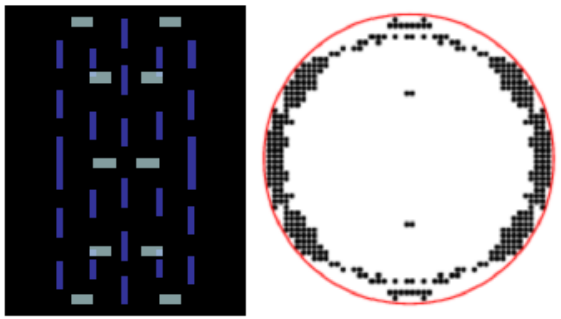




ACTIVE



GATE

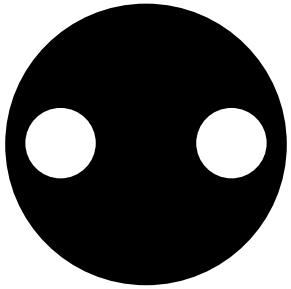


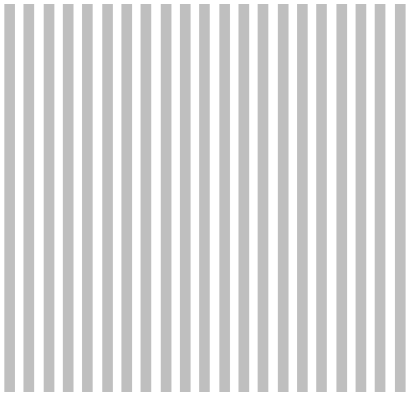
CONTACT

James Blatchford, TI, SPIE 2011

Cost of source optimization
Layout is restricted to pitches defined by the source

Dipole source

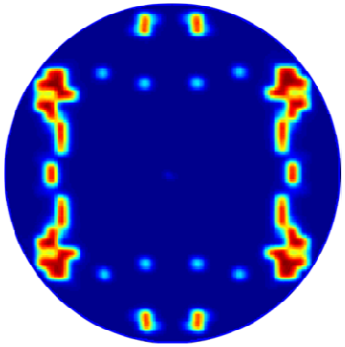




✓ Low noise for this pattern

X Can't resolve this pattern

Custom source



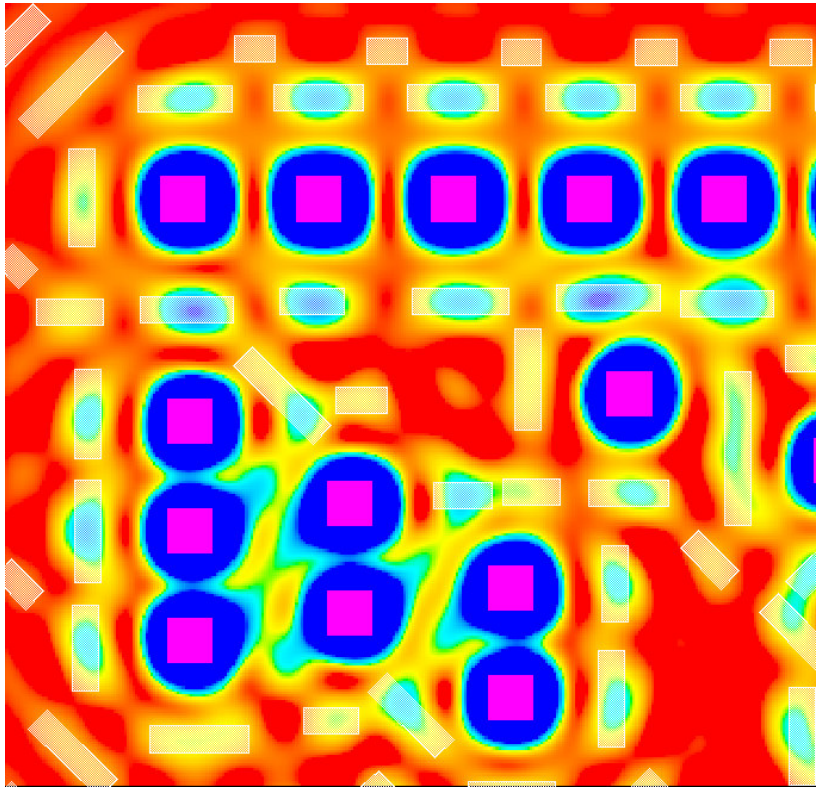
Physical noise sources are unaffected.

- A custom source makes layout patterns with certain spatial frequencies more immune to noise;
- But other layout configurations will be more susceptible.

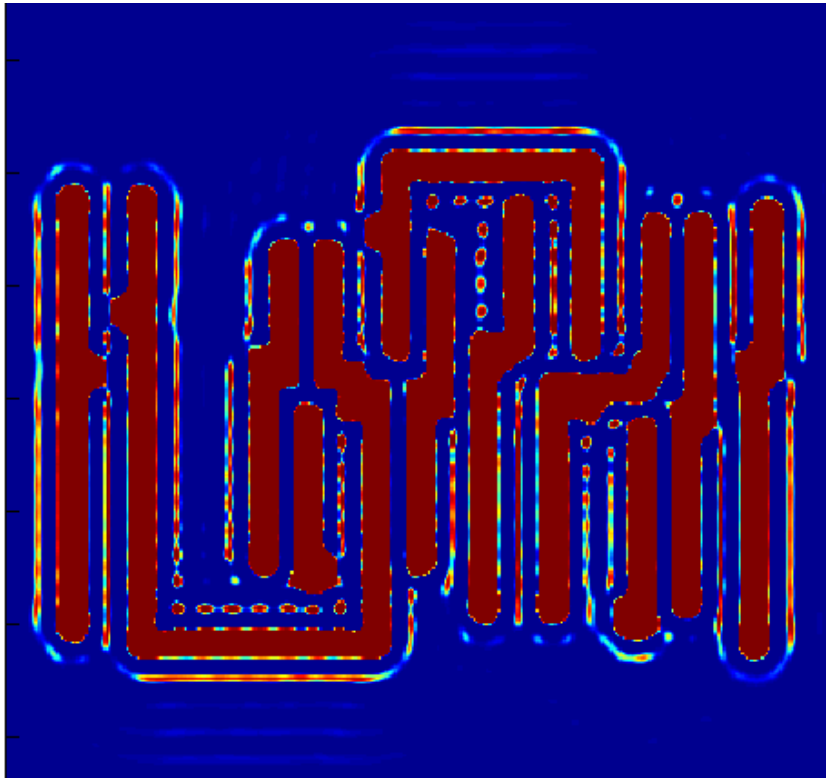
Design layouts must conform to spatial frequency constraints.

Mask optimization with subresolution assist features

Contacts

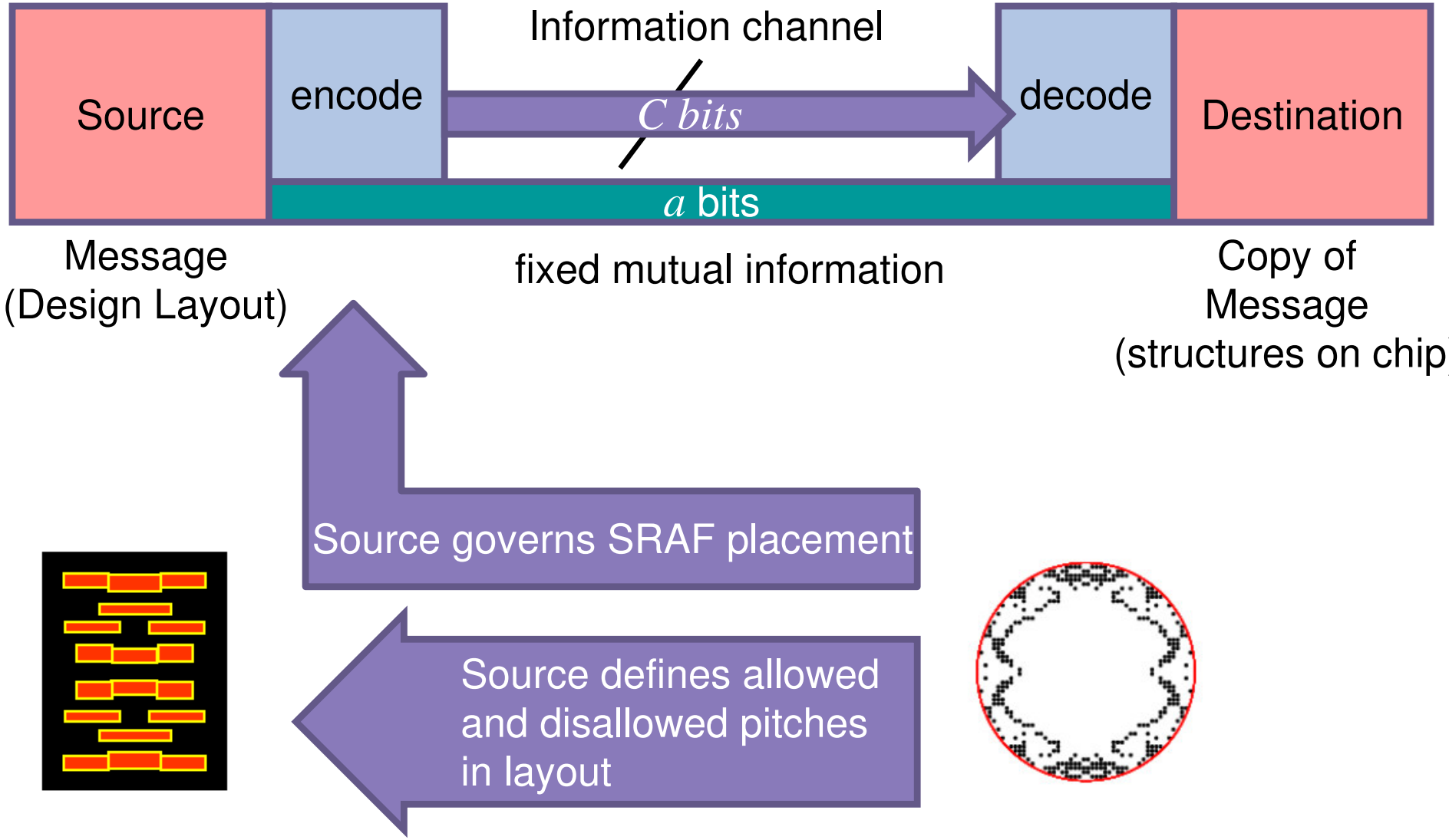


Lines



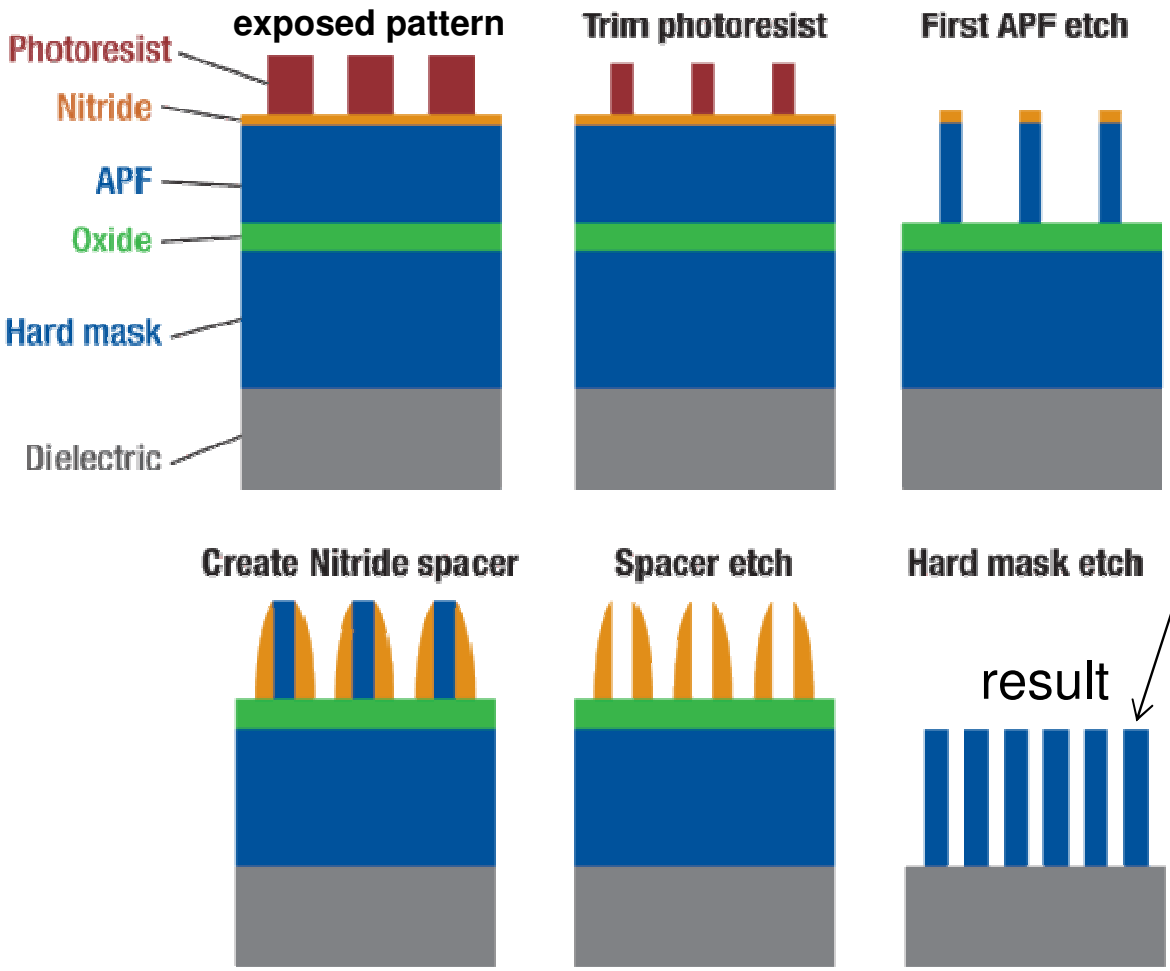
Assist features (SRAFs) generate spatial frequency components in the mask layout consistent with specific source configurations

Mutual information between design and process



Constant-width features defined by SAPD process

Sidewall-aligned pitch doubling (SAPD)

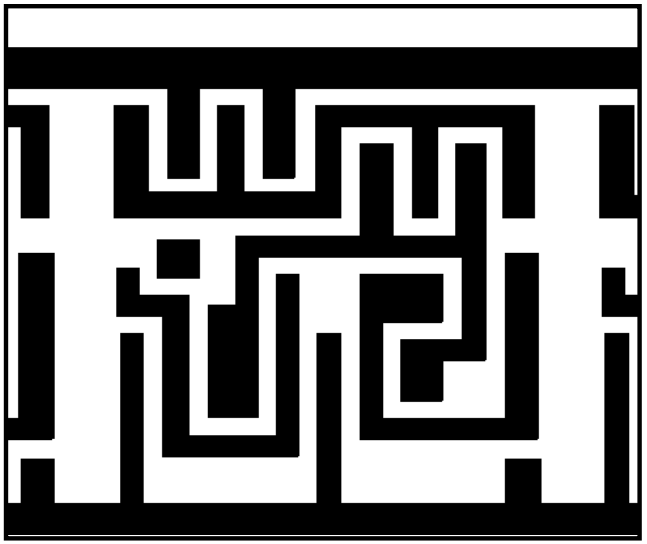


Width of printed structures is constant everywhere and determined by the process

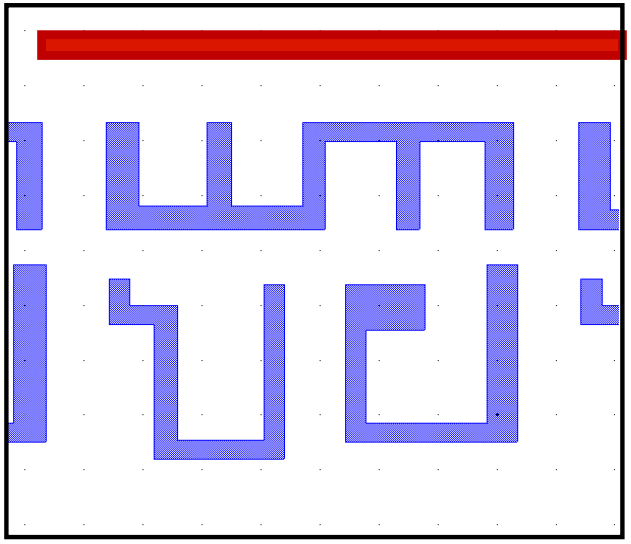
Spacer will form closed loops everywhere, and they must be “cut” with a second mask exposure and process step to form useful features.

SAPD for 2D layouts

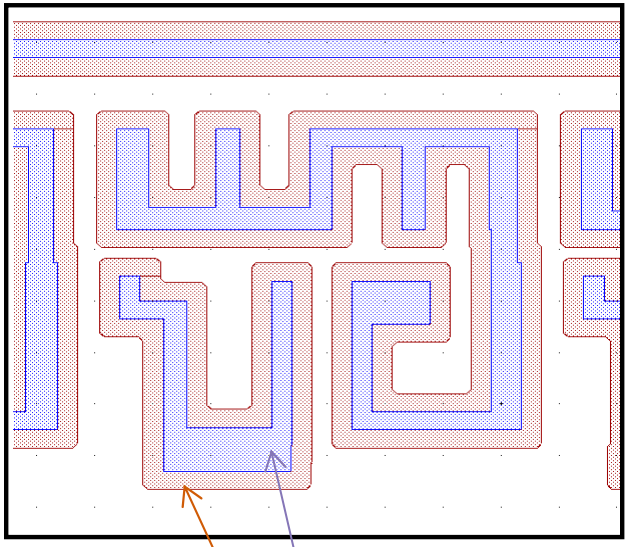
design



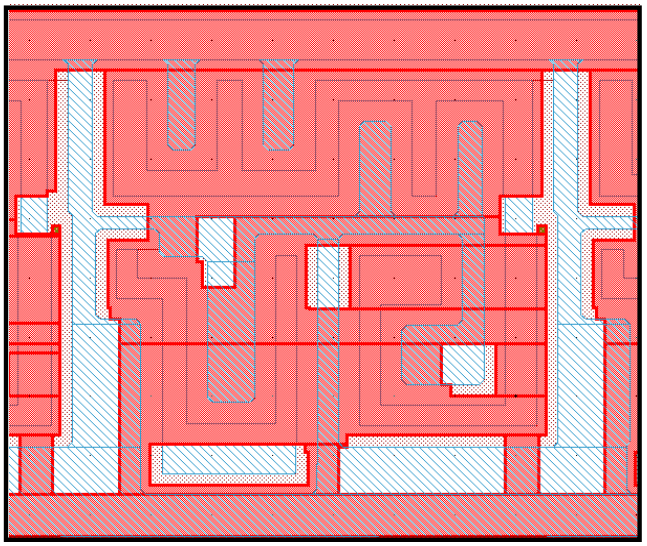
first exposure



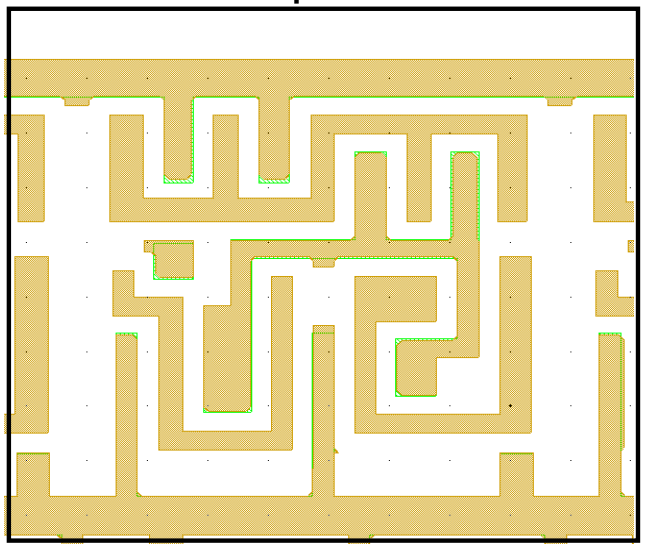
add sidewall features

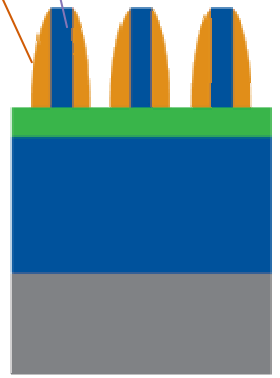


trim exposure



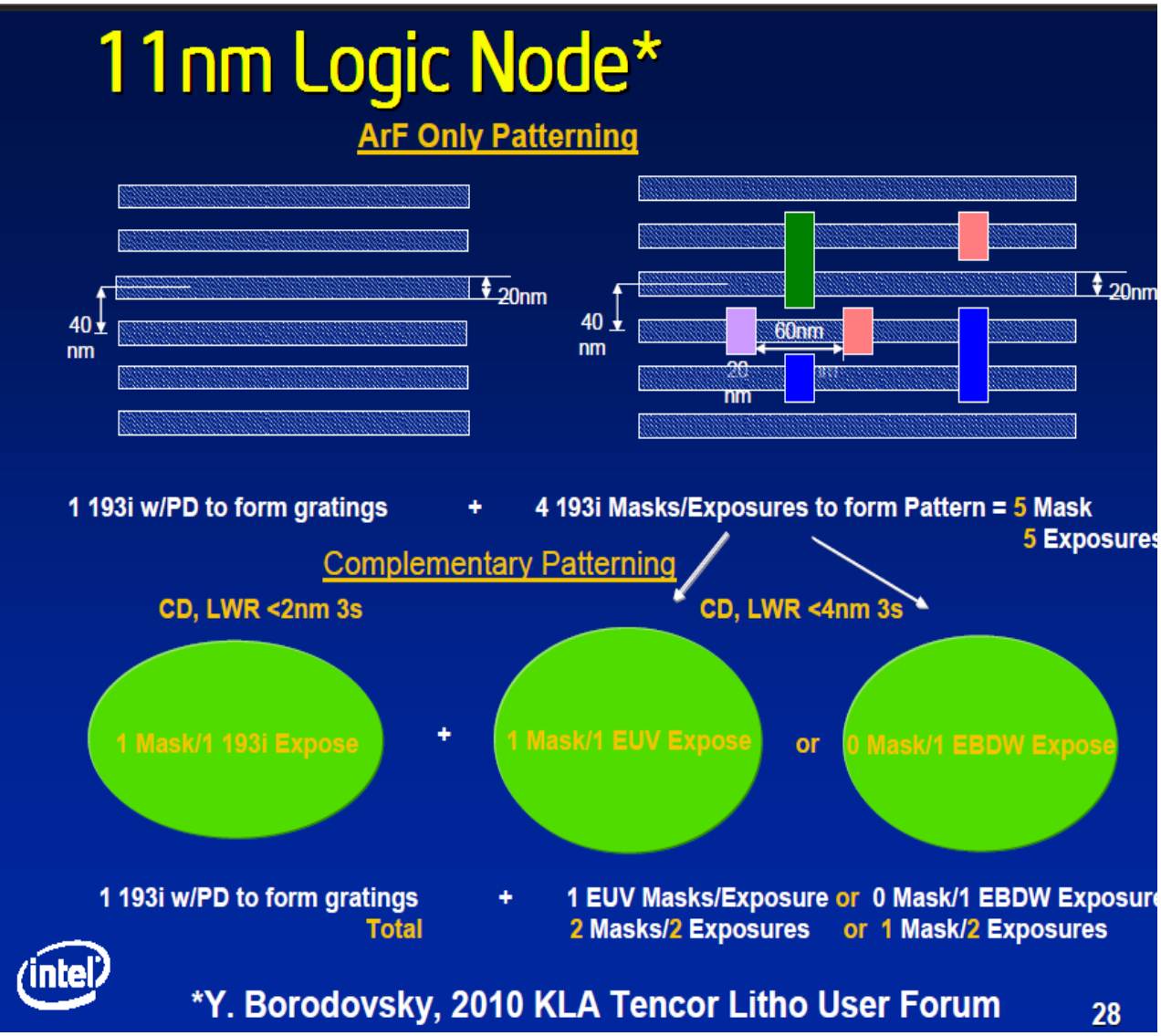
final pattern





Yongchan Ban, U. Texas, *et al,* SPIE 2011

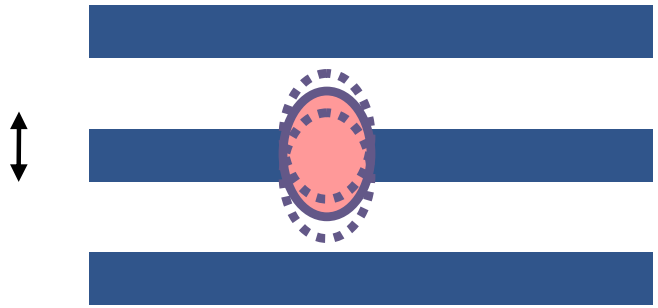
Complementary Patterning



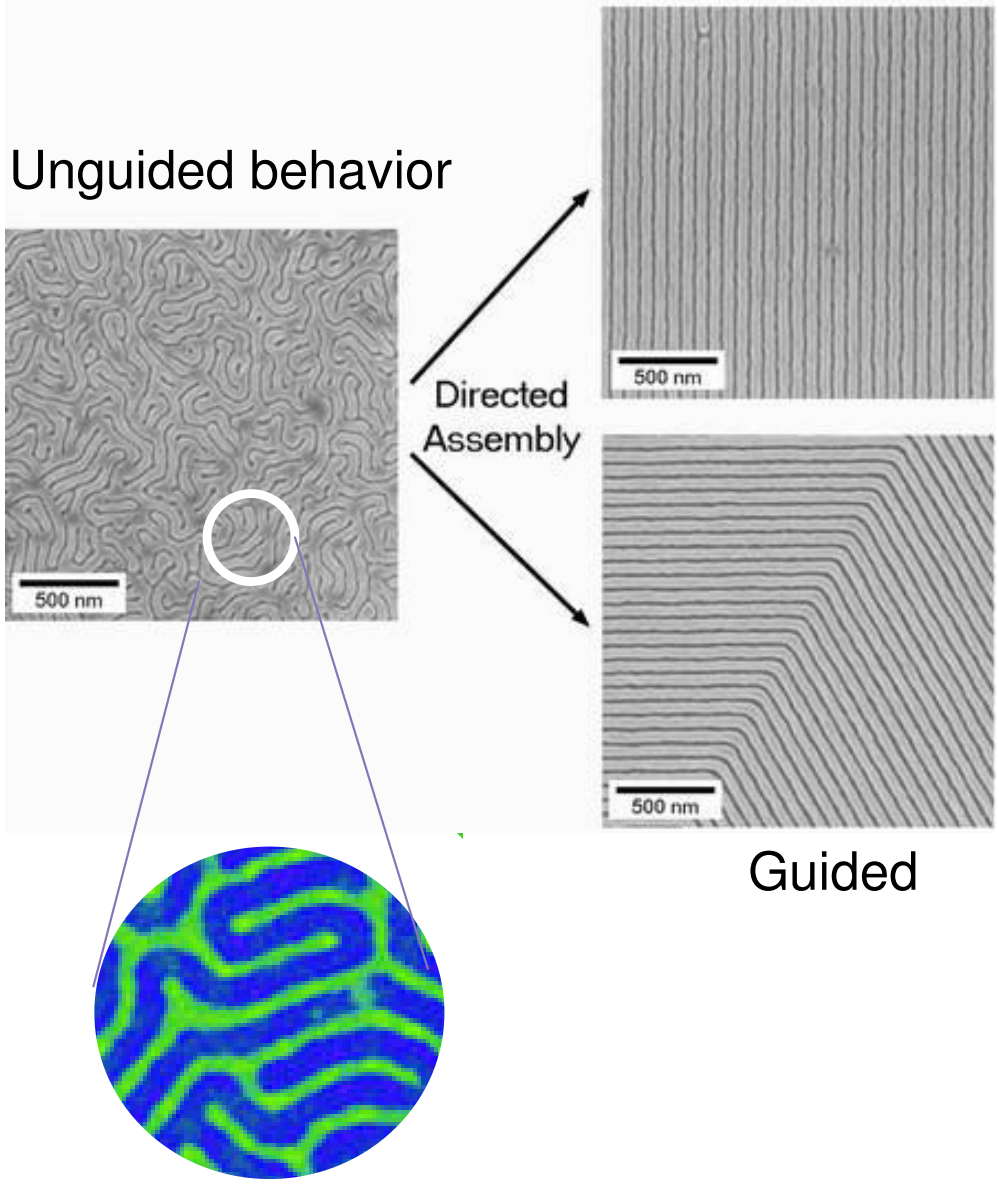
Grating pattern is **mutually known** to process and design.

Relevant information is the set of cut locations & sizes.

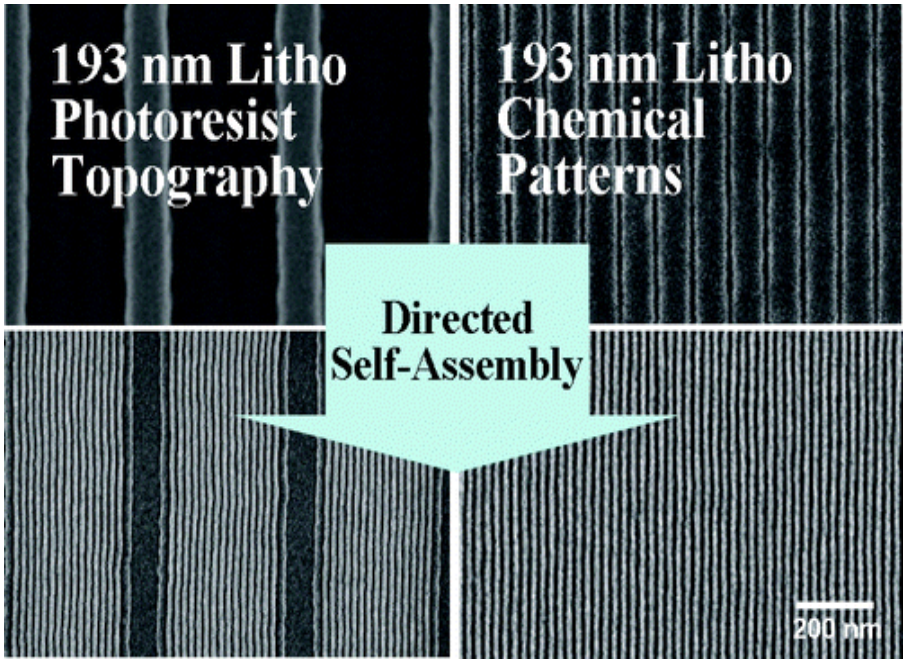
- Relatively sparse (low duty cycle)
- relaxed tolerance for placement uncertainty:



Directed self assembly (DSA) materials

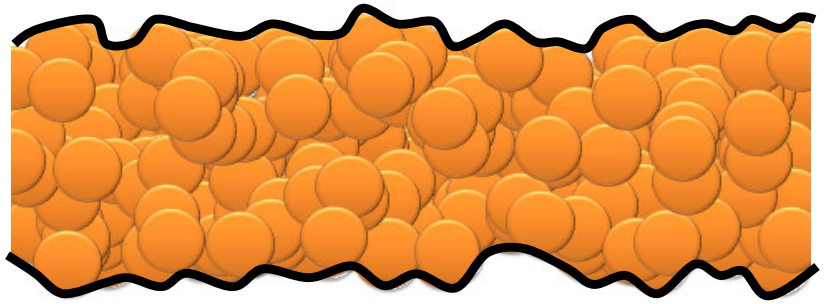


Density multiplication



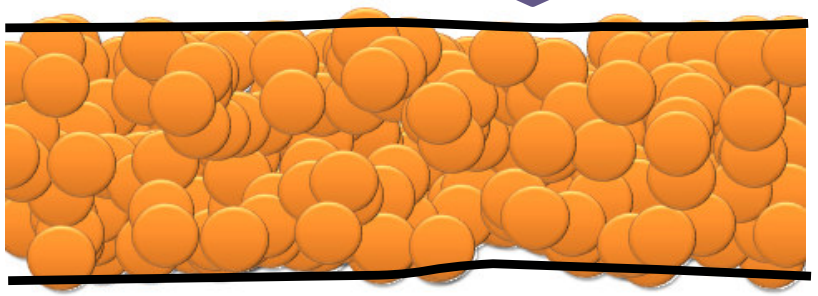
JSR, IBM, nextbigthing.com

Materials (hypothetical) solution to LER from shot noise

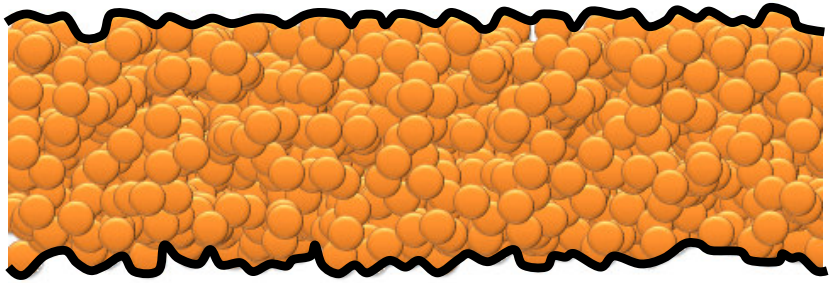


low photon density, high sensitivity

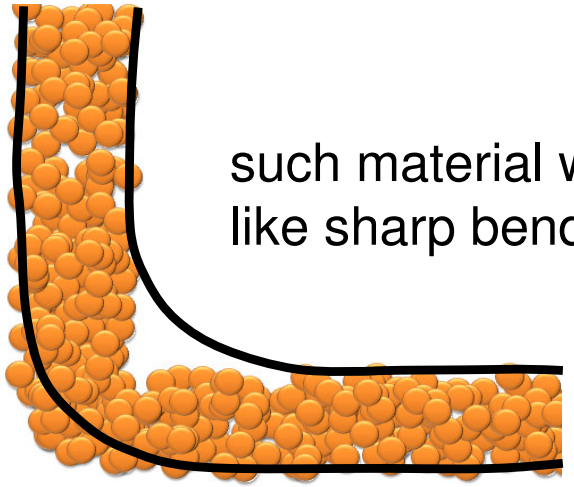
apply “stiff” directed material



increase photon density



high photon density, low sensitivity



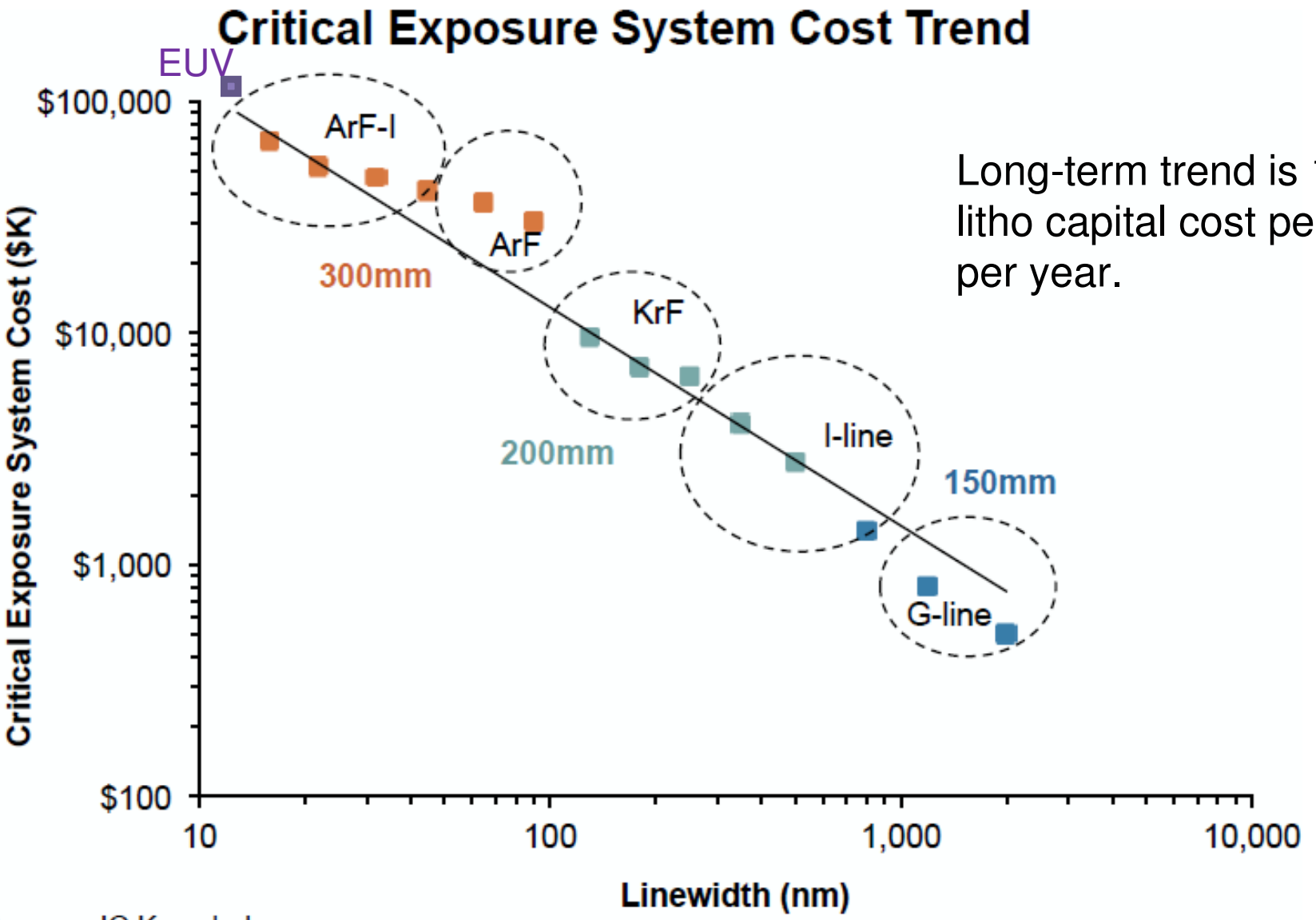
such material won’t like sharp bends

Productivity trends

	Cost reduction/yr.	Productivity increase/yr.
IC part cost per transistor, 30yr average[1]	-39%	
IC part cost per transistor, lately[2]	-10%	11%
Mask cost per transistor[3]	-11%	12%
Design cost per transistor[4]	-09%	10%
Design cost per transistor less embedded SW development cost[4]	-14%	16%
US long-term, annual productivity improvement[5]		3%

[1]R. Kurtzweil, 2008
[2]IBS Vol 18 # 5, 2009
[3]IC Insights
[4]IBS Vol 18 #7, 2009
[5]Crestmont Research, 2010

Lithography tool cost

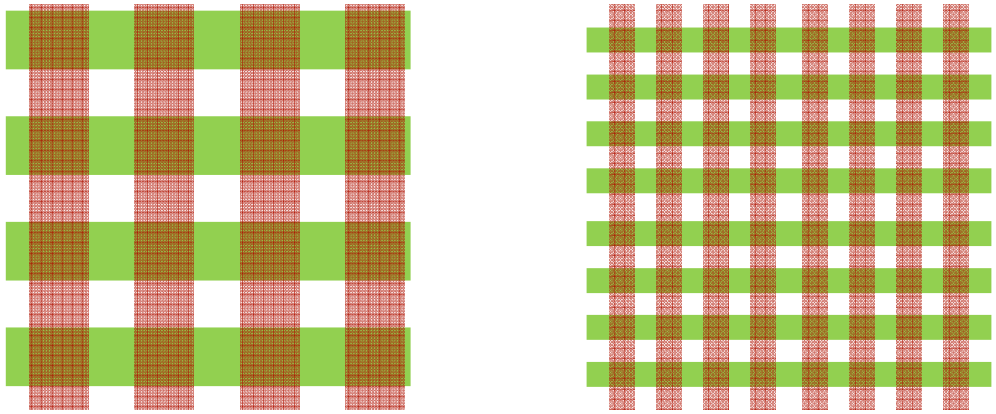


Long-term trend is 18% reduction in litho capital cost per transistor, per year.

Source: IC Knowledge

Observations

- EUV promises nearly an 7X increase in information density compared to 193i (1240 vs. 178 Mbytes/mm^2) -- nearly a 3-generation shrink .
  - Very good for 2-D configurations, such as contacts, trim/cut patterns.
- On a single layer, double patterning (pitch splitting and pitch doubling) doubles density, thus there is no net productivity gain (cost /feature same as single exposure).
  - At least DP does not increase cost per device.
- Double-patterning provides a 2-generation shrink (50%) for 1-dimensional layouts; interactions between DP'd layers can provide device density increase up to 4X.



Conclusions

- When design information exceeds available channel capacity, the litho process must lower entropy by limiting choices.
  - The missing information is provided by having more order (spatial structure) in the process, which must be accommodated in design layout constraints.
- Materials & process will be playing an increasing role in “more Moore.”
  - Enable resolution and density.
  - Reduce cost.
- Restricted pitches (spatial frequencies) are becoming a dominant layout constraint.
  - highly regular, repeating patterns are best.
- Regular 1-D layouts provide compelling manufacturing benefits:
  - Low entropy maximizes optical image fidelity.
  - Defines realistic targets for self-assembling process technologies.
  - Maximizes the effectiveness of double patterning.

Acknowledgements

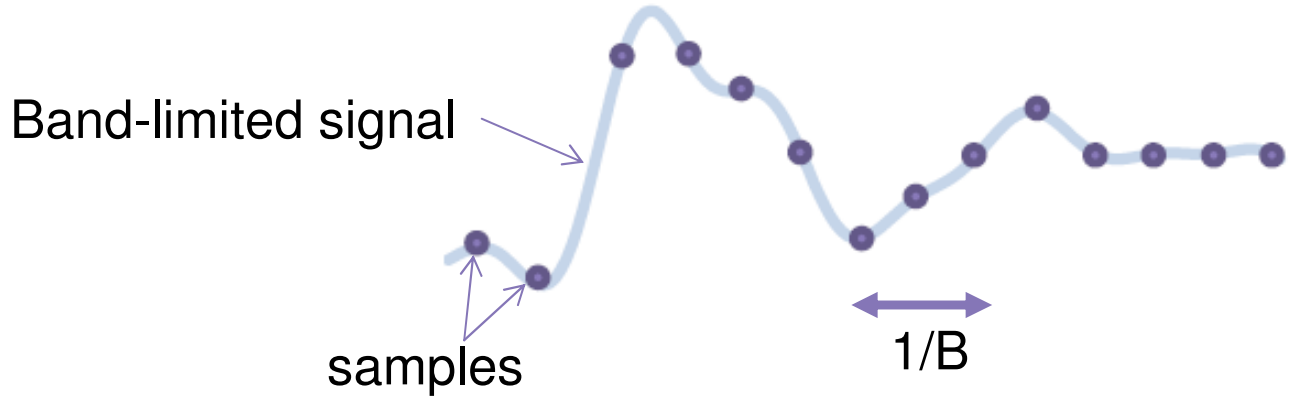
- John Stirniman, Lars Bomholt, Kevin Lucas, Thomas Schmoeller, Bob Lefferts.

Thank you

Appendix and backup

Review: Nyquist sampling theorem

A signal containing no frequencies higher than B can be exactly reconstructed from a series of samples spaced by ½ the period of B.



Reconstruction function convolved with samples

Harry Nyquist, *Certain Topics in Telegraph Transmission Theory*, 1928

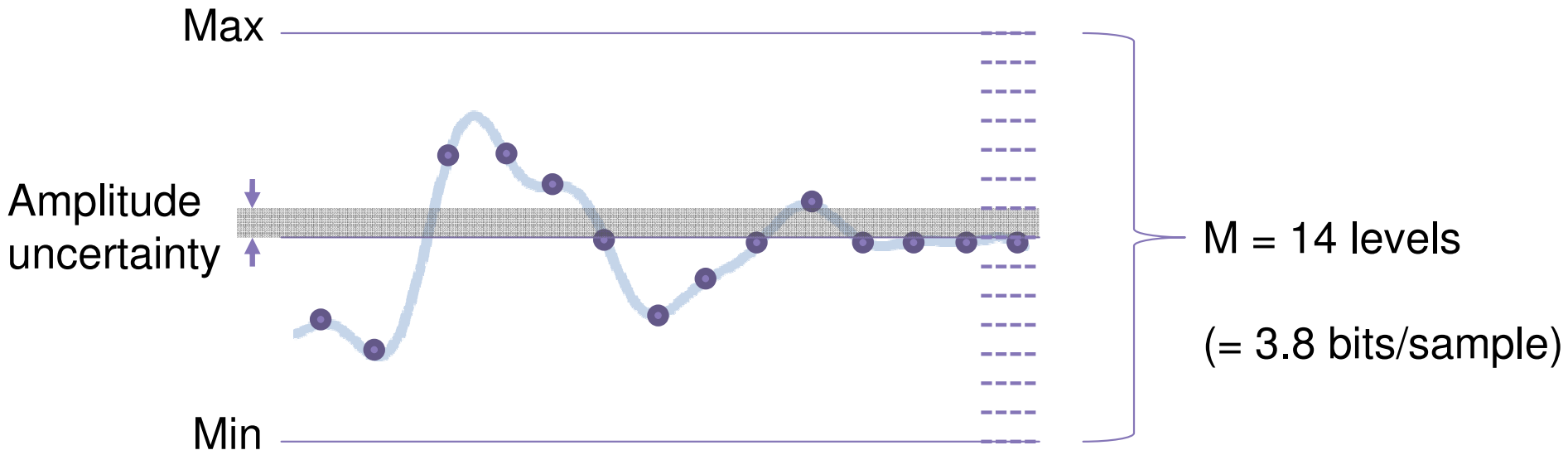
Review: Hartley's Law

Hartley's Law extends Nyquist to express the information capacity of a channel in terms of bits/second, R.

$$R <= 2B \log_2(M_H)$$

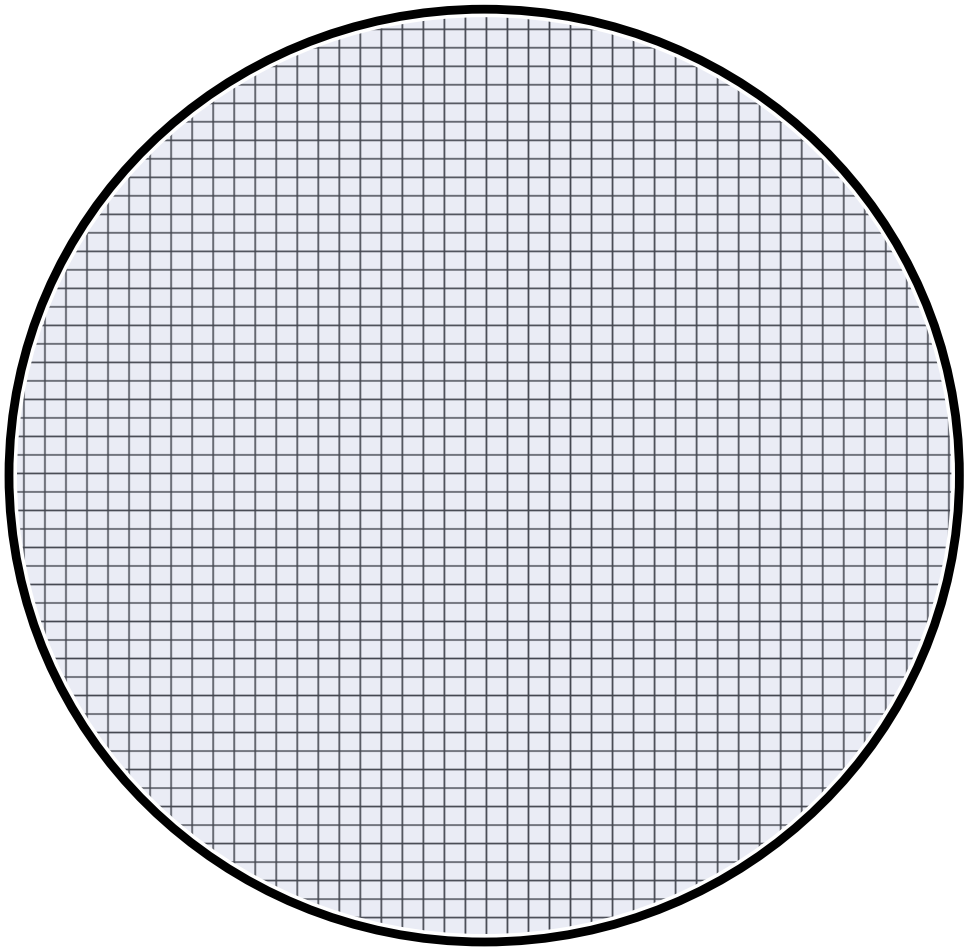
Where M_H is the number of distinguishable levels per sample.

Example:



Ralph Hartley, *Transmission of Information*, 1928

Calculating information density of litho optics



x,y sample spacing = $k_1 \frac{\lambda}{NA}$

$$R <= 2B \log_2(M_H)$$

Square the Nyquist sample rate in Hartley's Law, and replace Hz with:

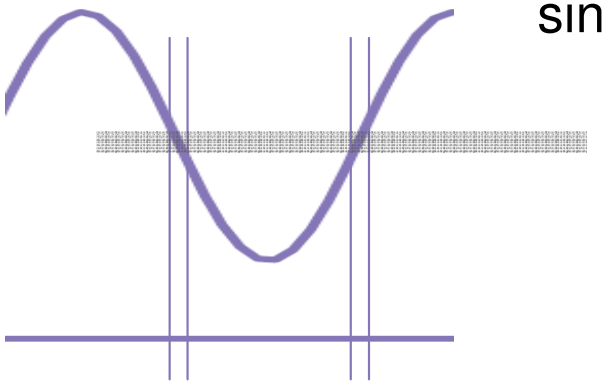
$$\frac{NA}{2k_1\lambda}$$

$$R \leq \left(\frac{NA}{k_1\lambda}\right)^2 \log_2(M) \text{ bits/m}^2$$

Note that R is information density (not information within the circle)

Estimating M_H

- Determining M_H
  - Meeting +/-10% CD spec at minimum ½ pitch @ contrast = 0.5 is (roughly) equivalent to an amplitude uncertainty of **1:25**



sinusoidal image signal at minimum pitch

~ amplitude uncertainty ~4% of peak

+/-5% each edge

Optical information density calculations

Optical density equation:

$$C = \left[\frac{NA}{k_1 \lambda}\right]^2 log_2(M_H)\ bits/m^2$$

ArF 193 immersion scanner:

$$\left[\frac{1.35}{0.4 \cdot 193nm}\right]^2 log_2(25) \frac{bits}{m^2} = 178\ MBytes/mm^2$$

EUV 1st generation scanner:

$$\left[\frac{0.25}{0.4 \cdot 13.5nm}\right]^2 log_2(25) \frac{bits}{m^2} = 1240\ MBytes/mm^2$$