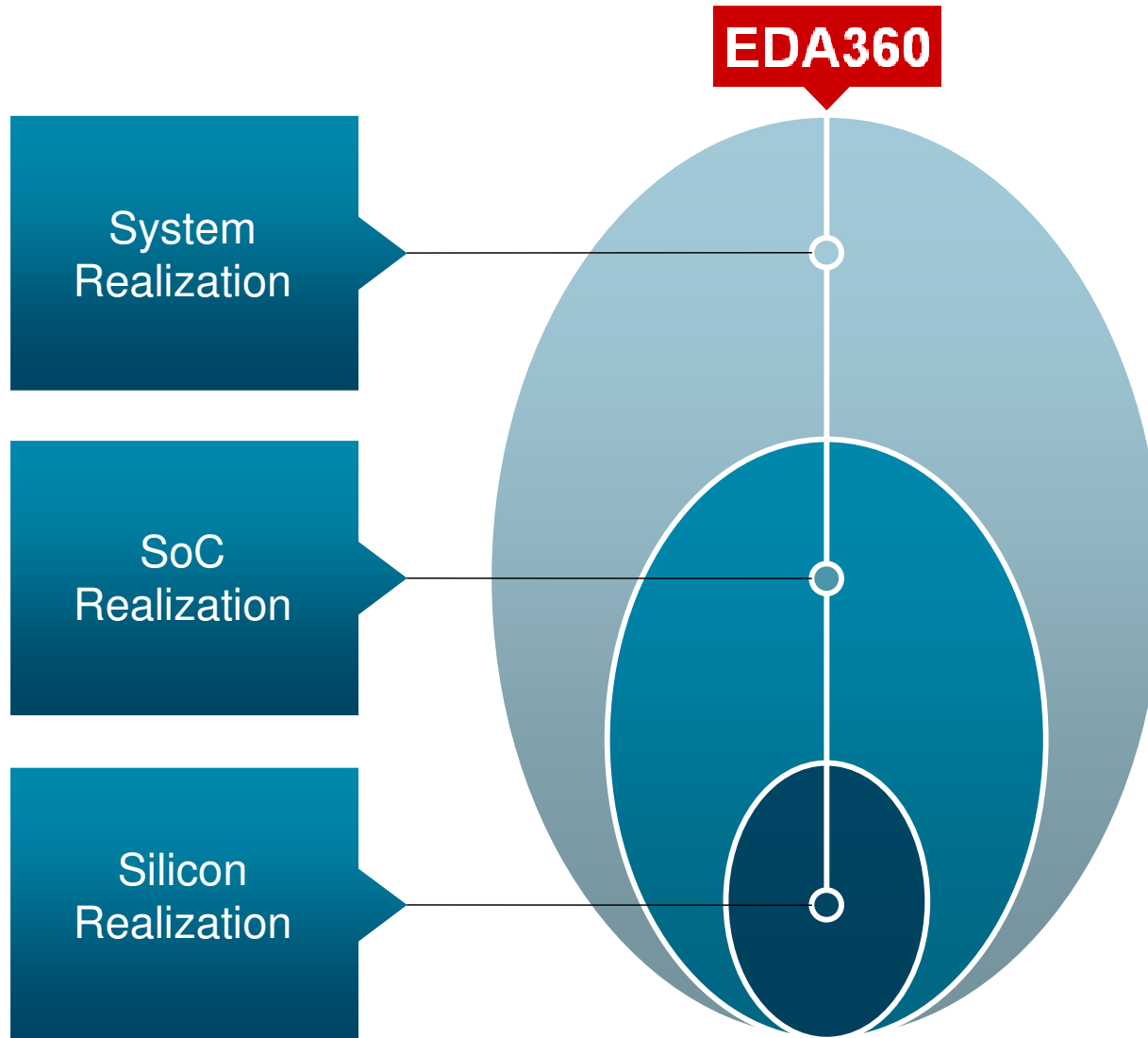


EDA360 - Is End-to-End Design a Riddle, a Rebus, or a Reality?

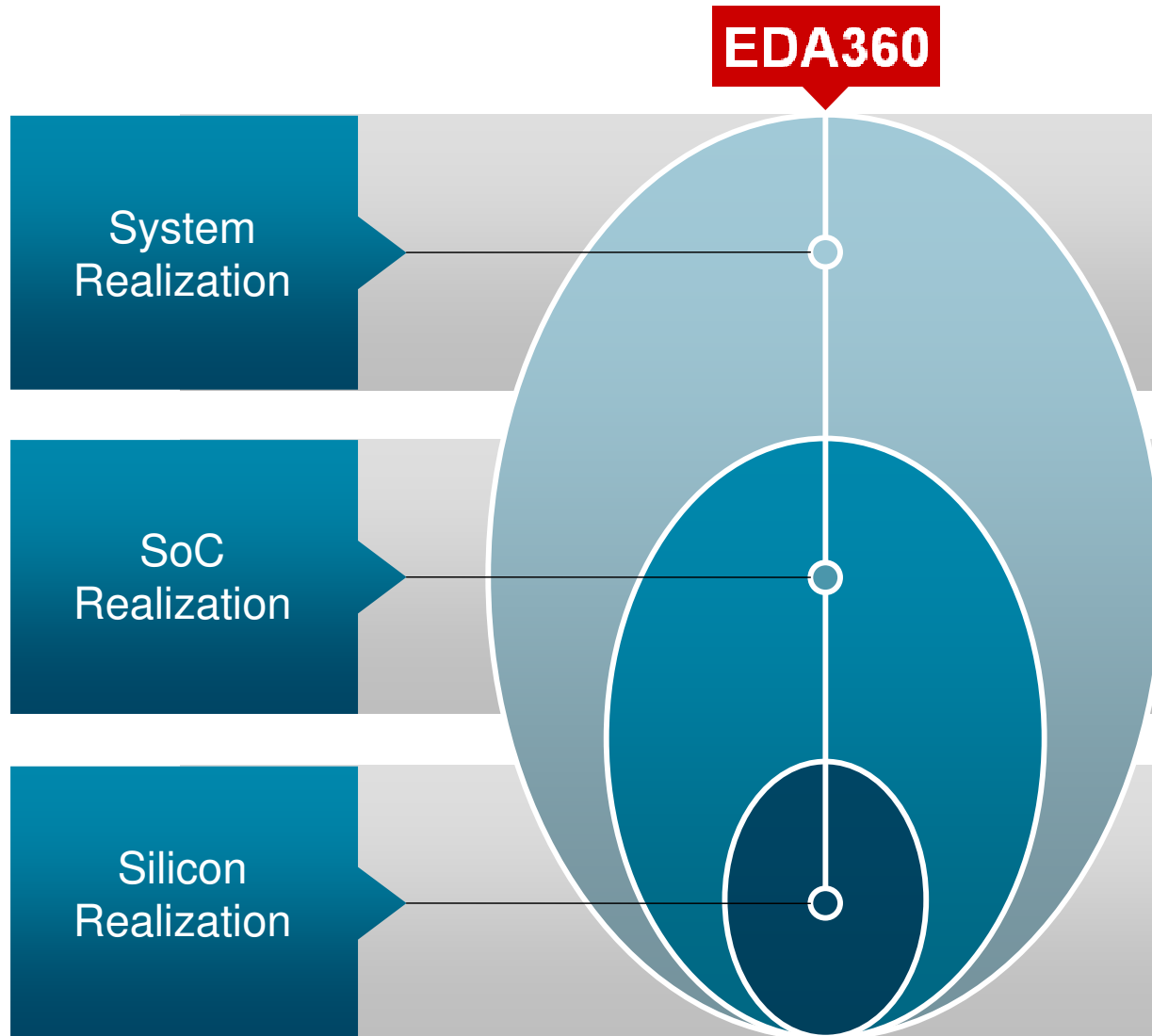
April 7, 2011



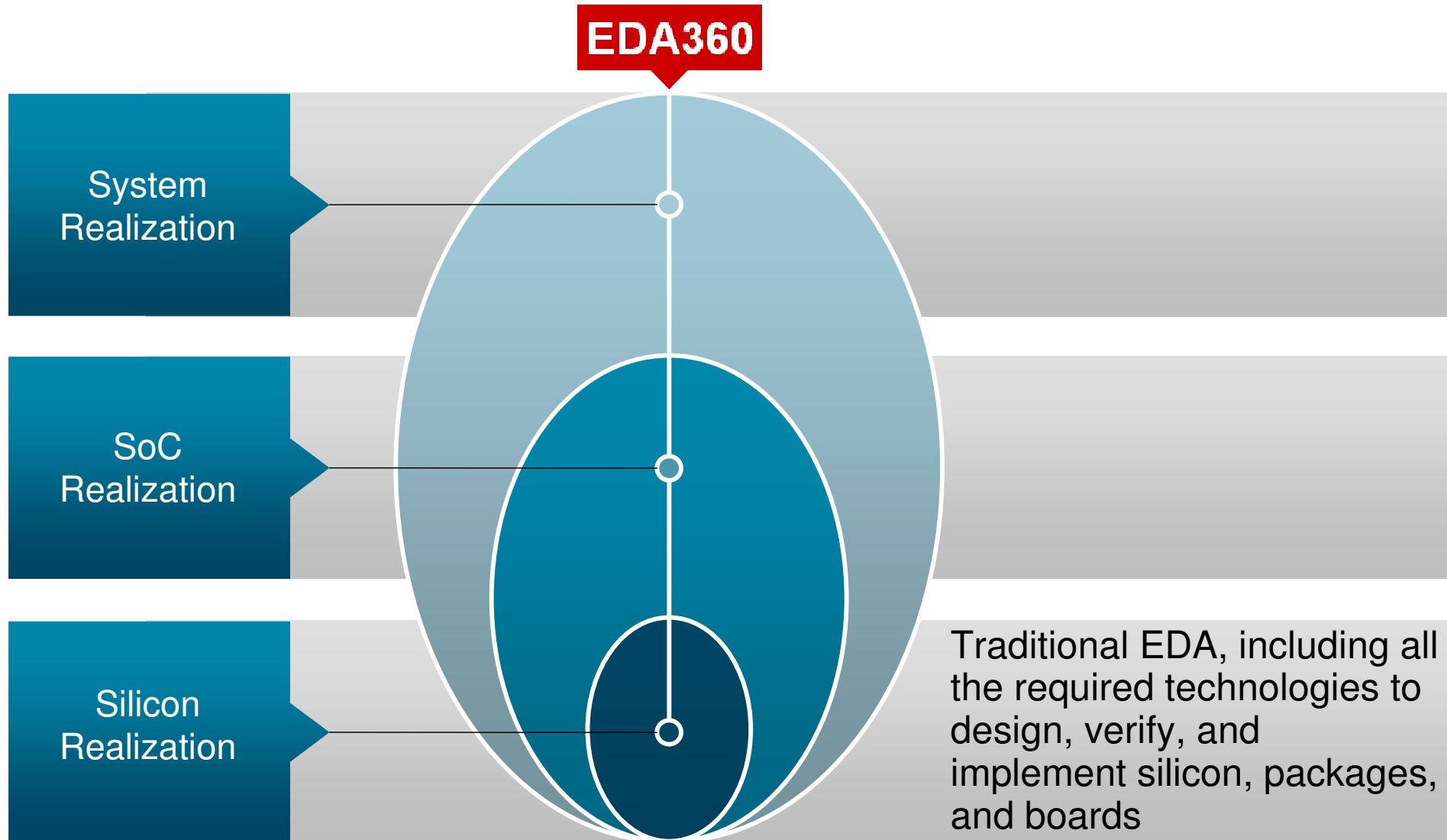
Three Key Pillars of EDA360



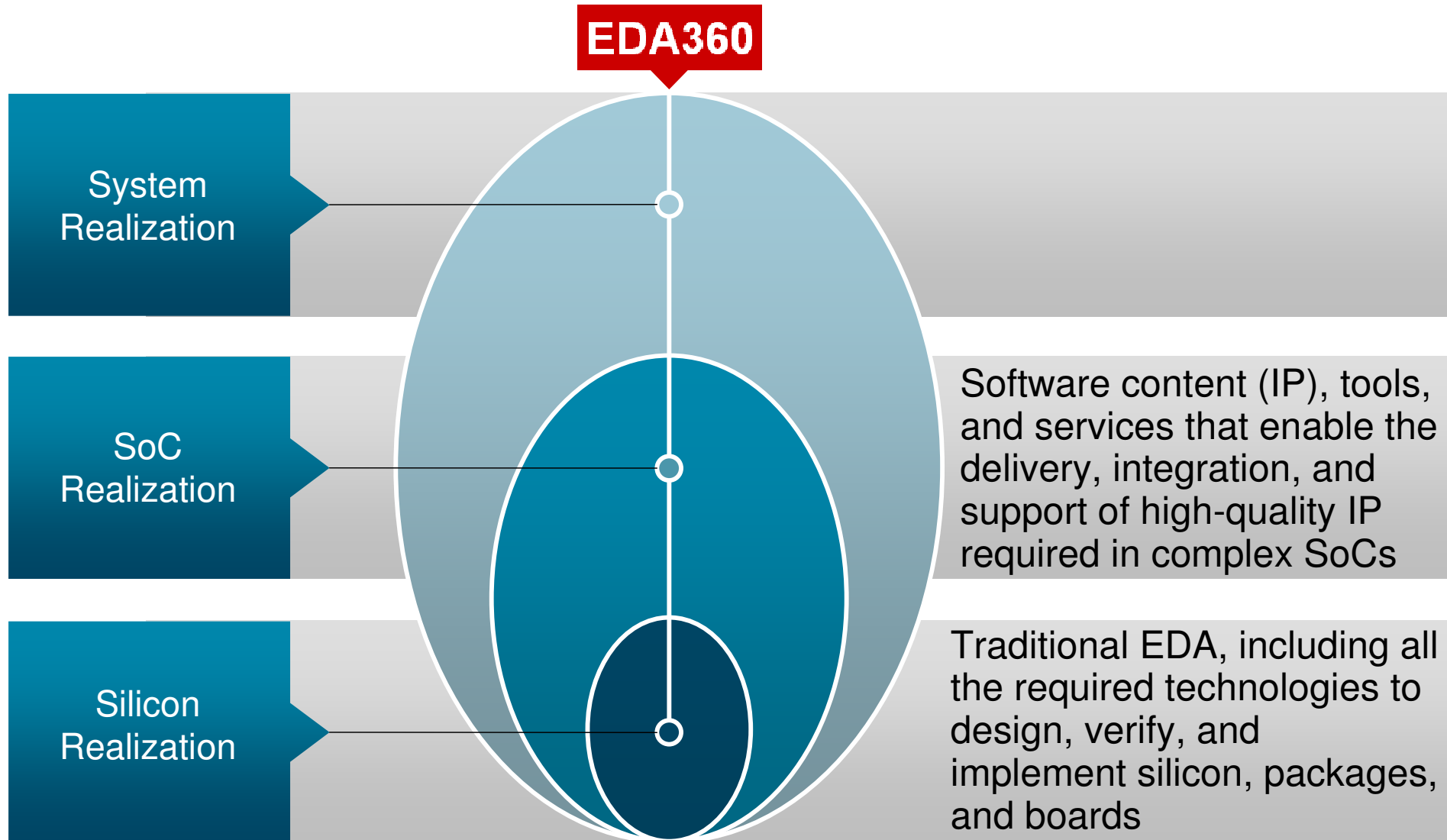
Three Key Pillars of EDA360



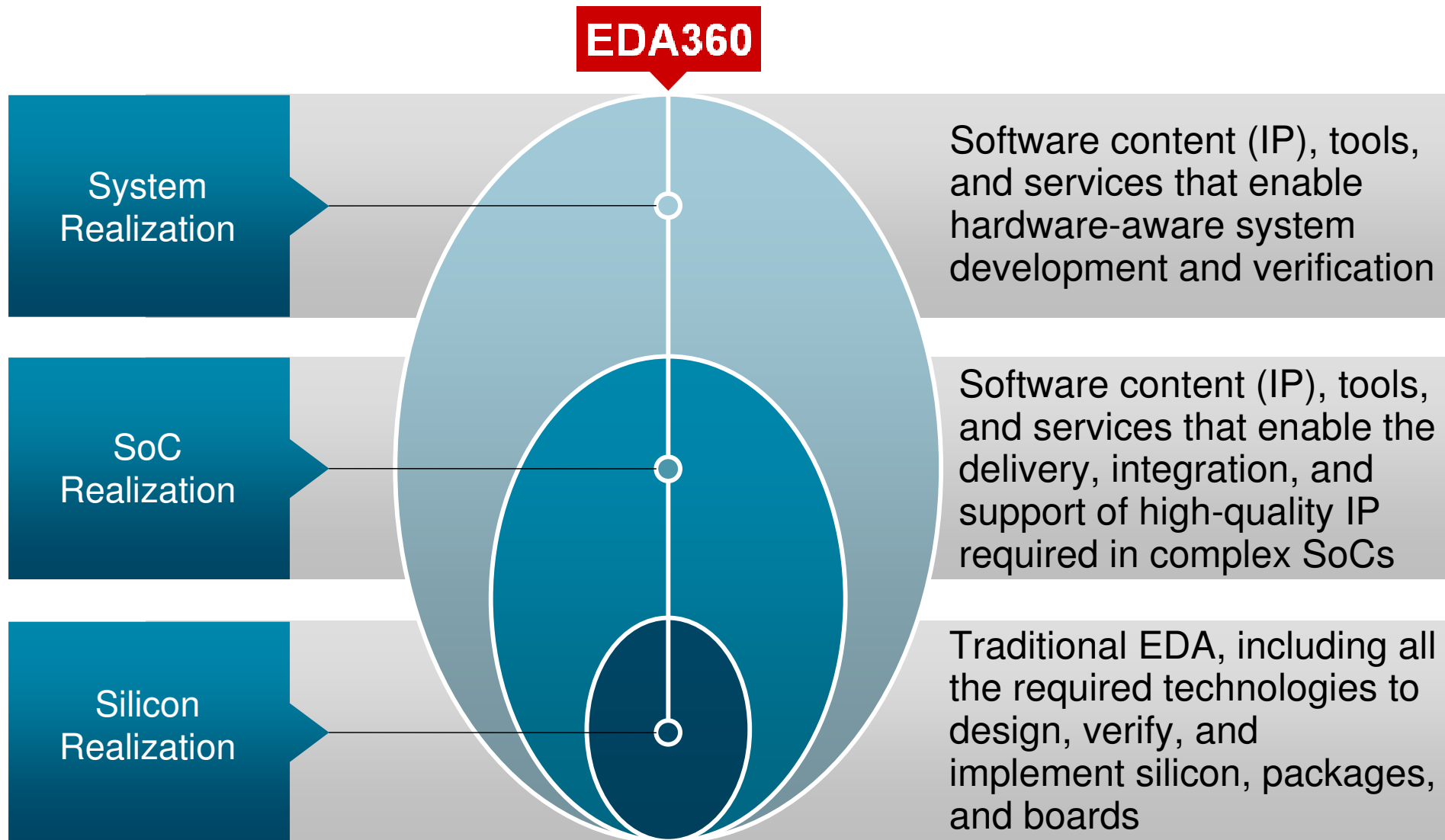
Three Key Pillars of EDA360



Three Key Pillars of EDA360

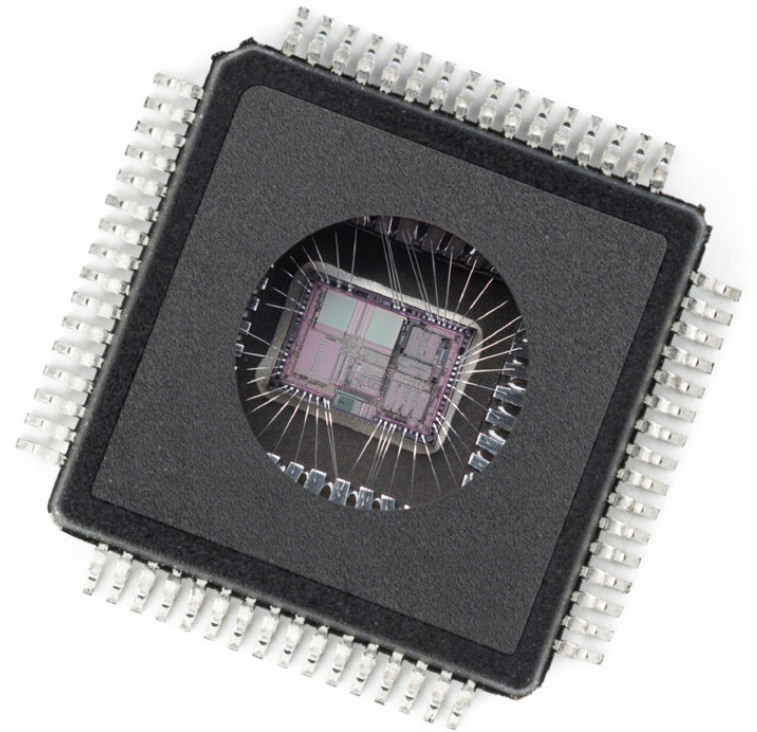



Three Key Pillars of EDA360



Silicon Realization – Customer Challenges

- Time to market
 - Disaggregated, global design chain limits visibility and predictability for complex designs – causing schedule delays and respins
 - Lack of true holistic and integrated silicon-package-board flows causes productivity gap
 - Reuse
- Profitability
 - Design failure catastrophic
 - Functionality, performance, and power improvements contribute to higher margins
 - Manufacturability



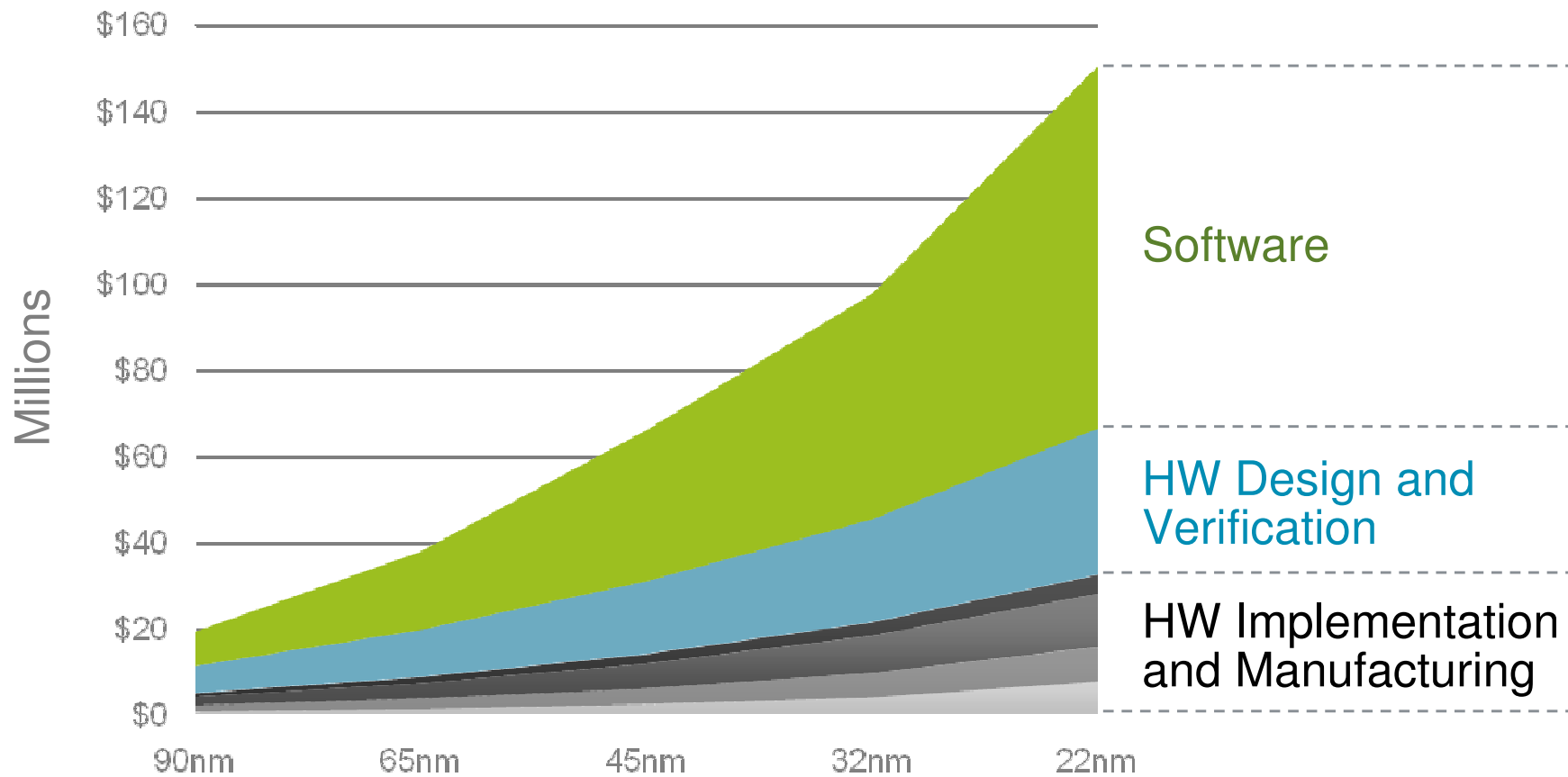


System Realization – Customer Challenges

- Software development trails hardware development, impacting time-to-market
- Hardware-software integration complexity impeding product shipments, quality
- Effective and predictable system and sub-system verification

System Realization – Market Landscape

Development costs rising

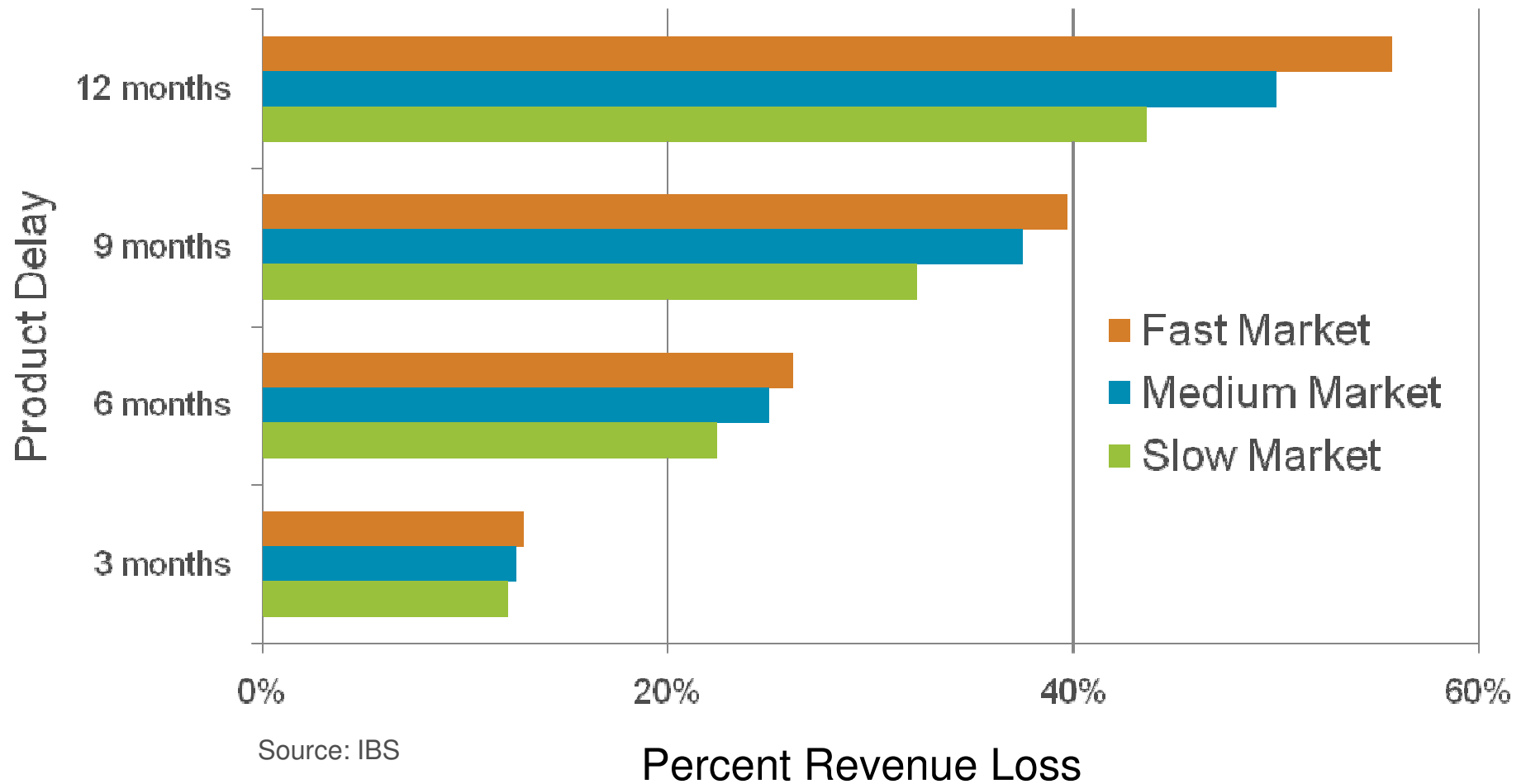


Source: IBS 2009

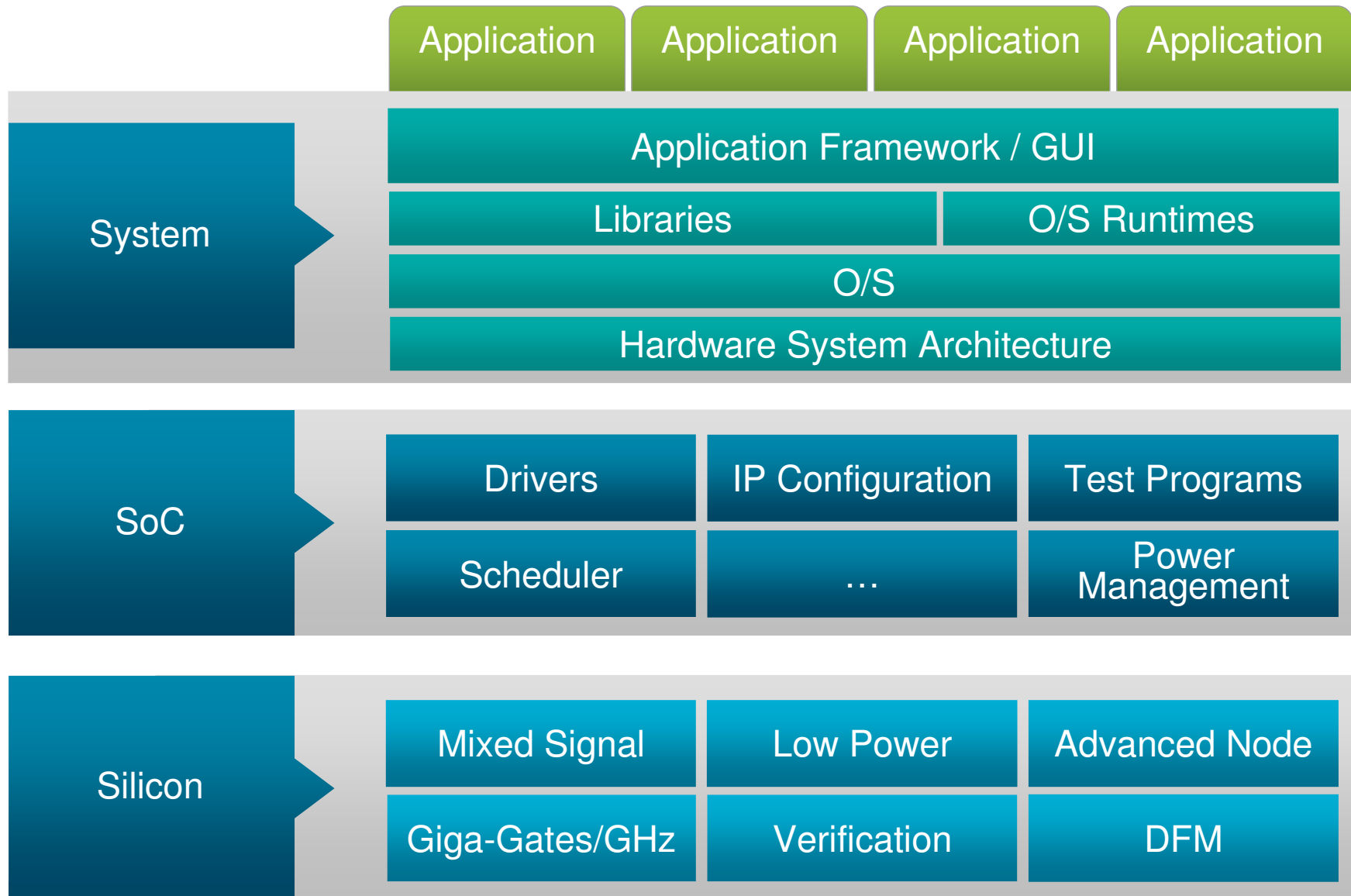
System Realization – Market Landscape

Market window shrinking; growing penalties for delay

IC Revenue Loss Due to Product Delay



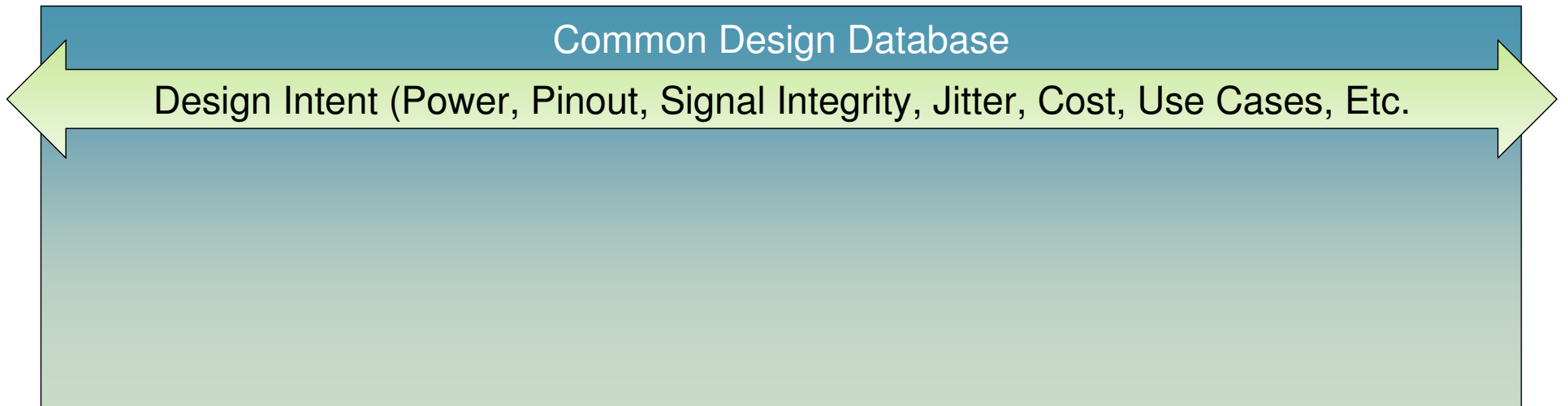
Sample Challenges at Each Realization Layer



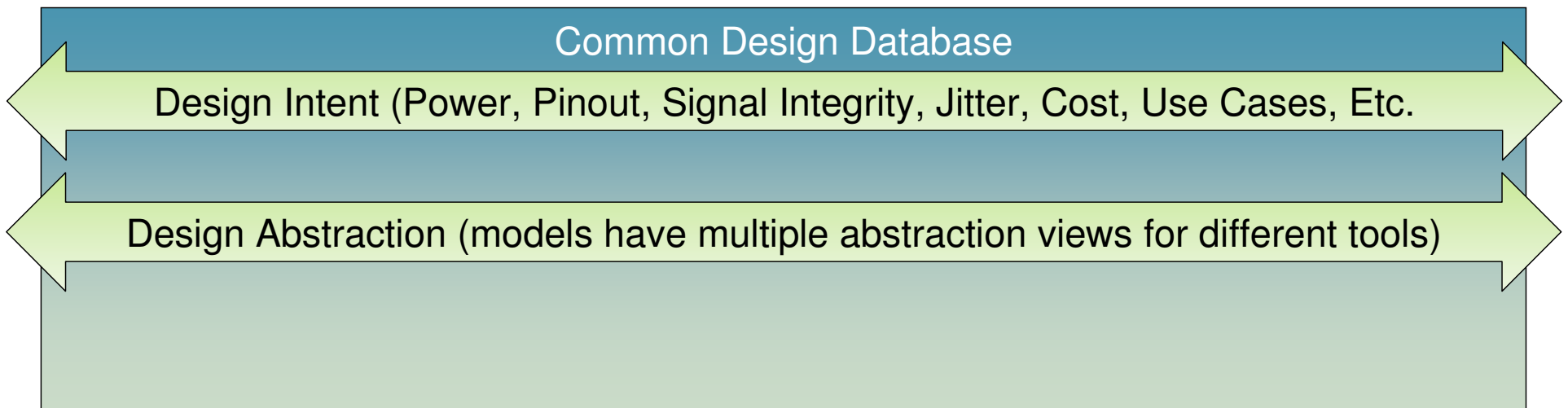
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Common Design Database

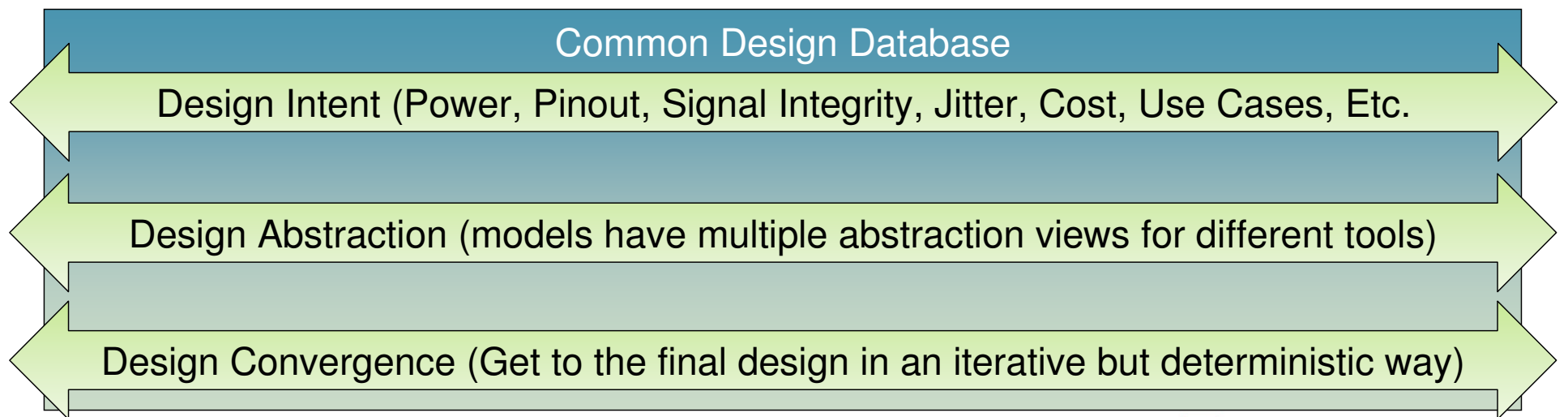
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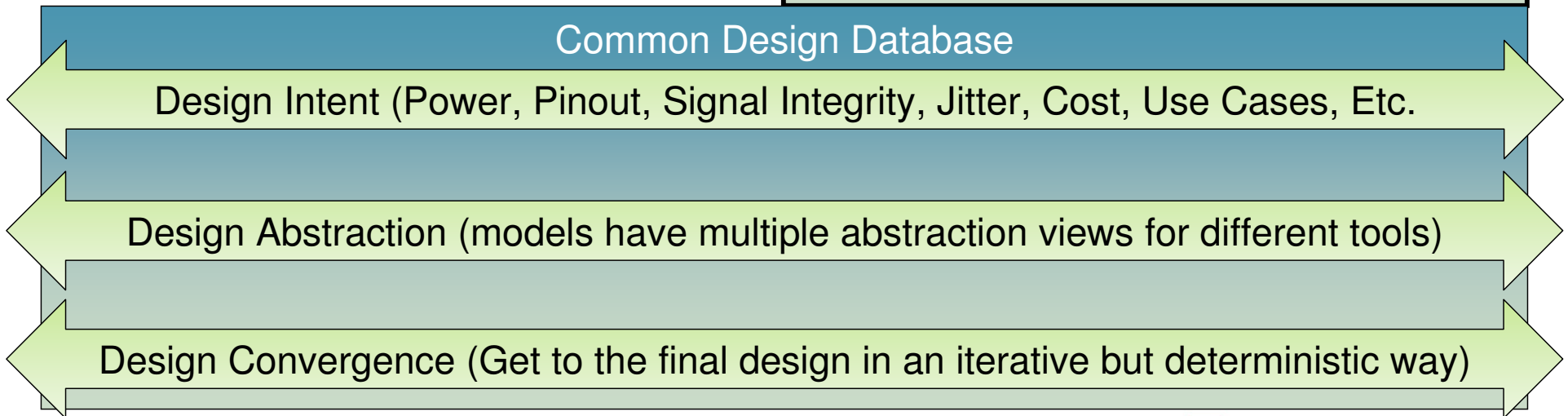
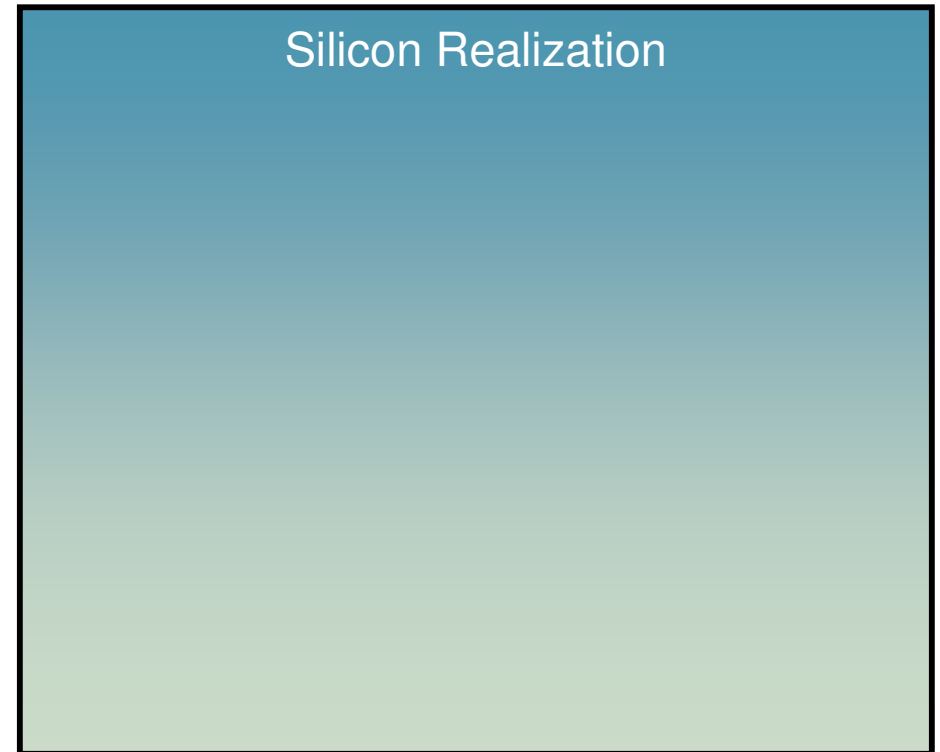
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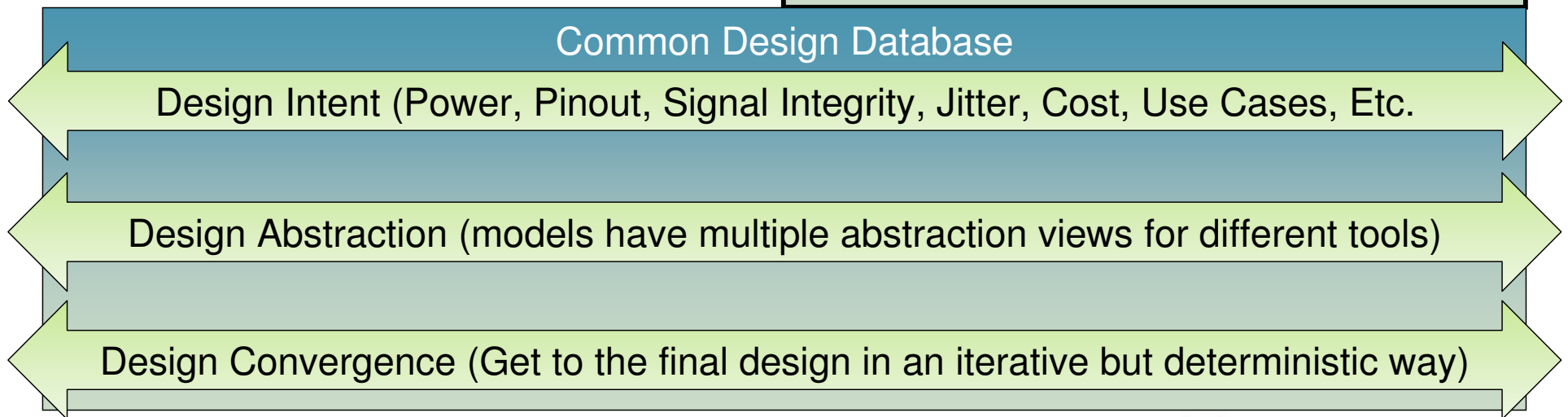
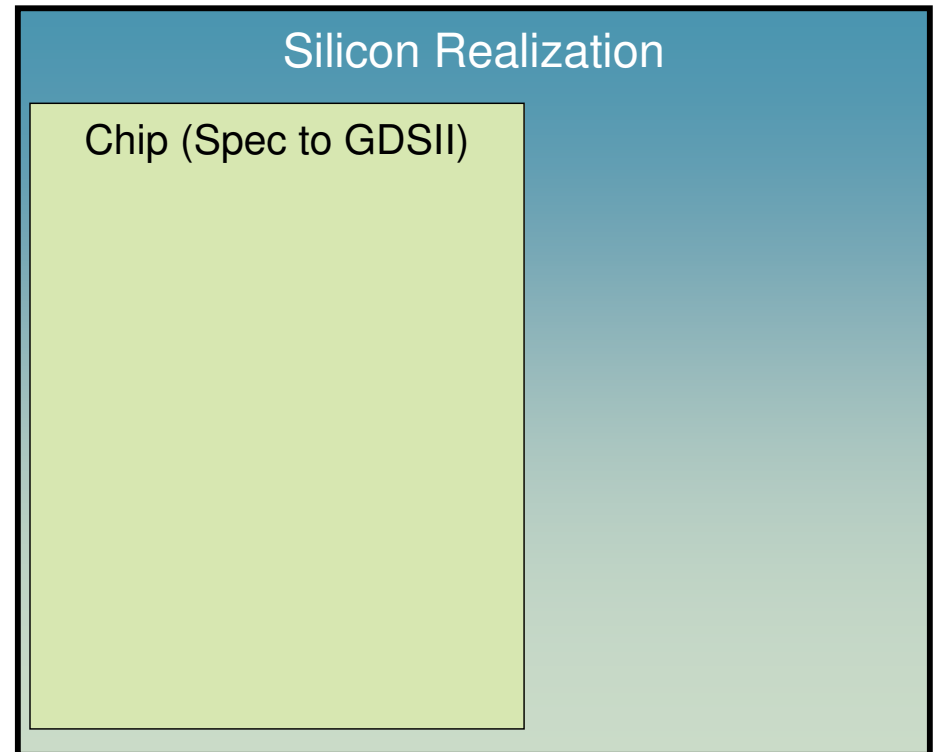
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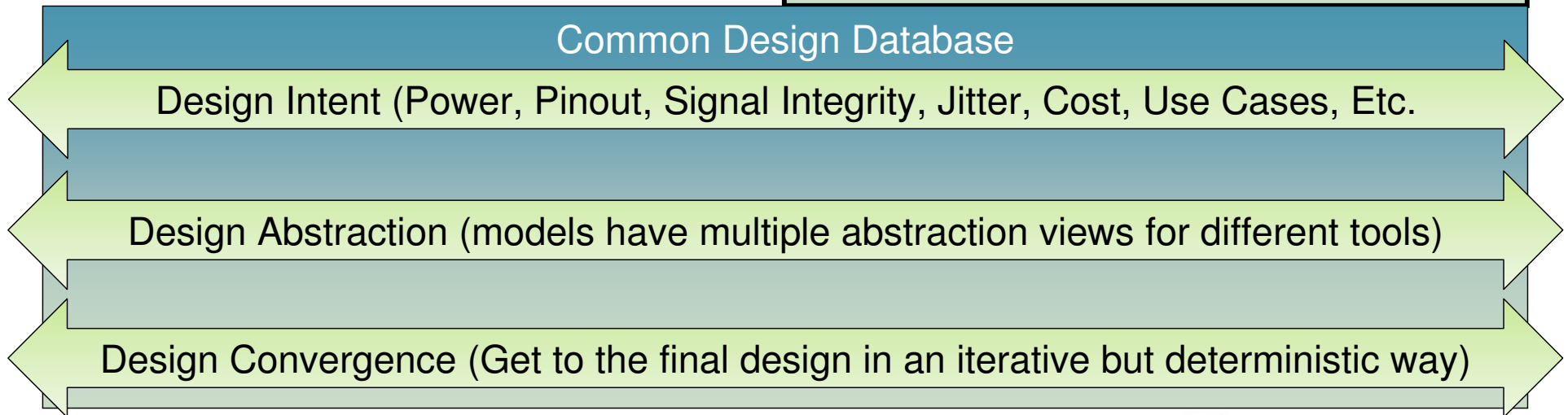
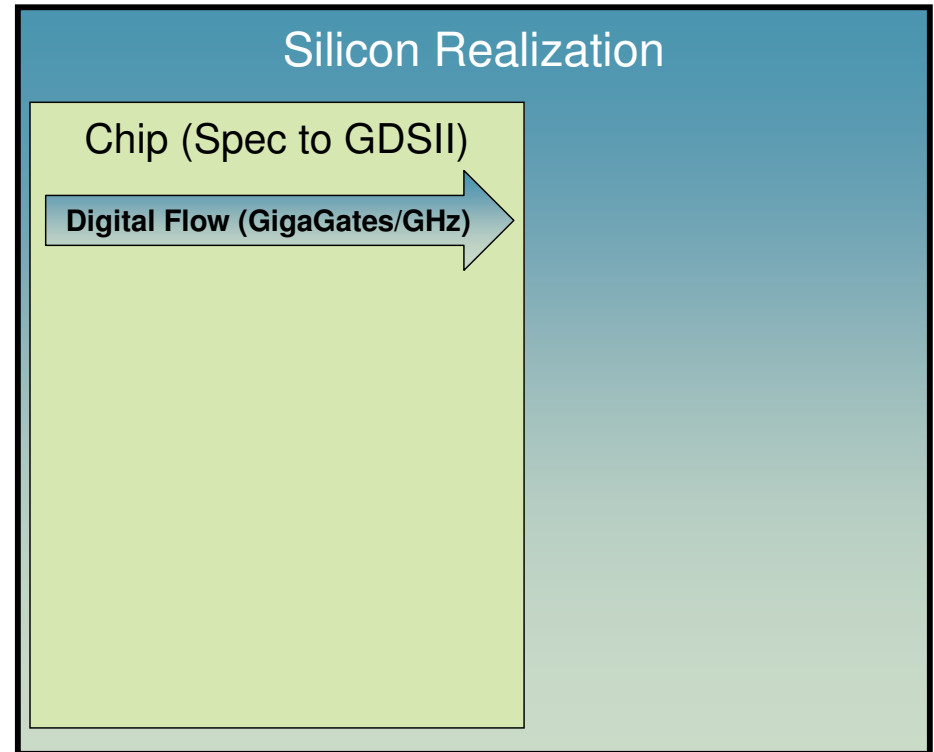
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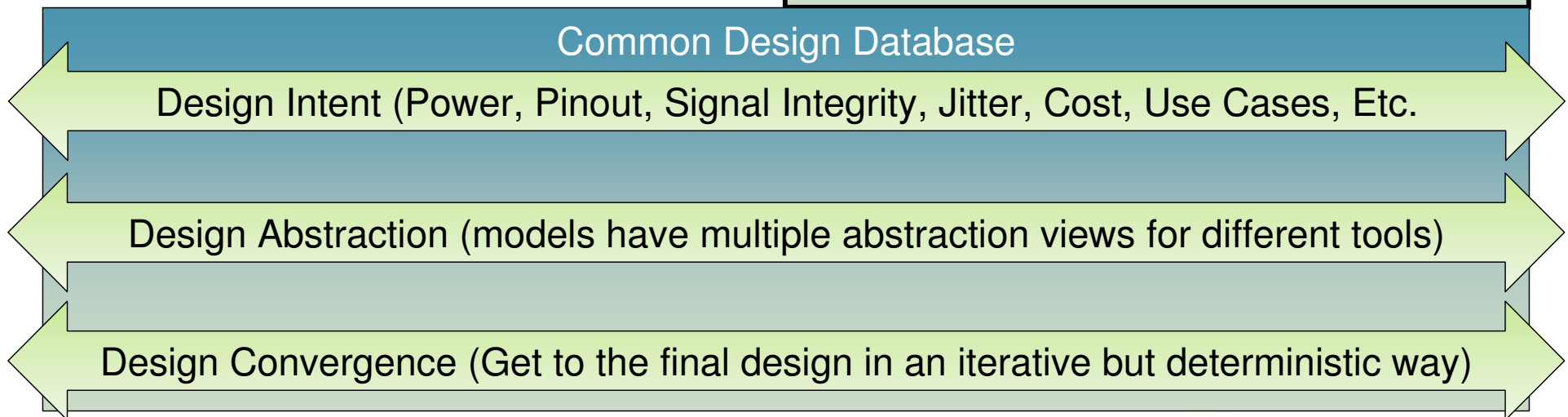
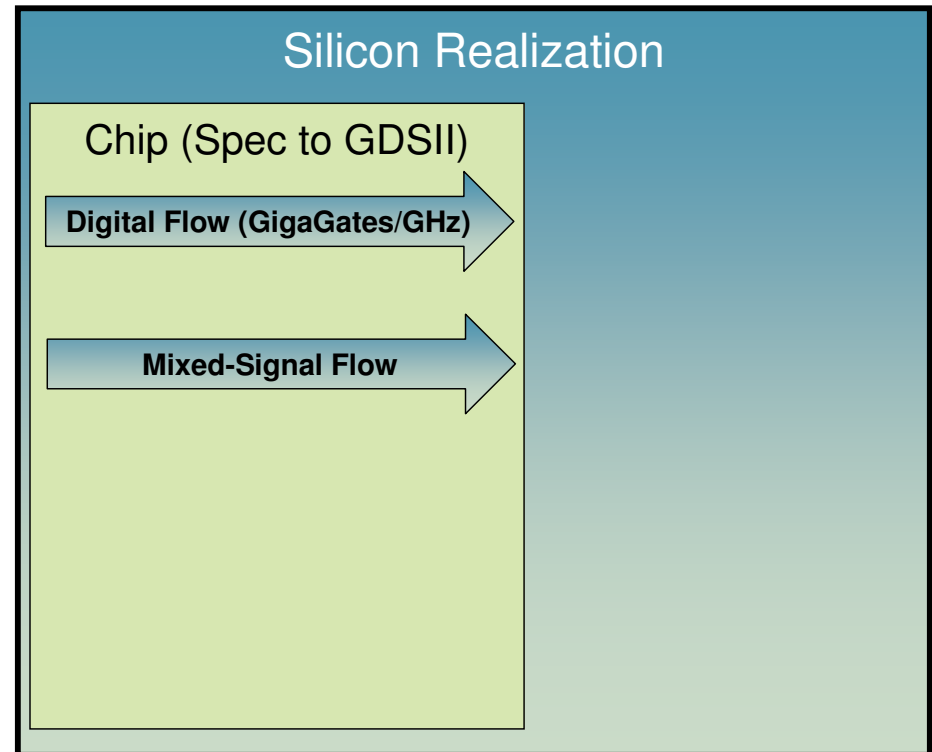
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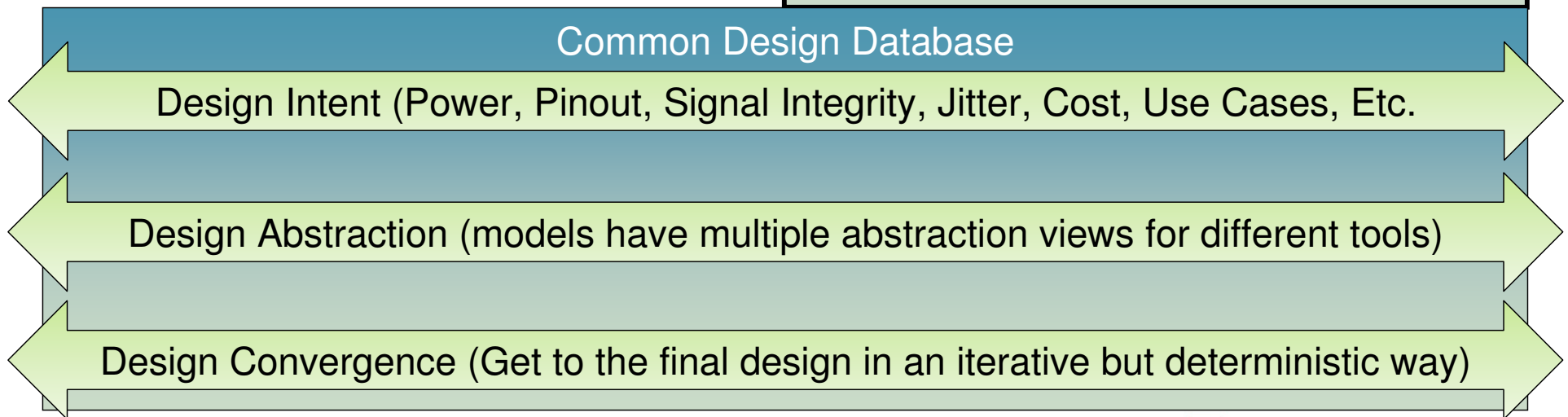
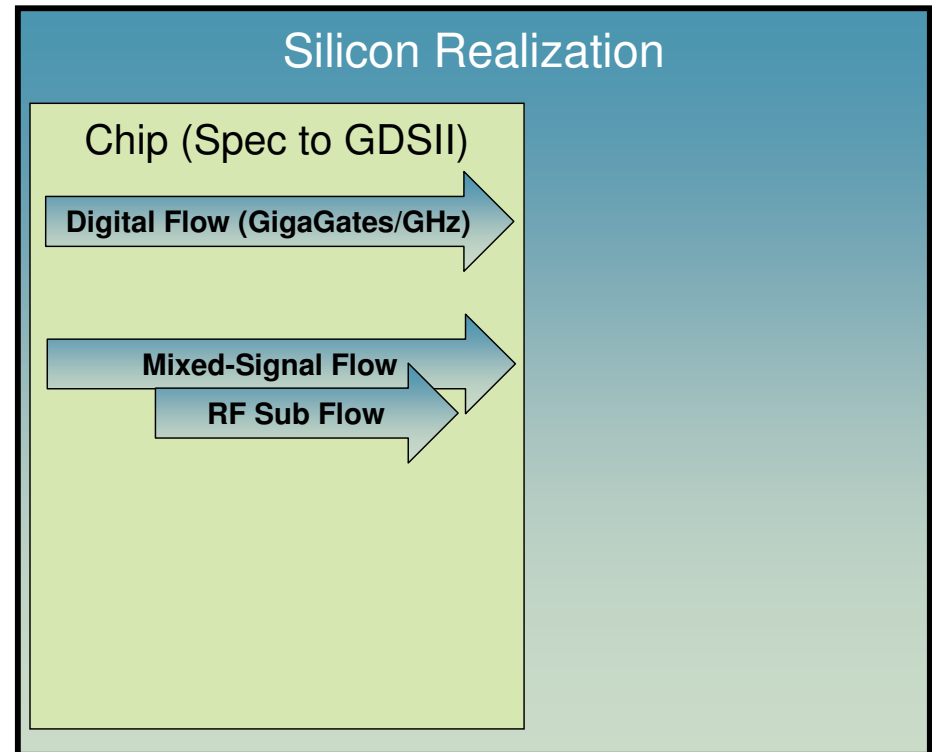
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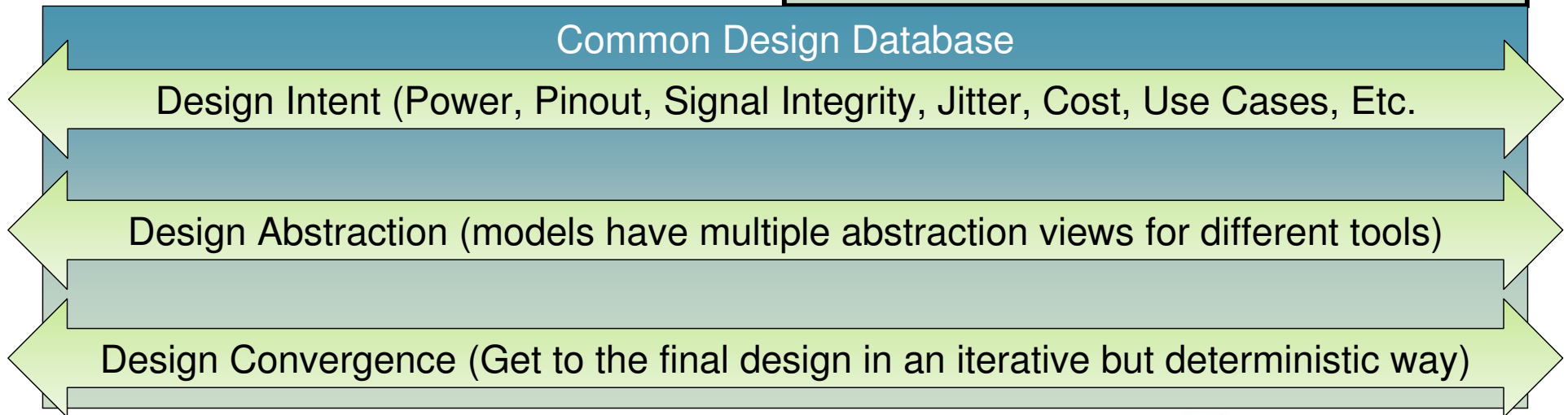
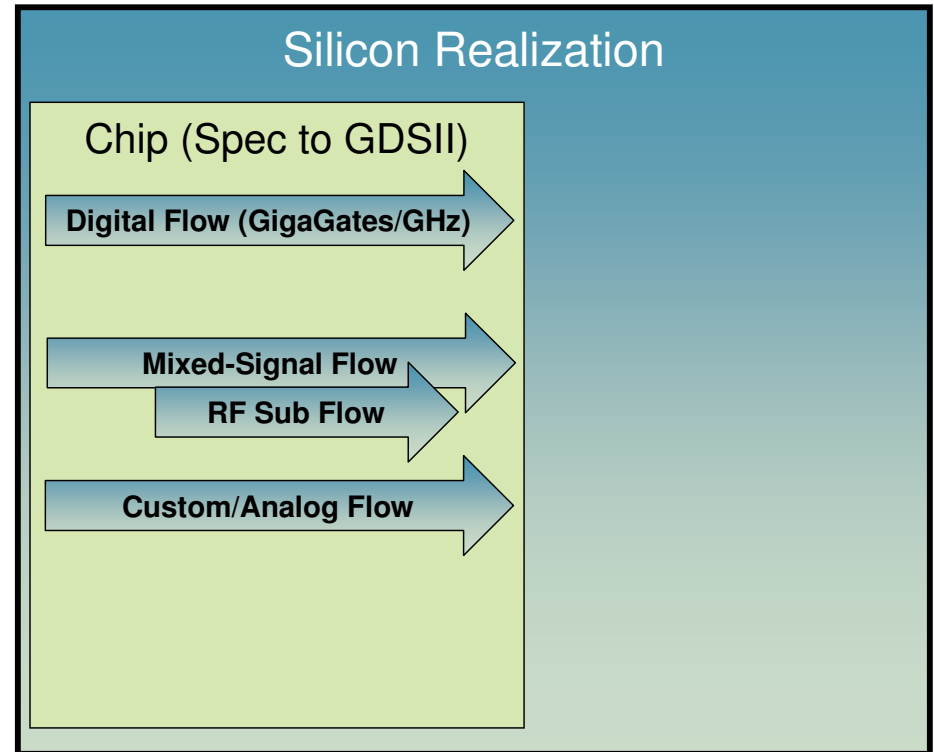
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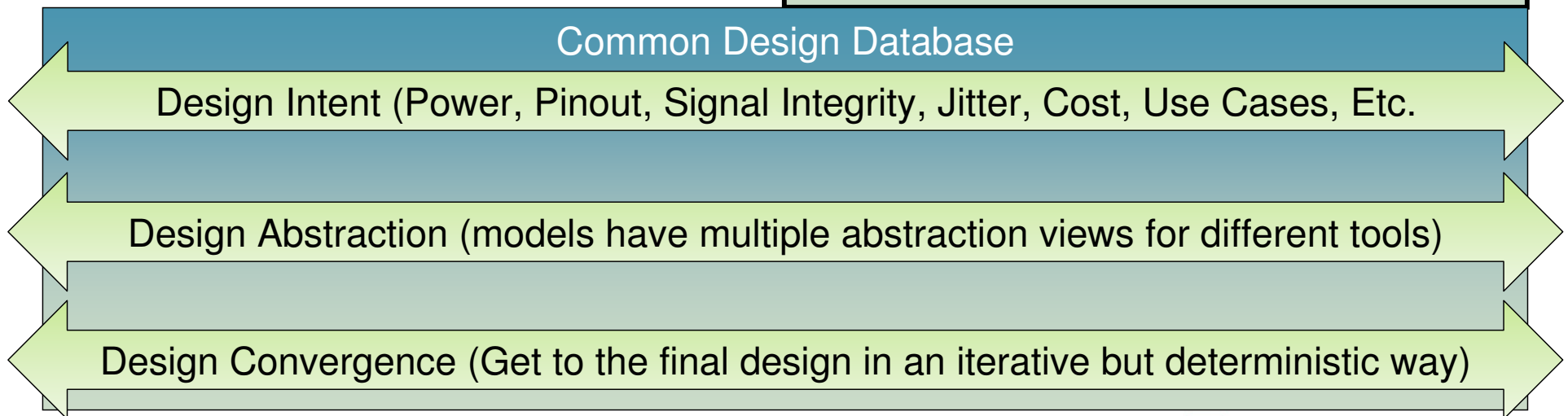
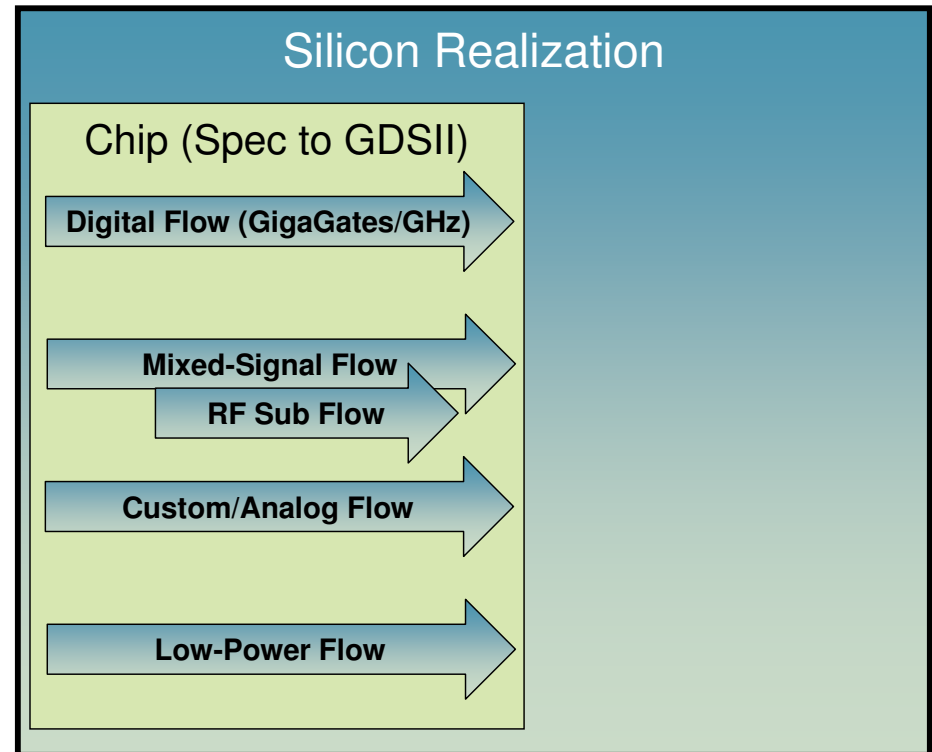
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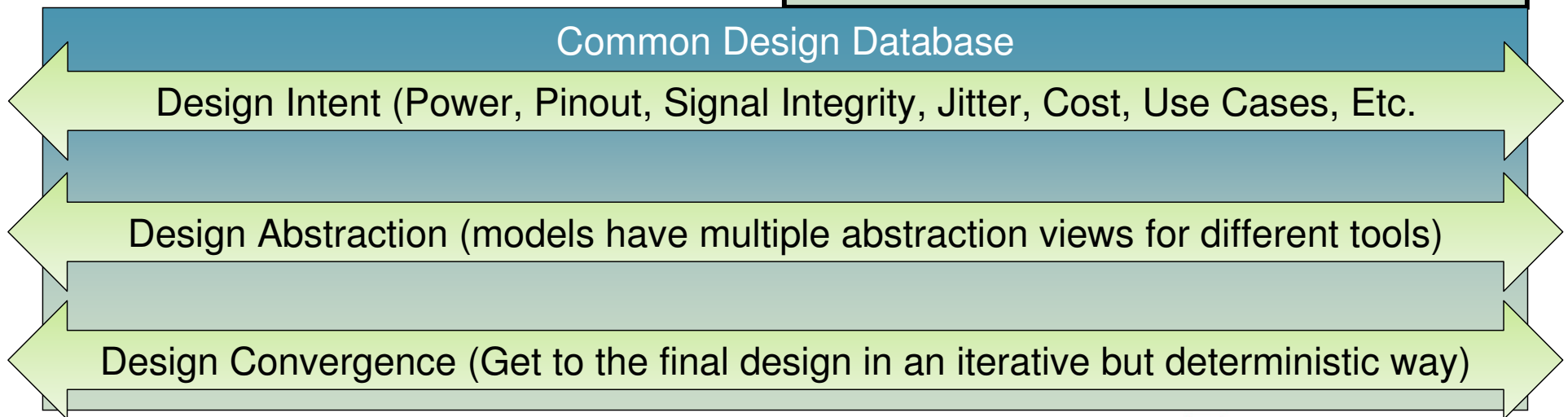
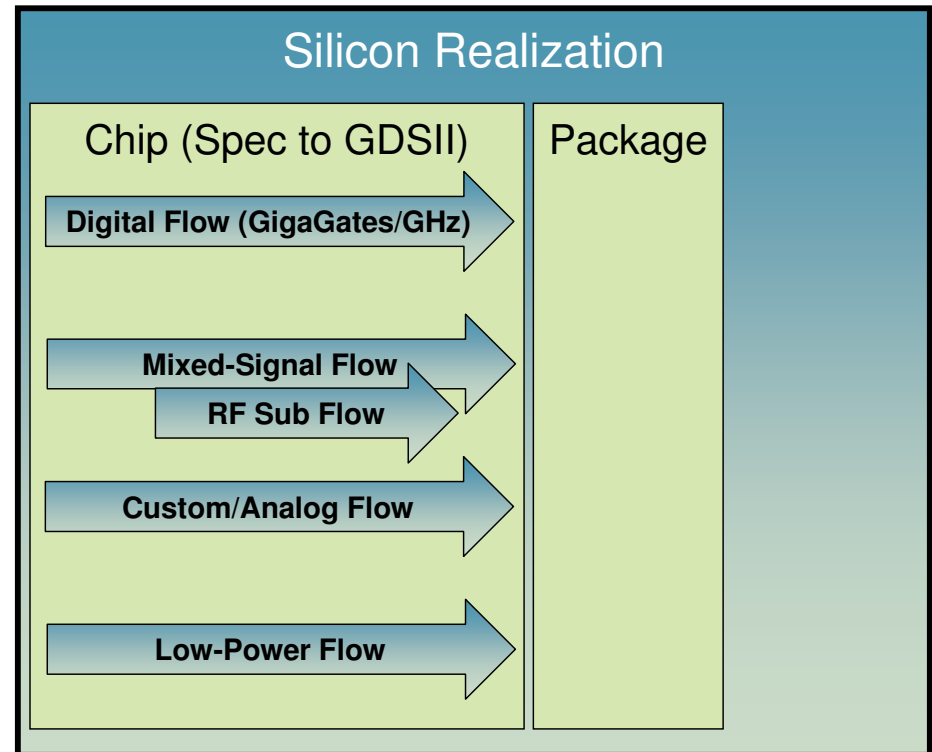
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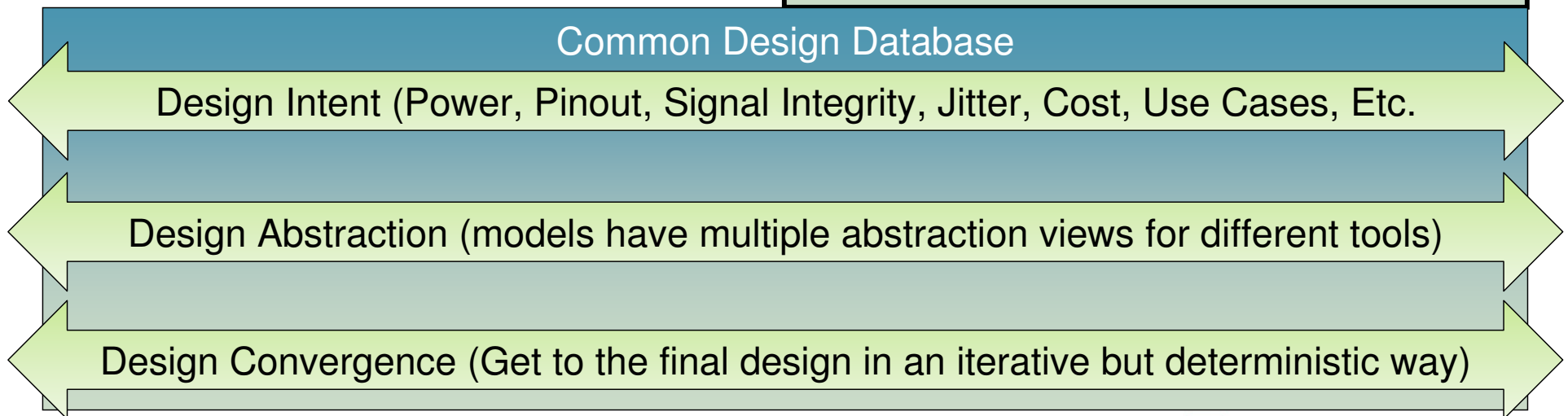
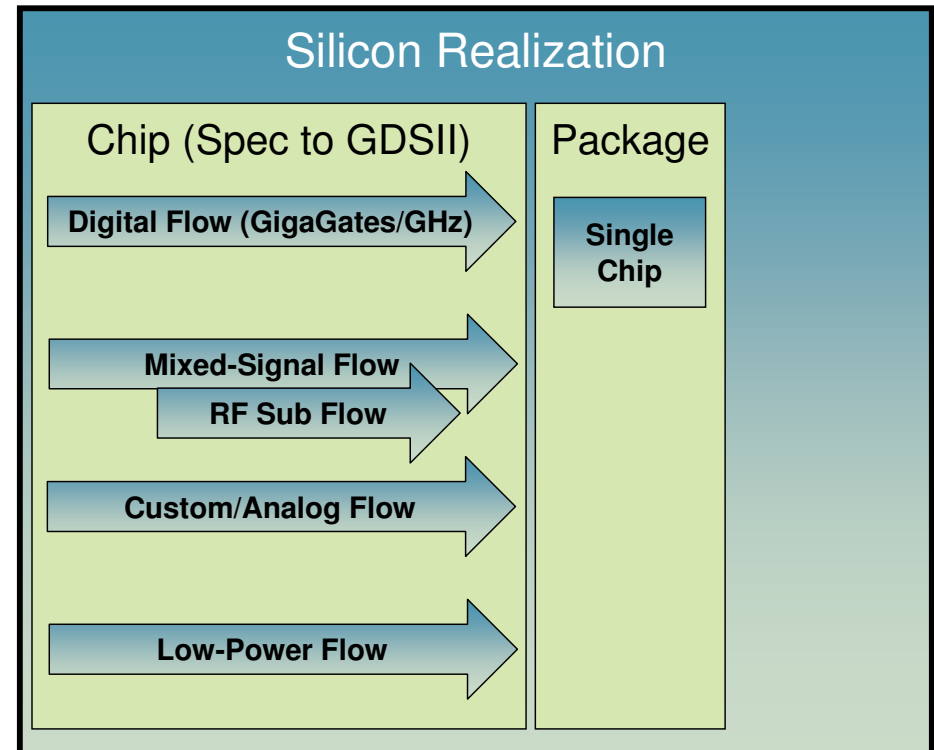
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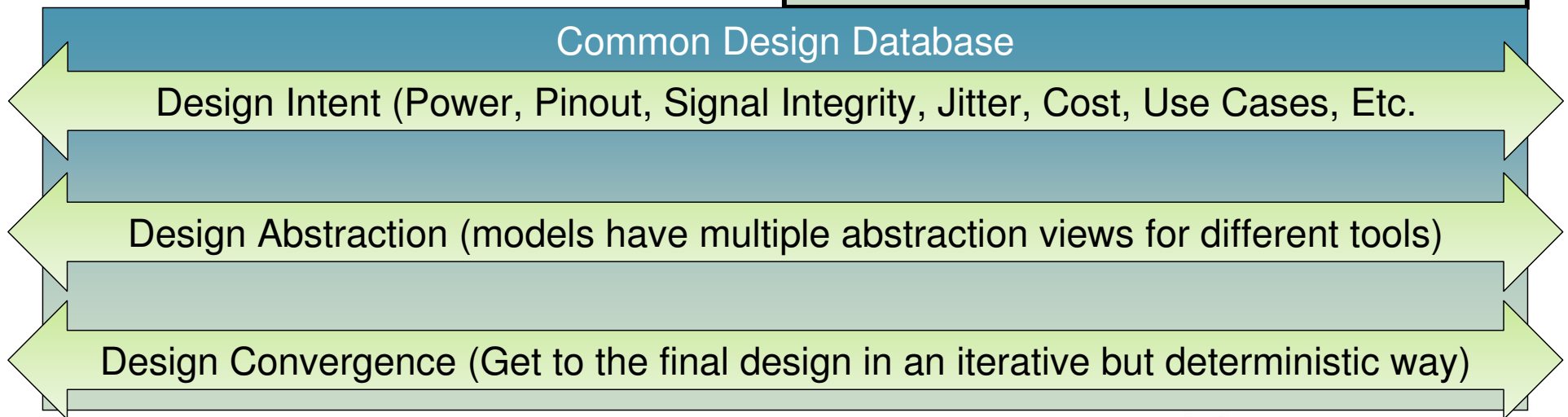
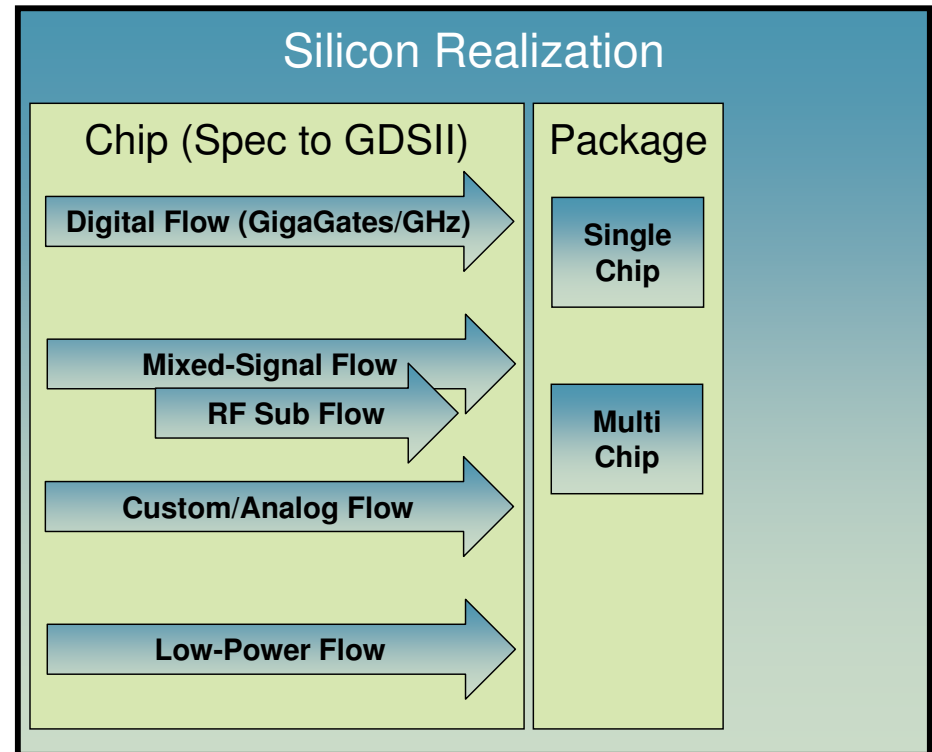
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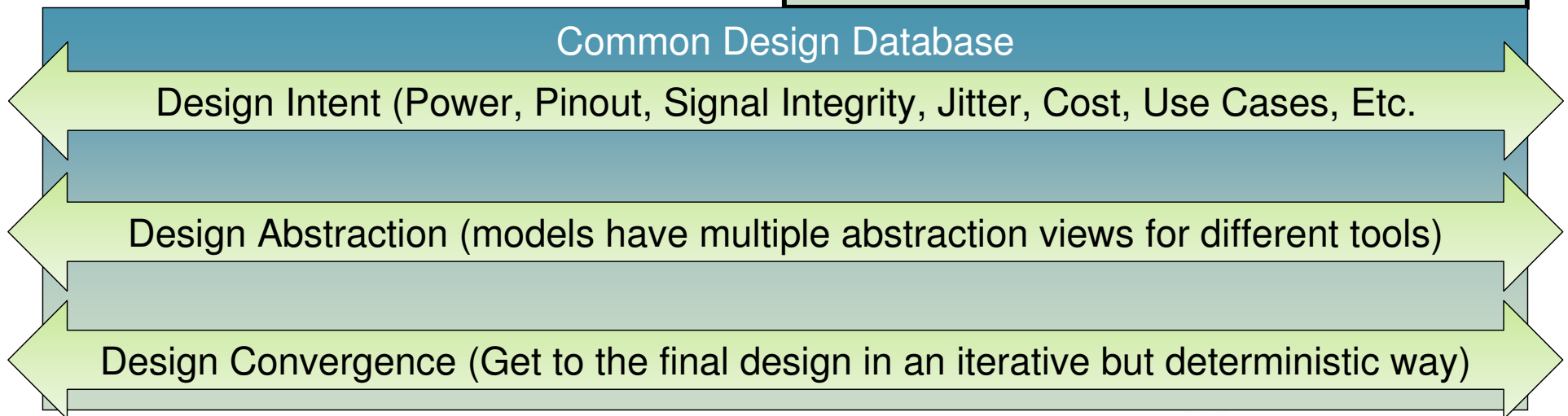
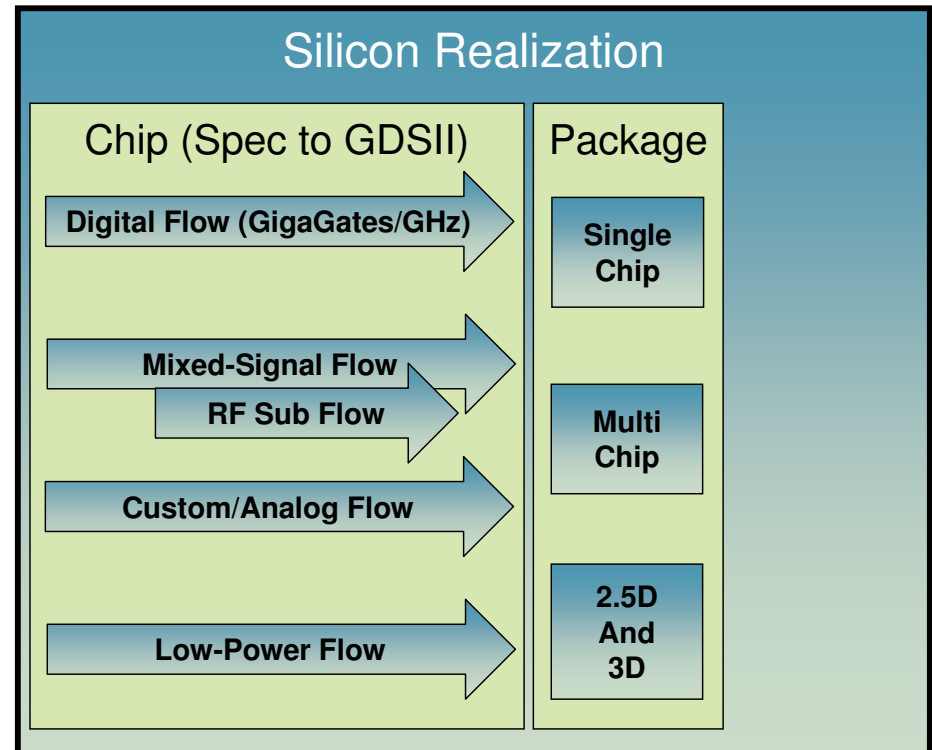
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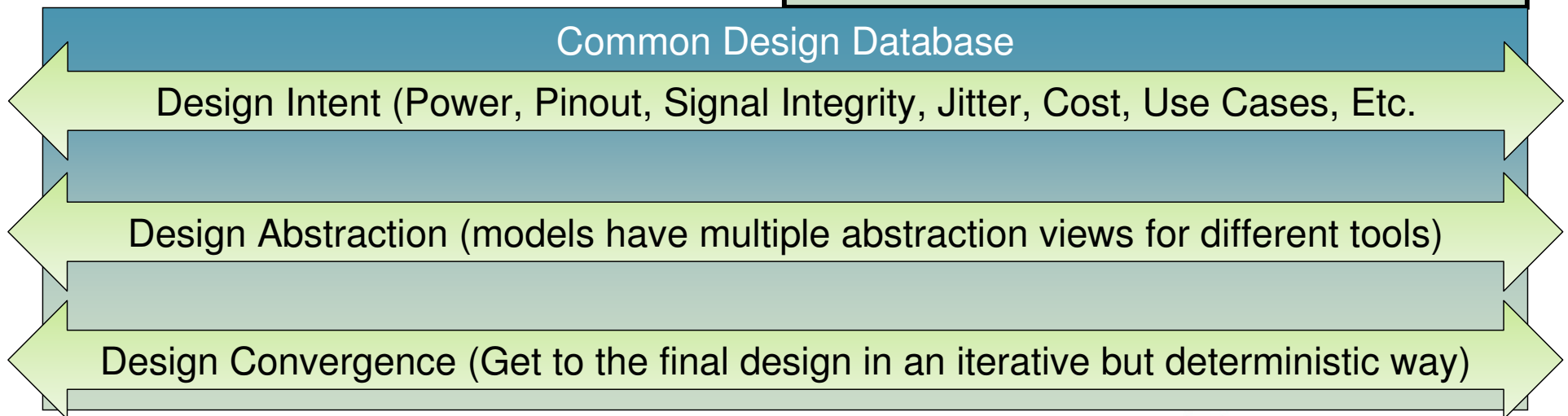
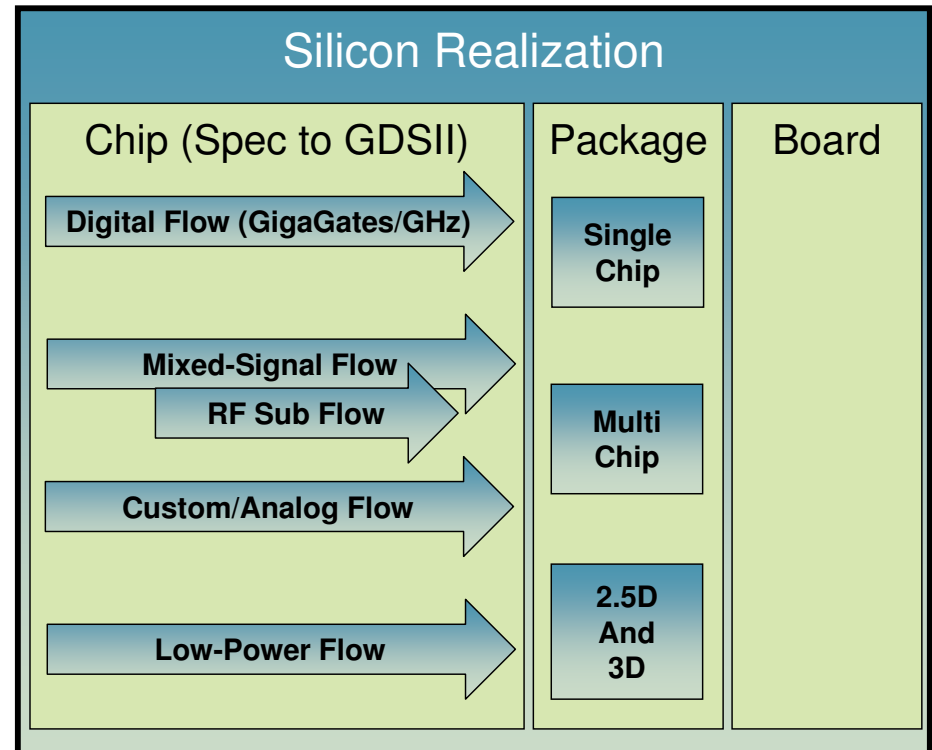
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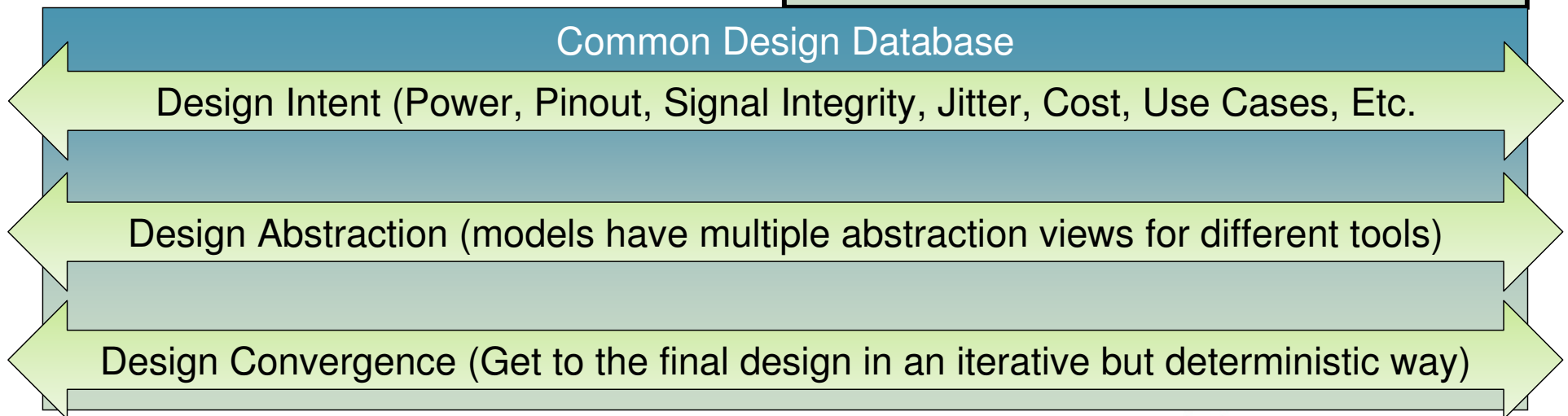
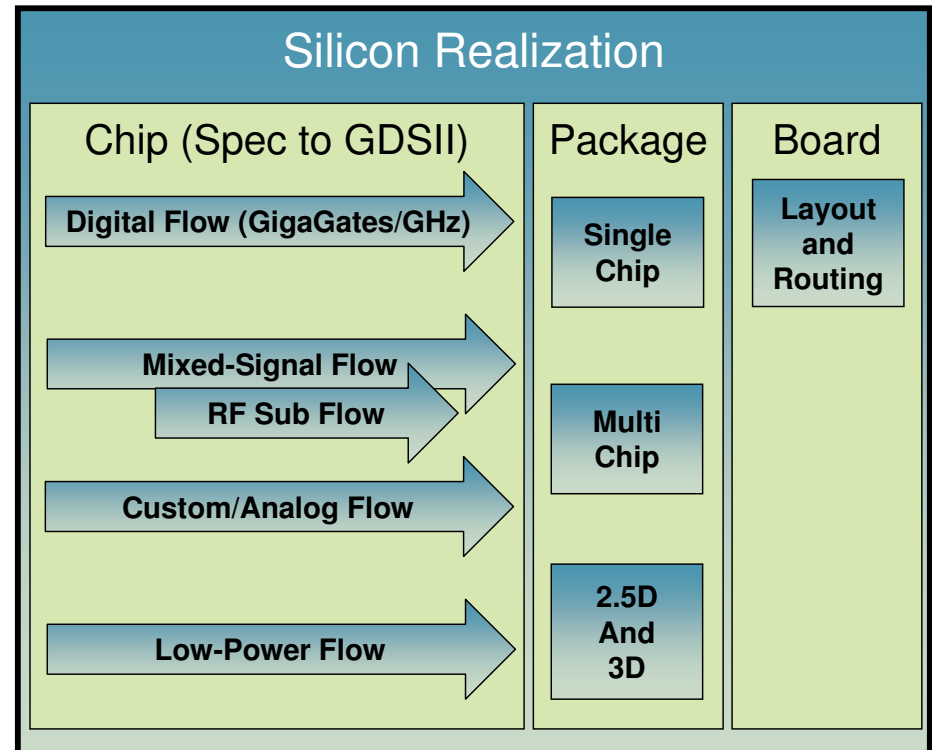
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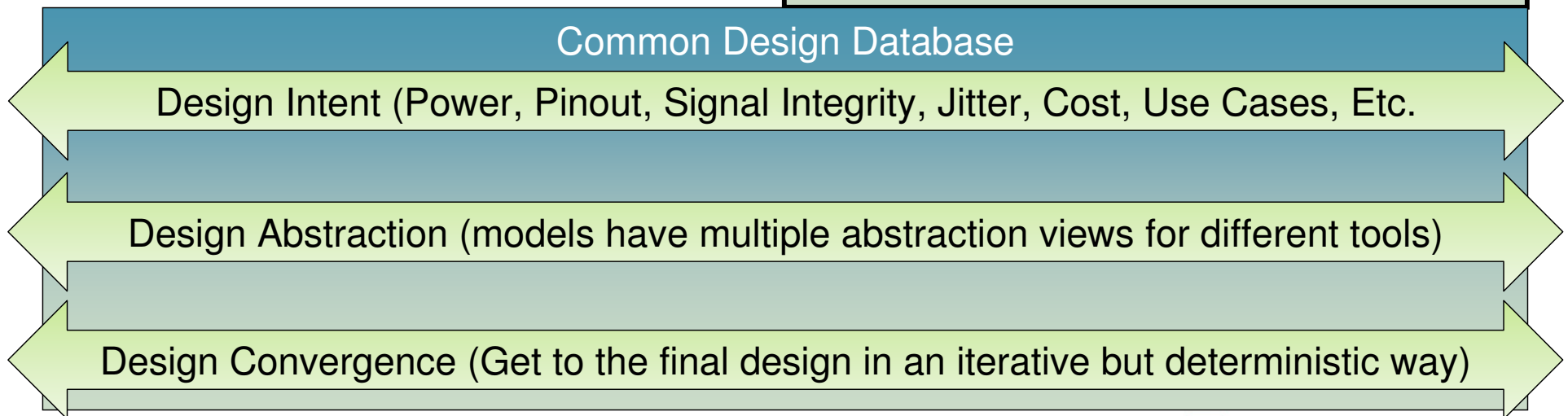
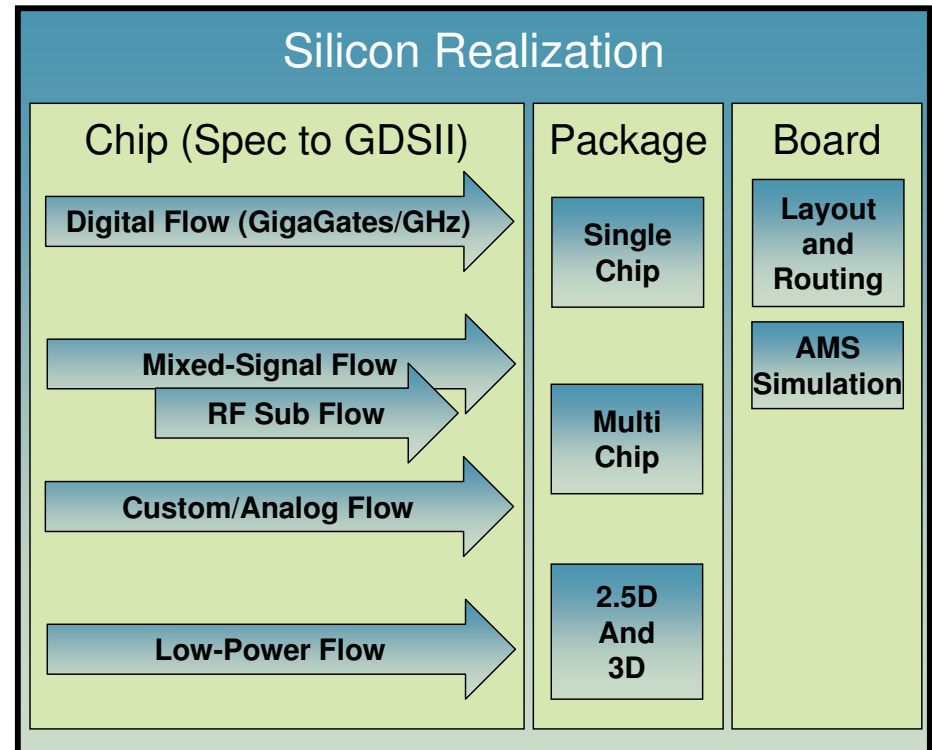
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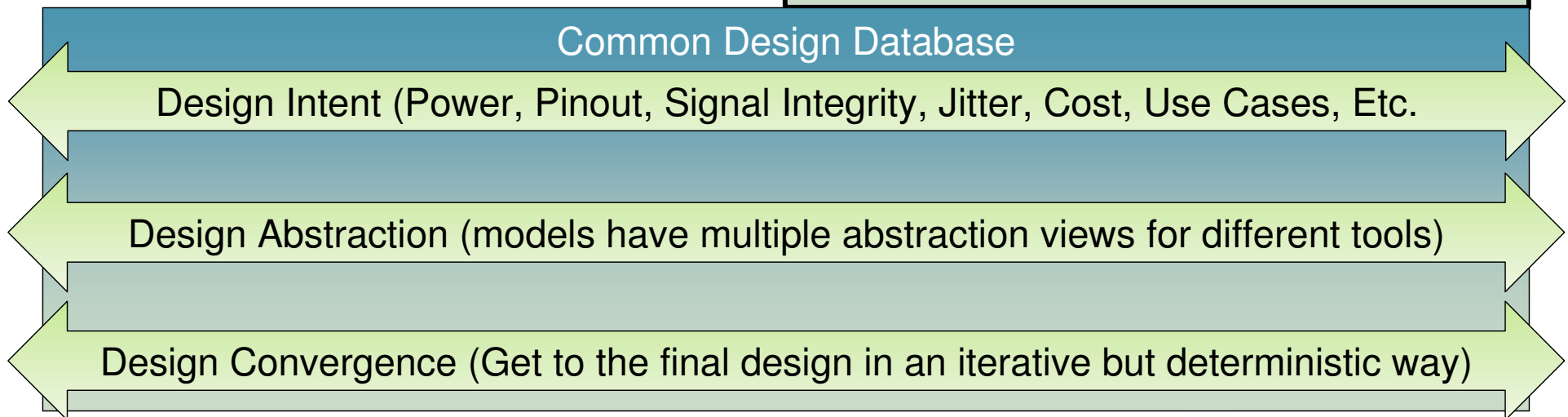
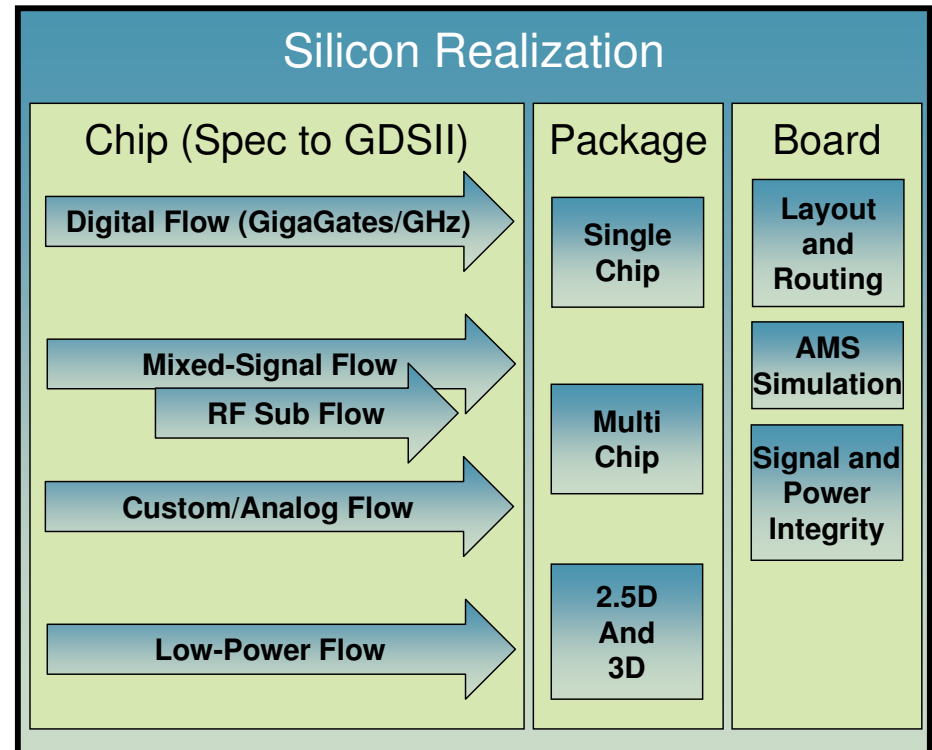
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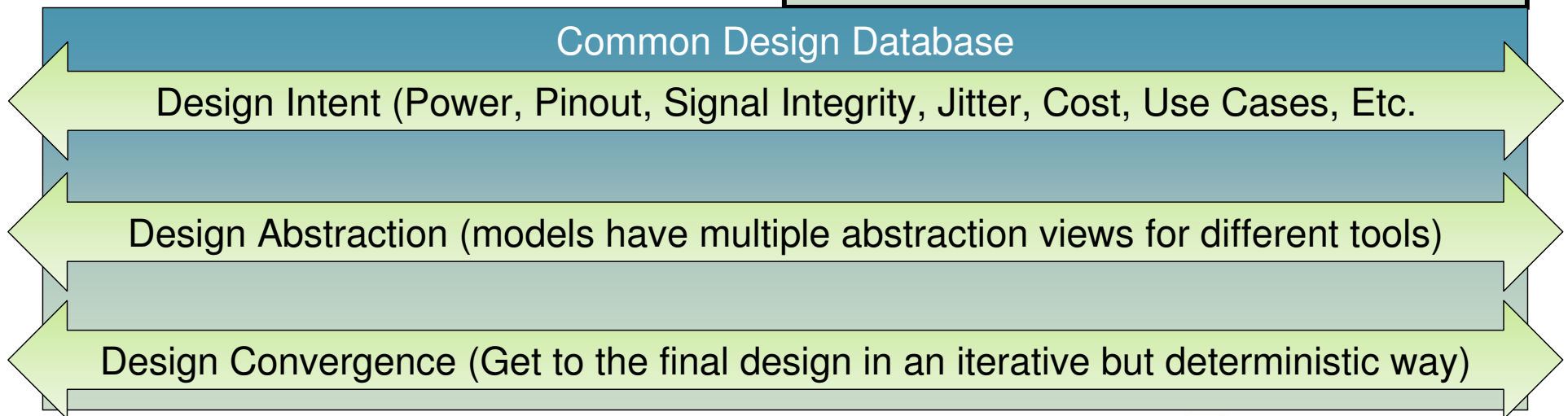
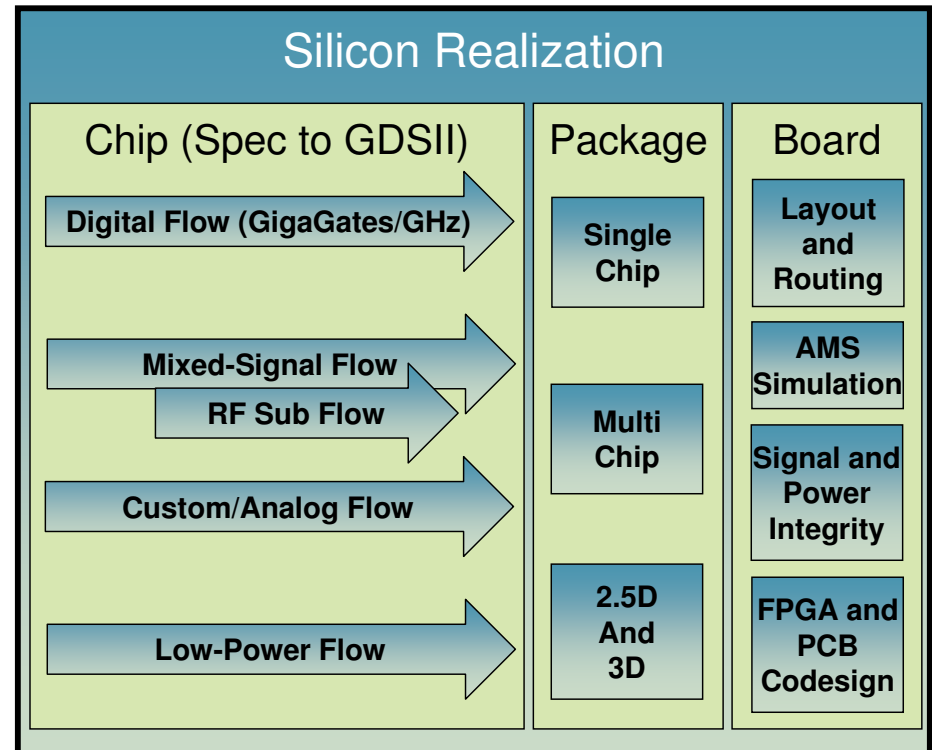
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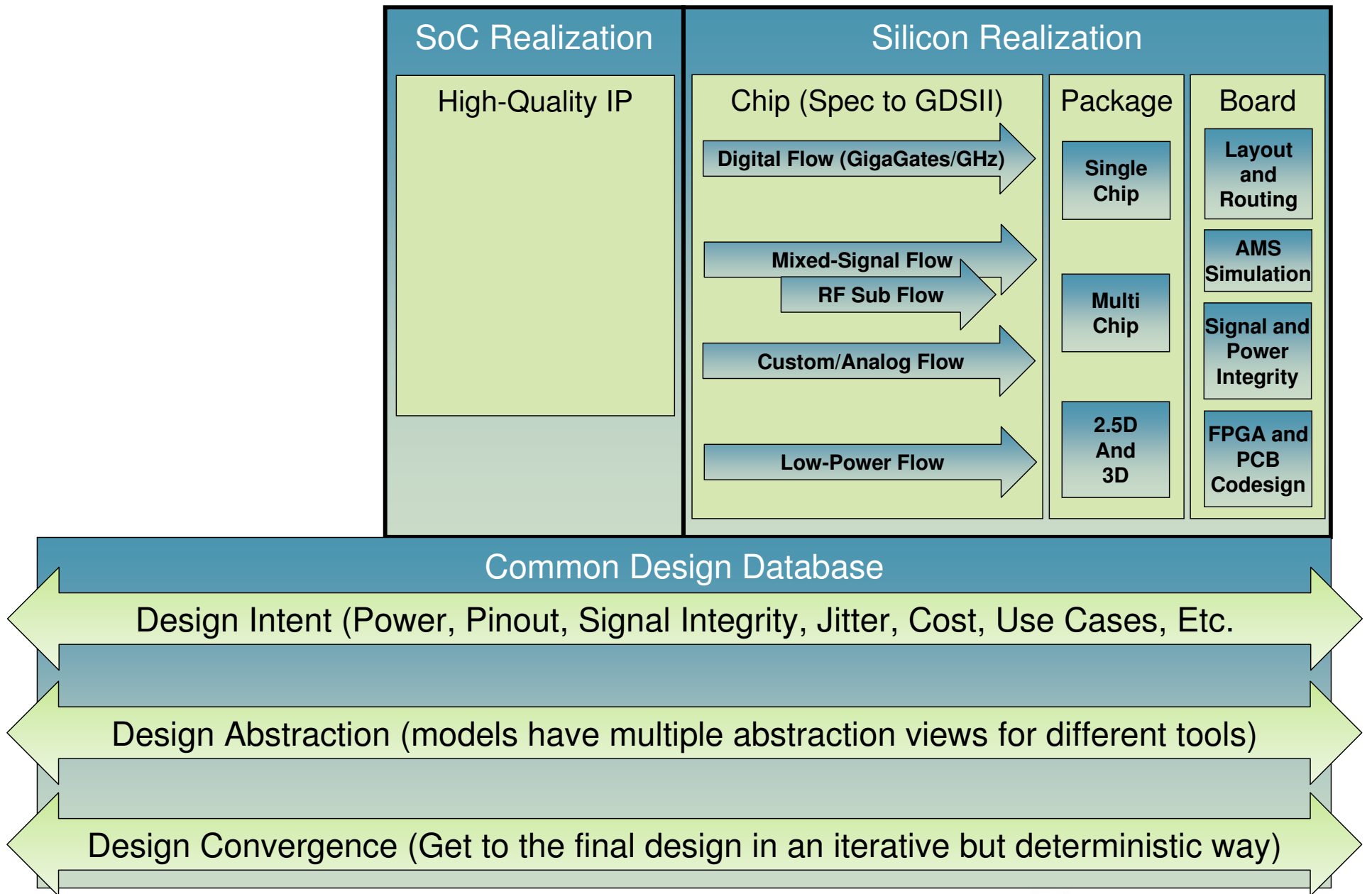
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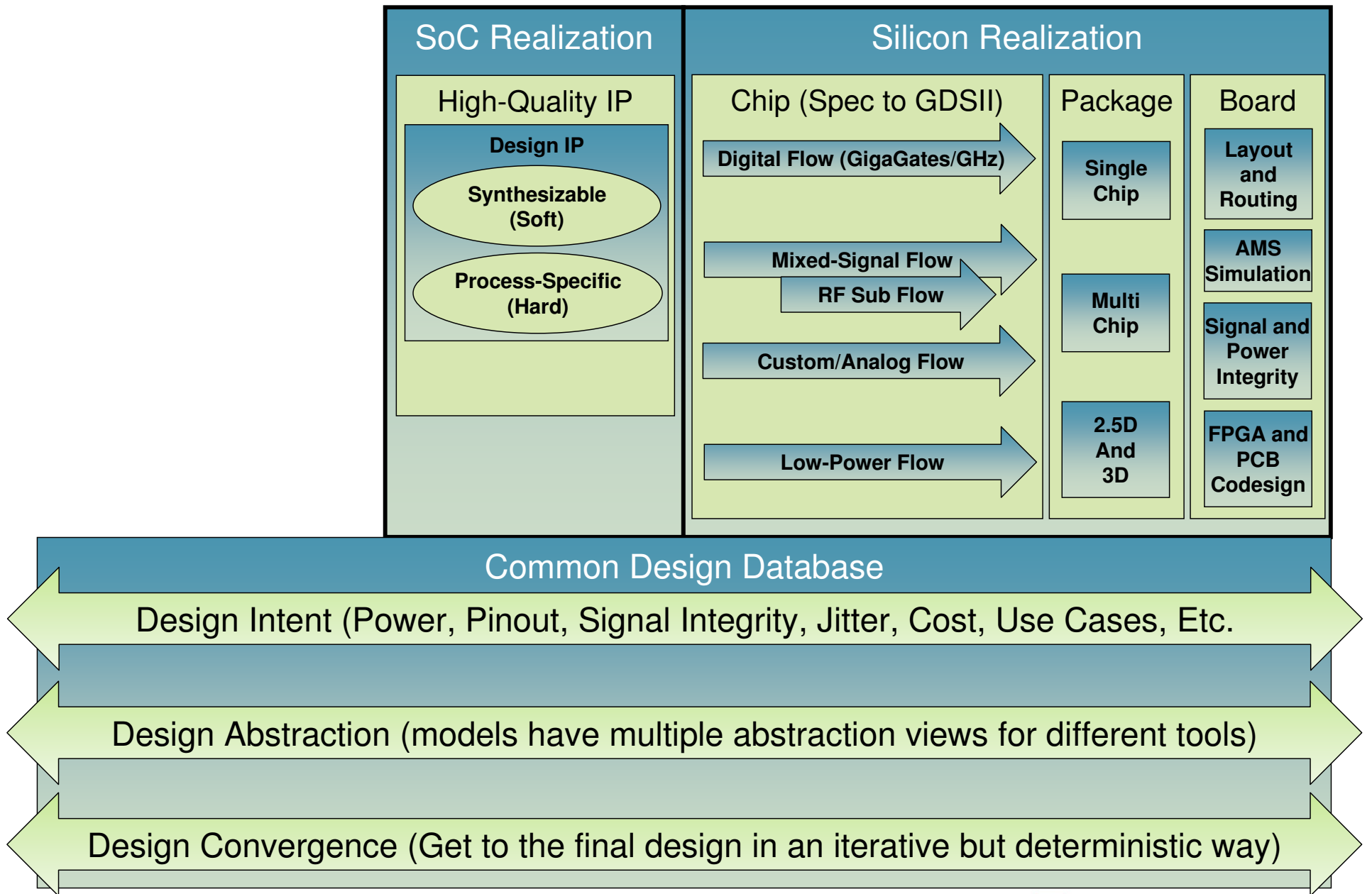
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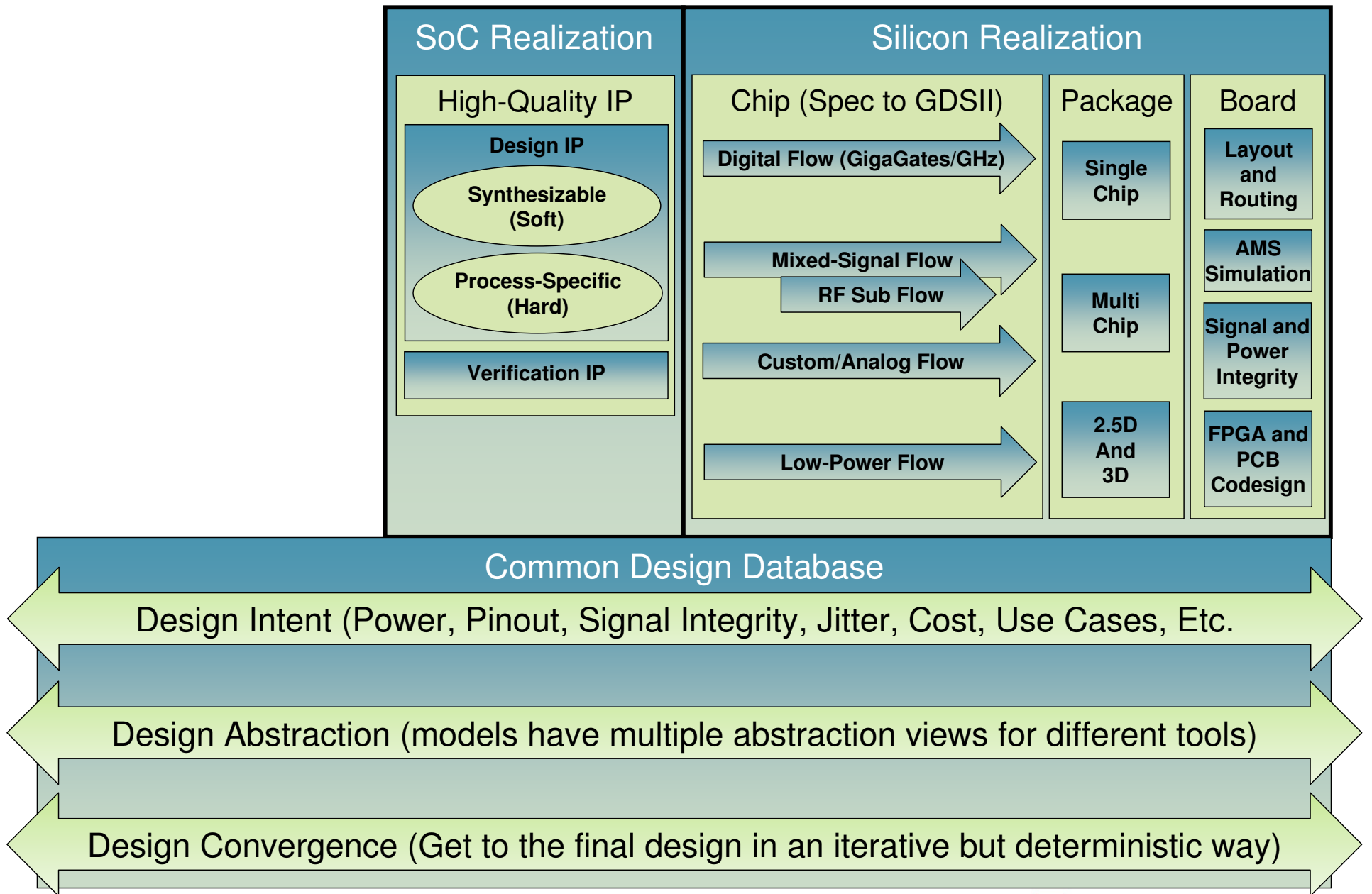
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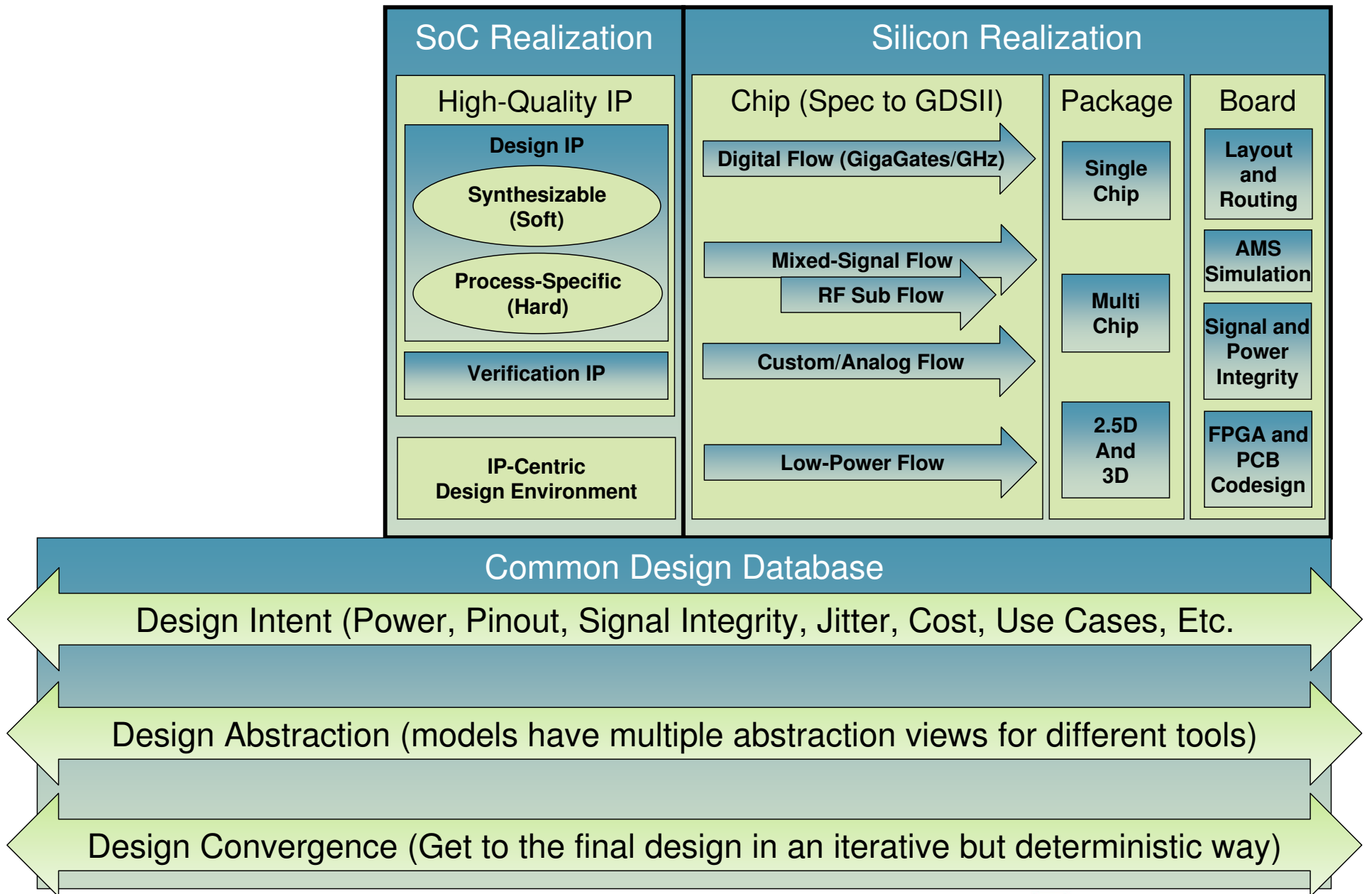
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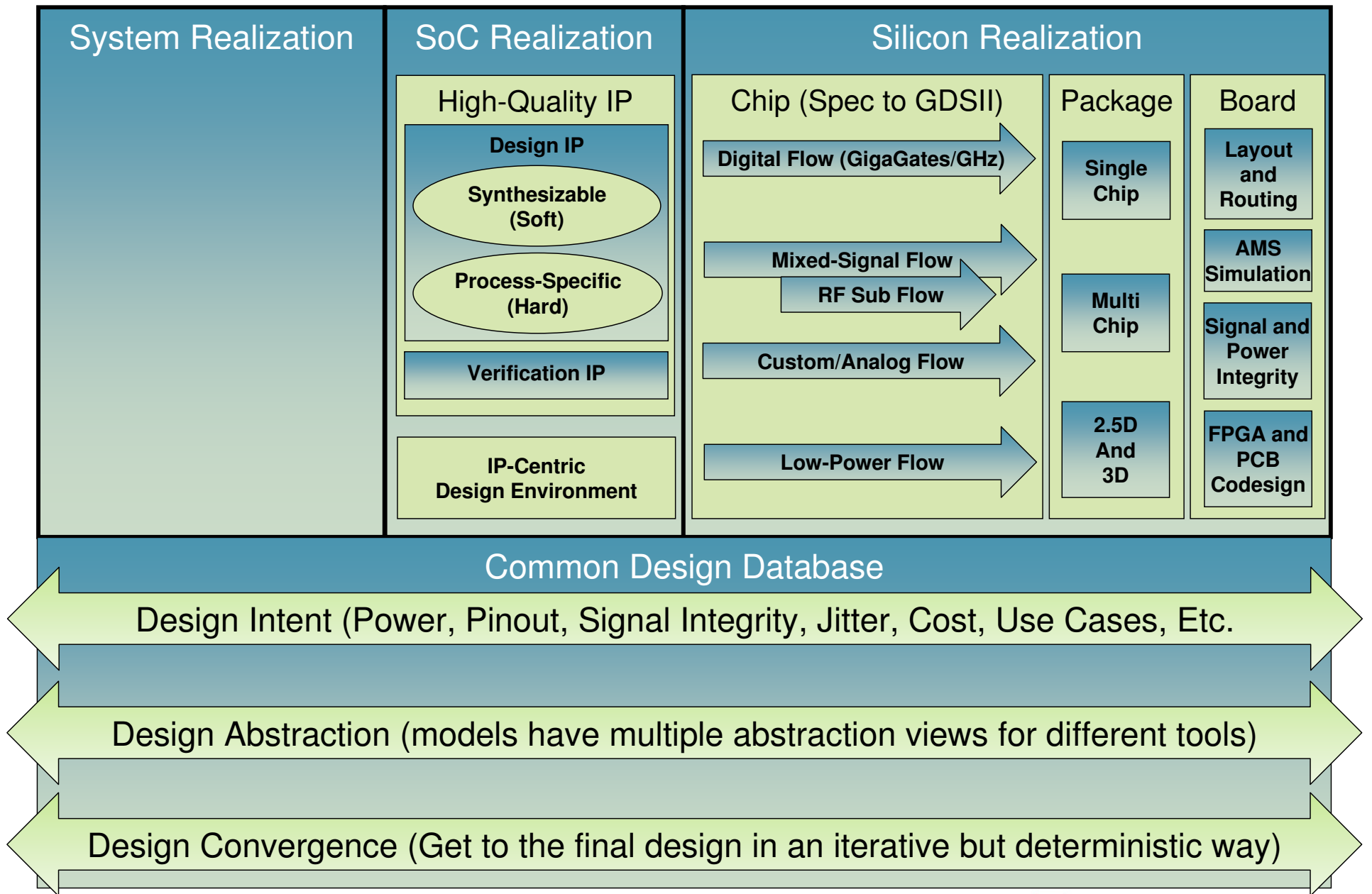
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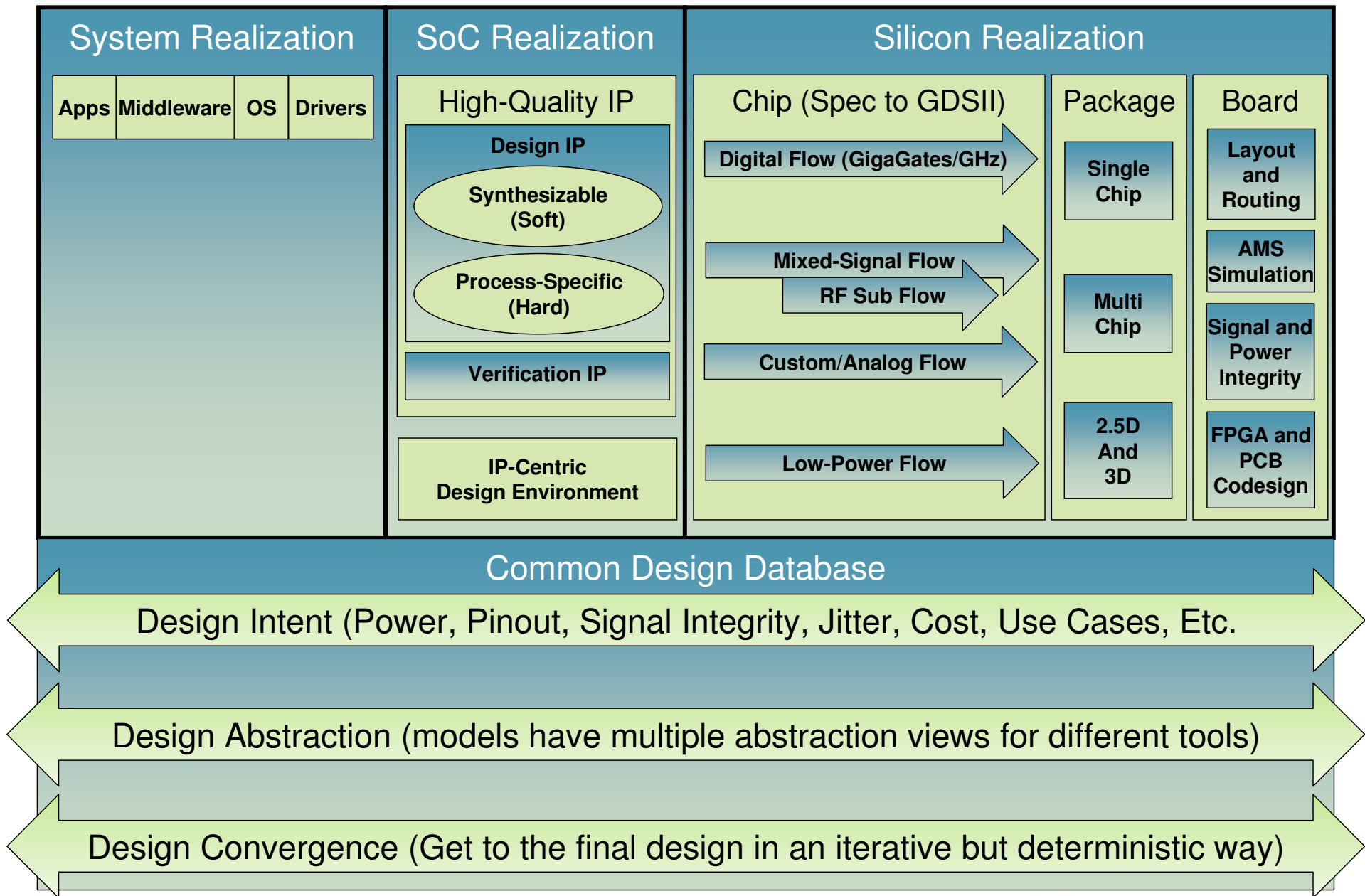
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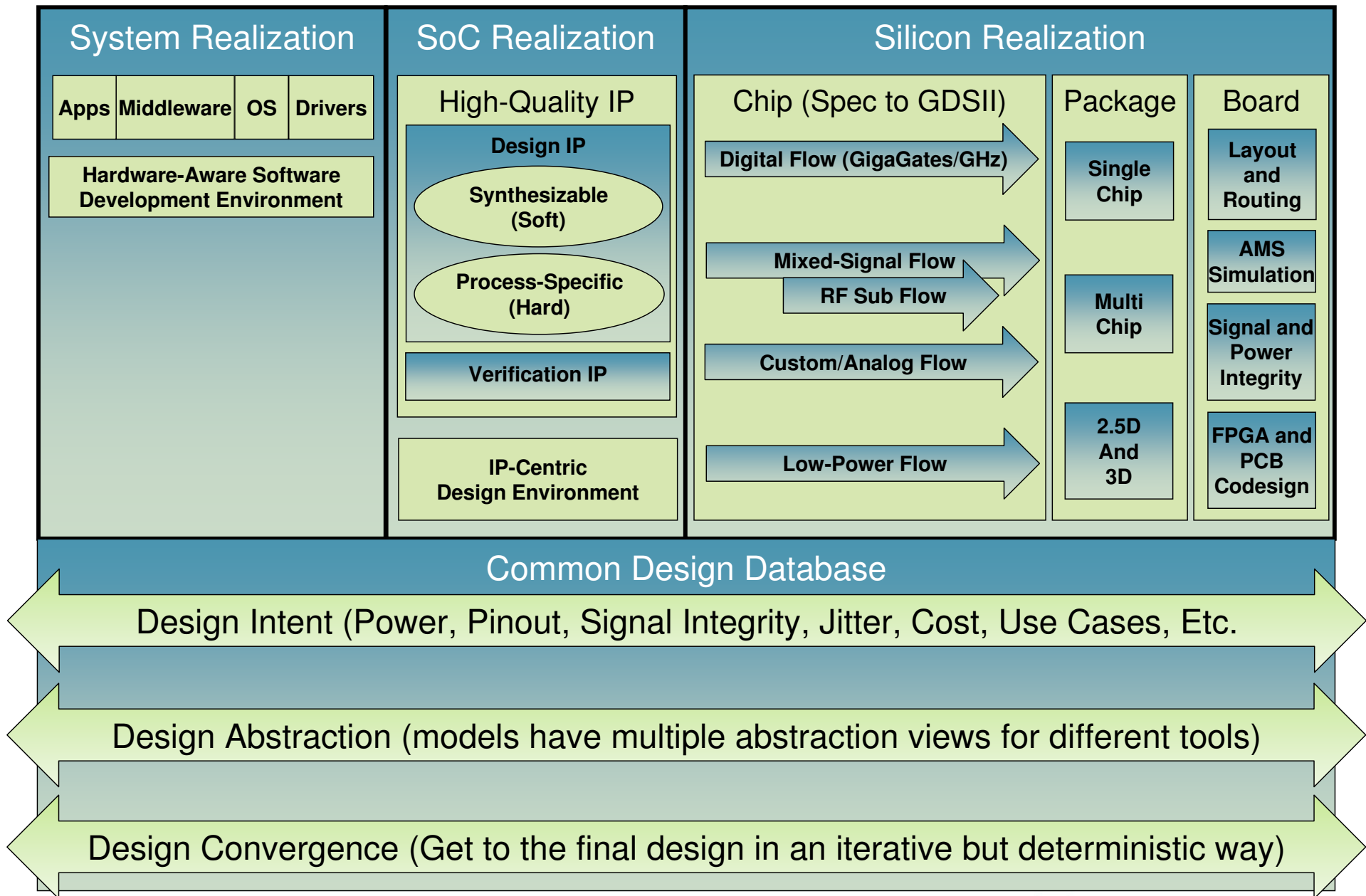
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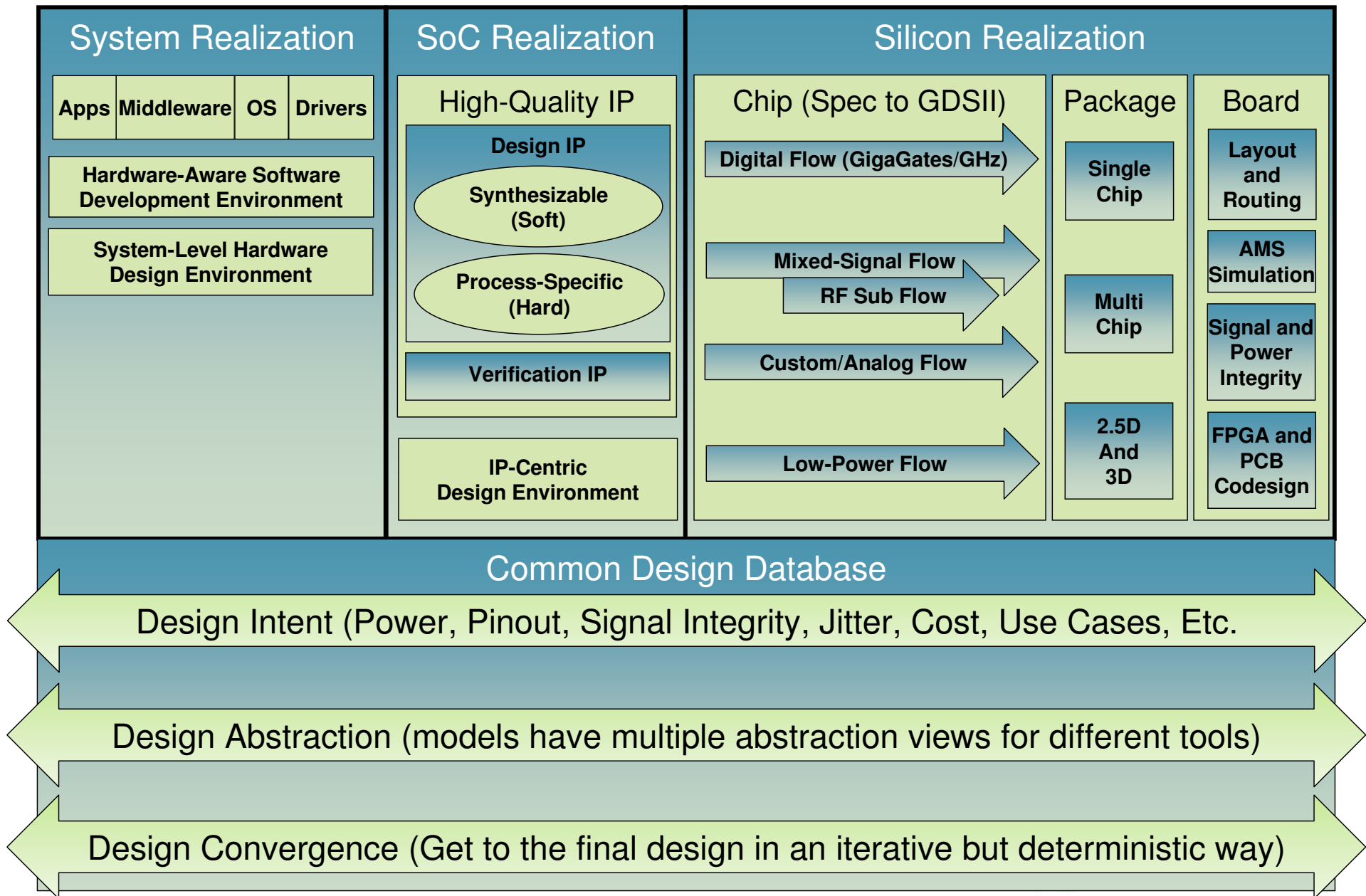
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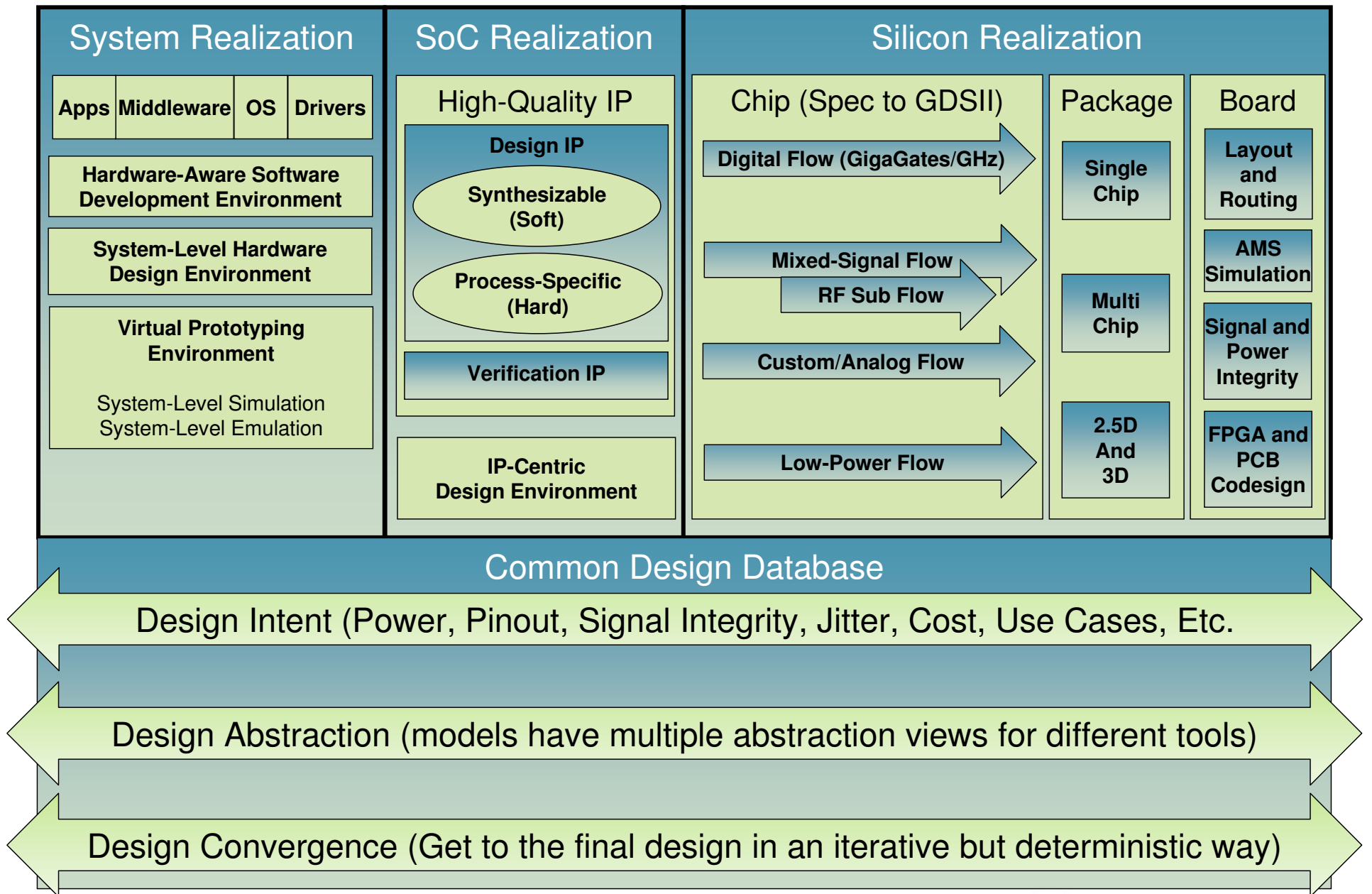
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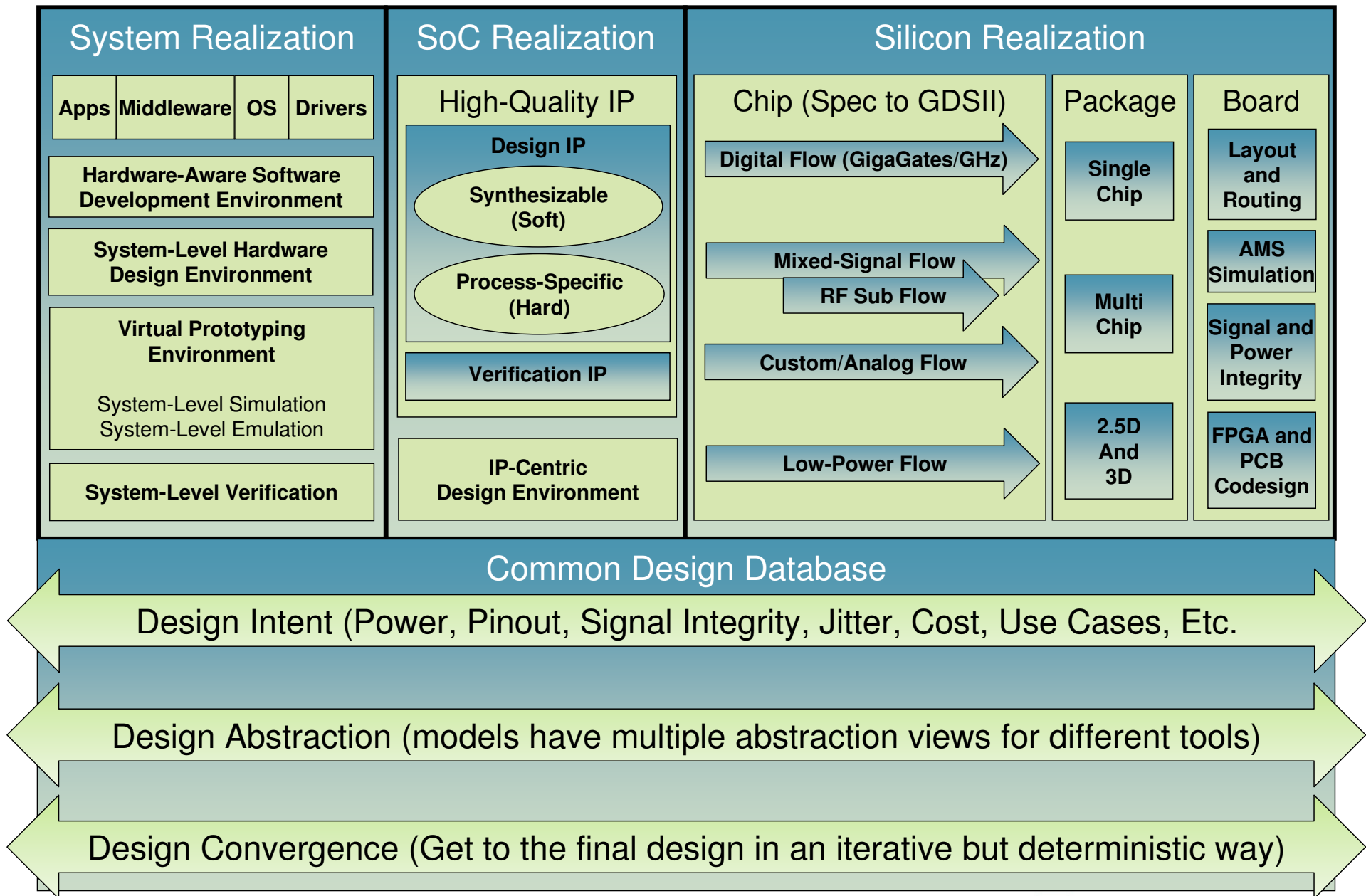
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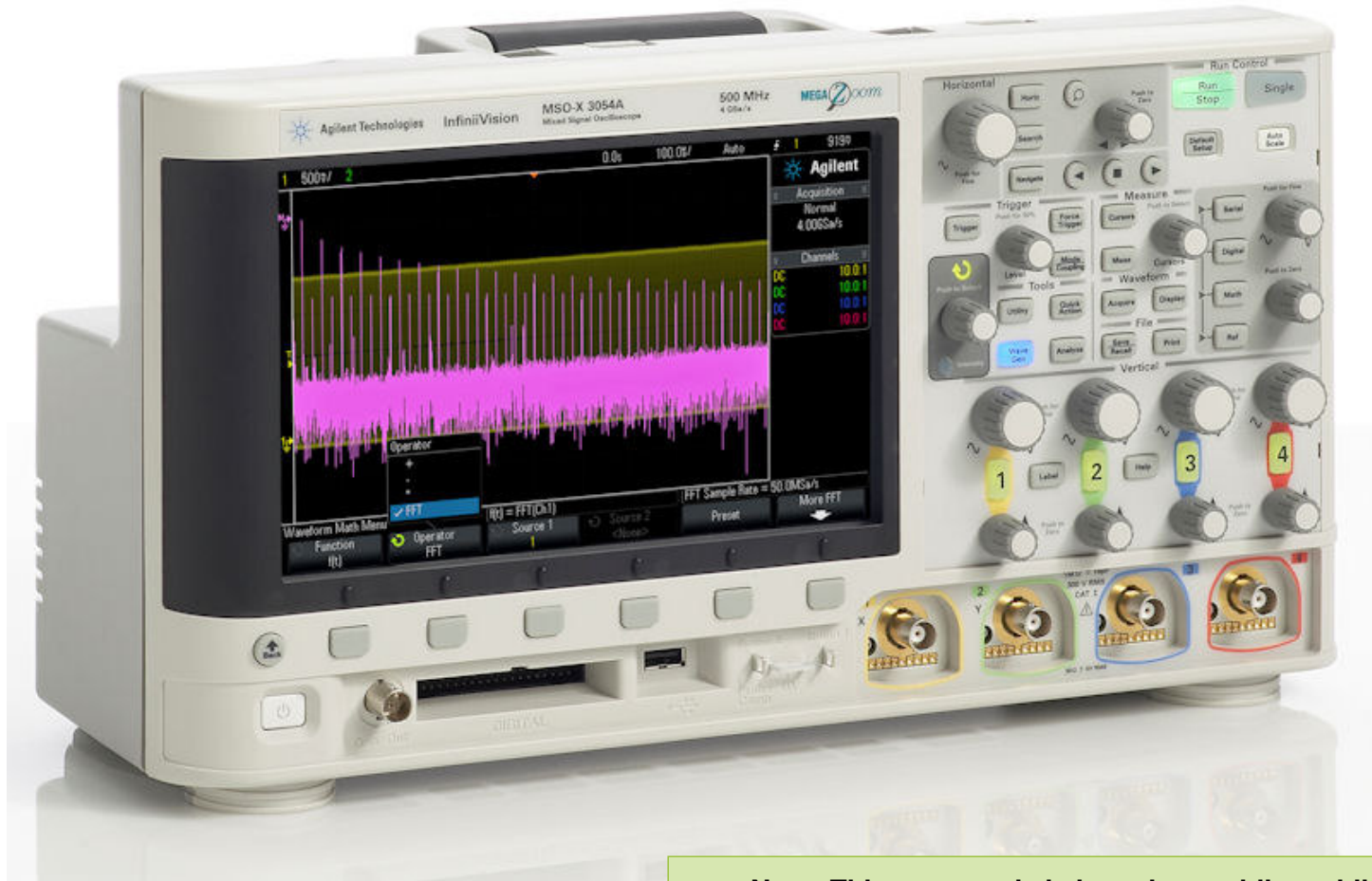
EDA360 – The Technical Version



EDA360 – The Technical Version



EDA360 Case Study: Agilent InfiniiVision Digital/Mixed-Signal Sampling Oscilloscope

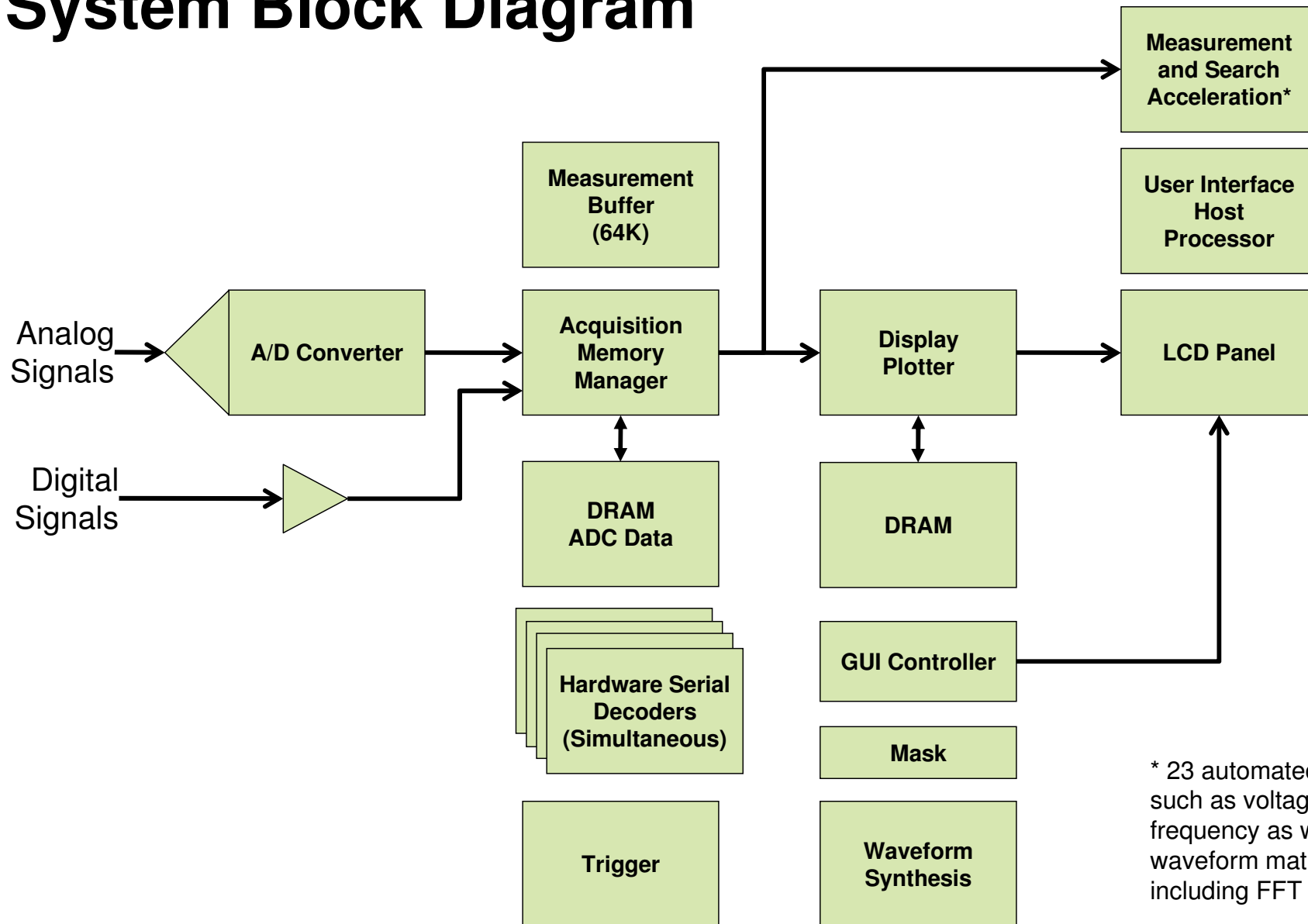


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Note: This case study is based on public, published data and nothing is implied about the EDA tools used to develop this product.



Agilent InfiniiVision 2000/3000 DSO/MSO System Block Diagram



* 23 automated measurements such as voltage, time, and frequency as well as four waveform math functions including FFT

Diagram as published in EE Times

Agilent InfiniiVision 2000/3000 DSO/MSO System Intent

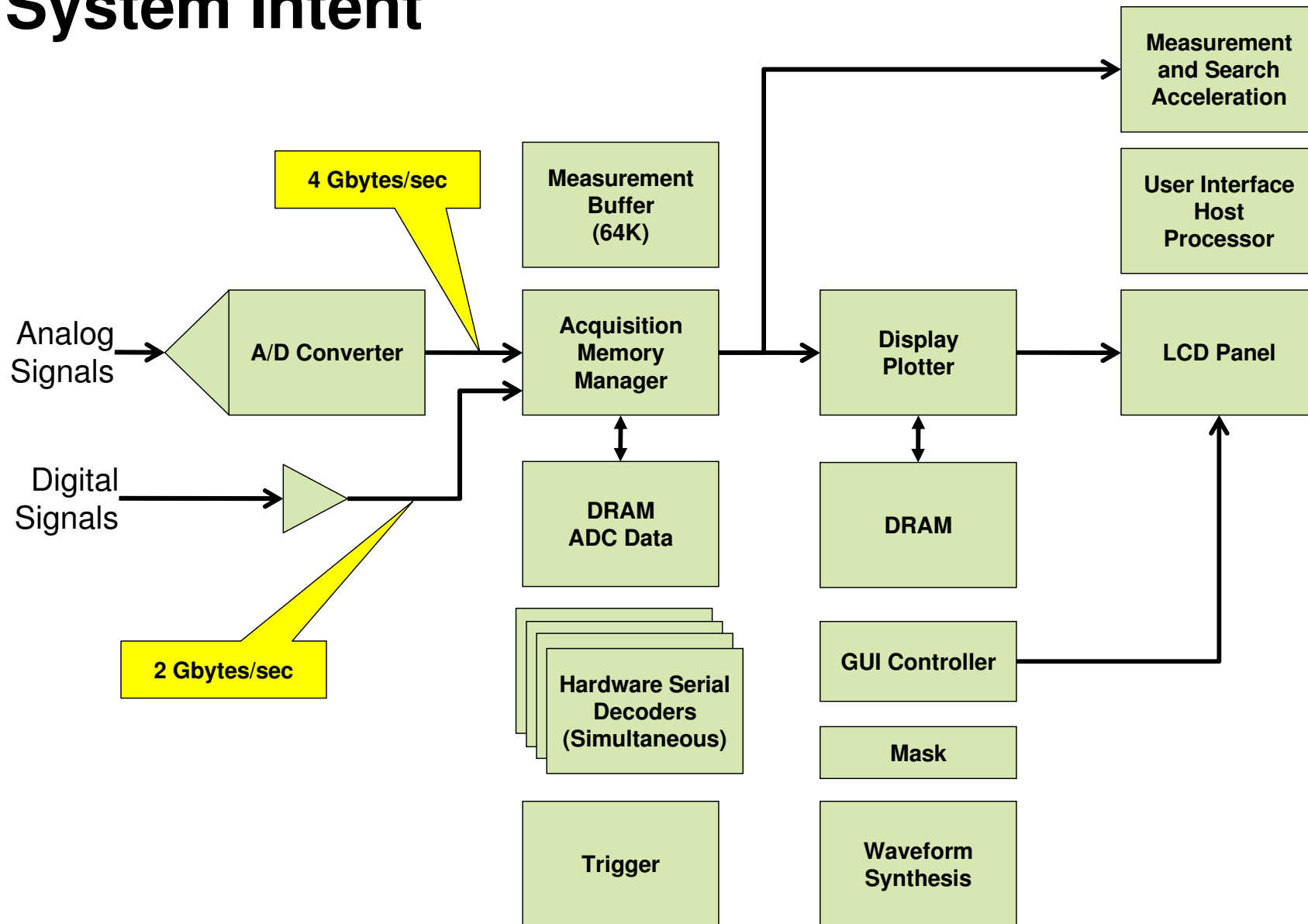


Diagram as published in EE Times



Agilent InfiniiVision 2000/3000 DSO/MSO System Intent

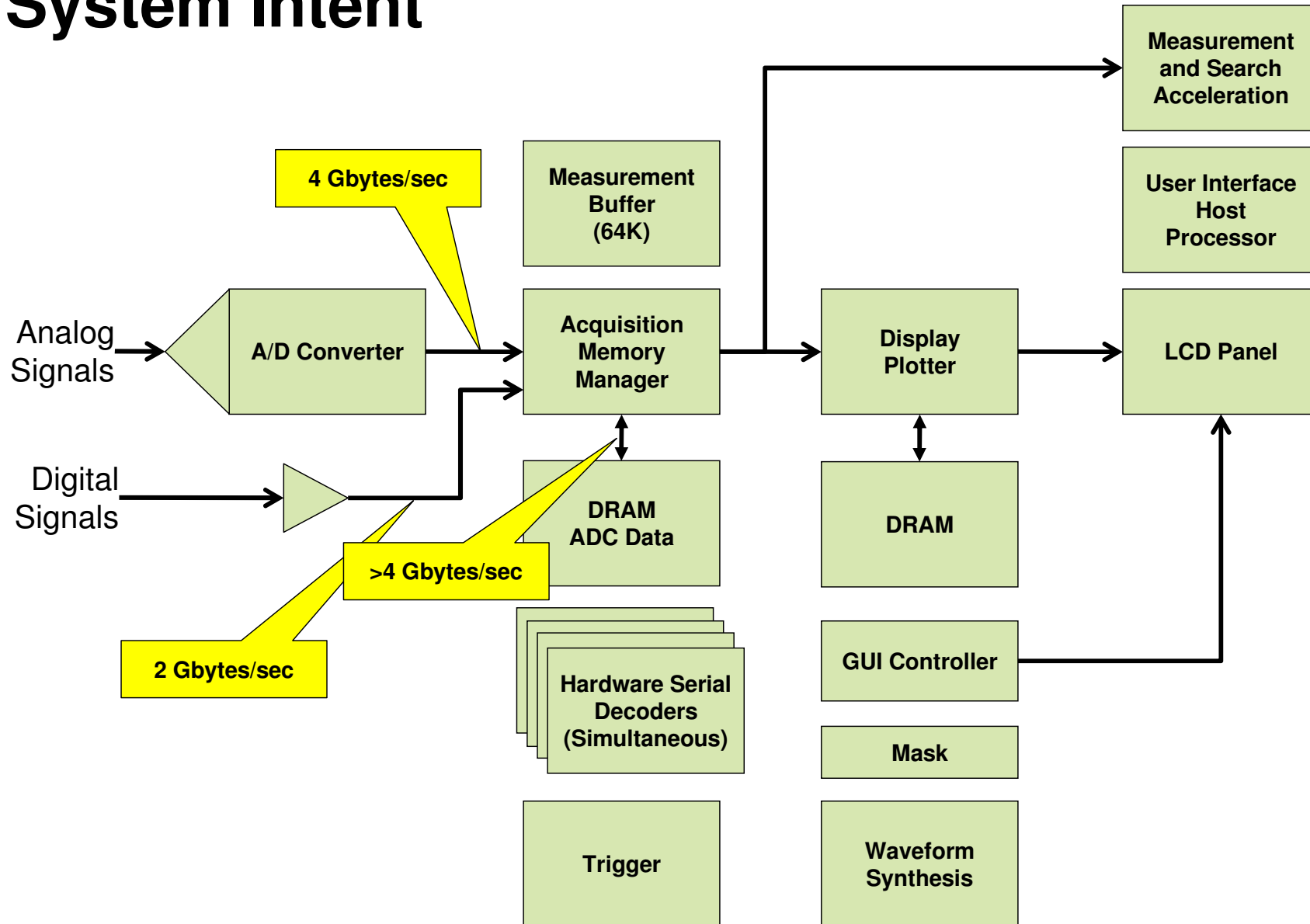


Diagram as published in EE Times



Agilent InfiniiVision 2000/3000 DSO/MSO System Intent

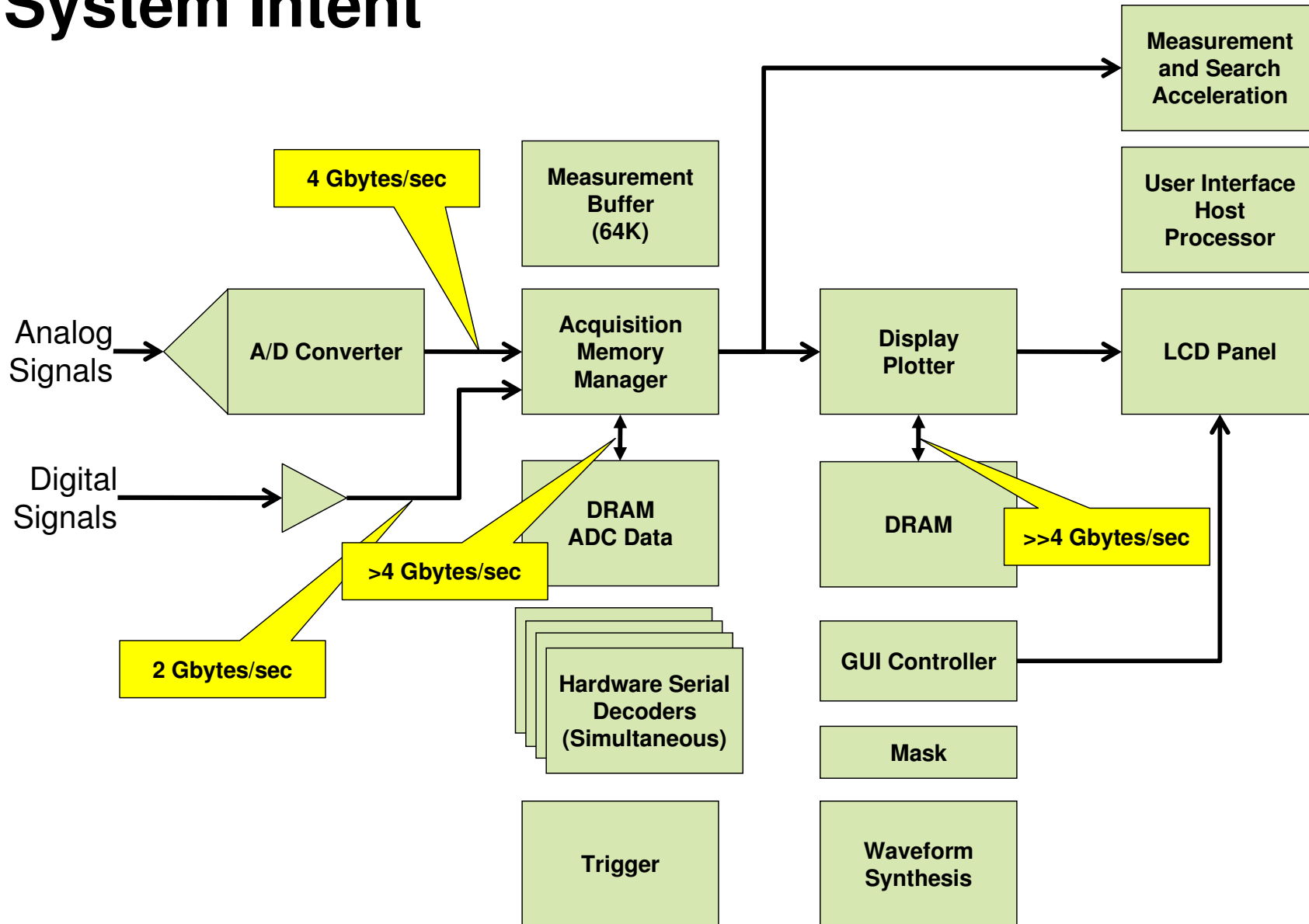


Diagram as published in EE Times



Agilent InfiniiVision 2000/3000 DSO/MSO System Partitioning

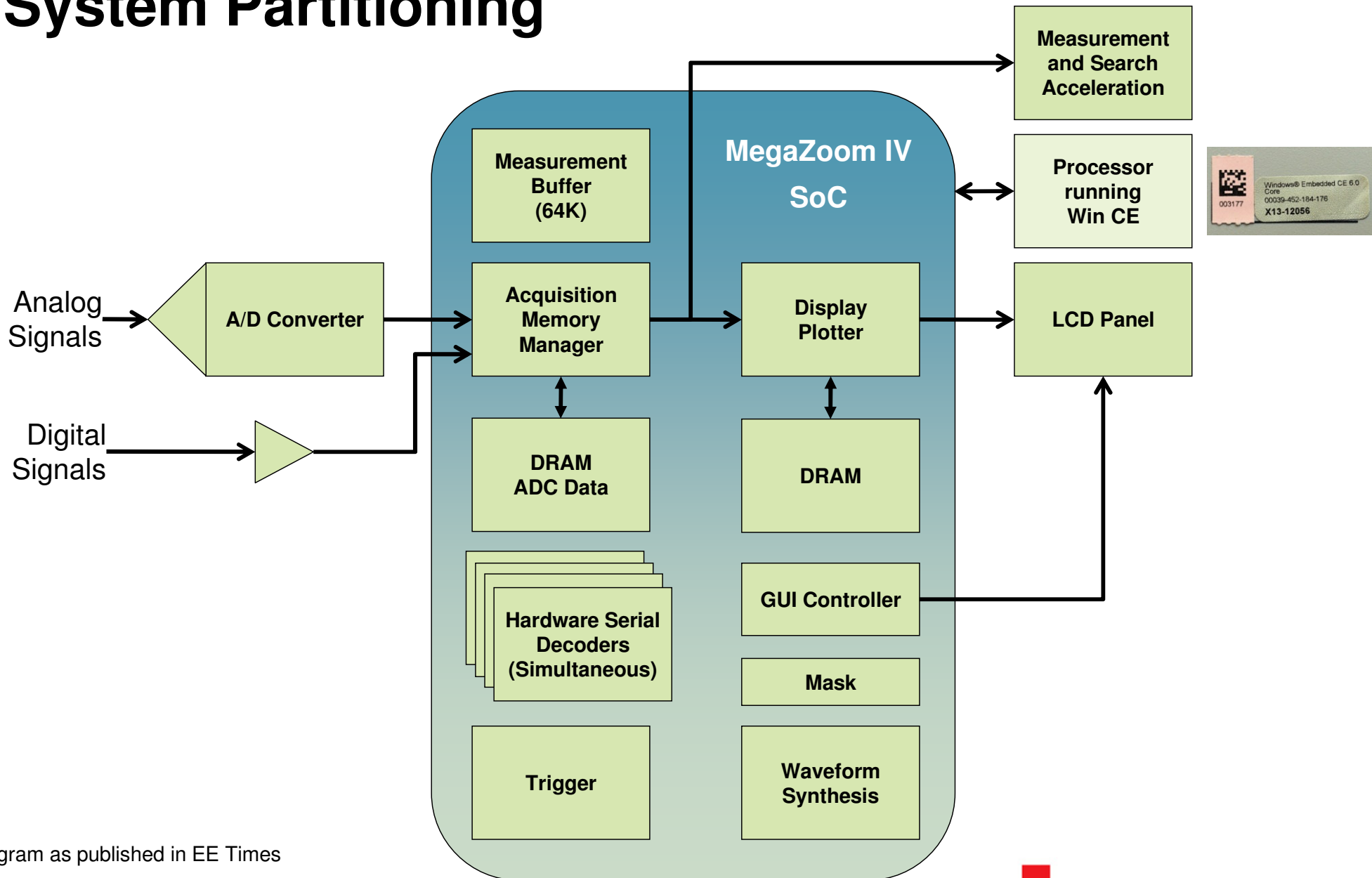


Diagram as published in EE Times

Agilent InfiniiVision 2000/3000 DSO/MSO System Partitioning

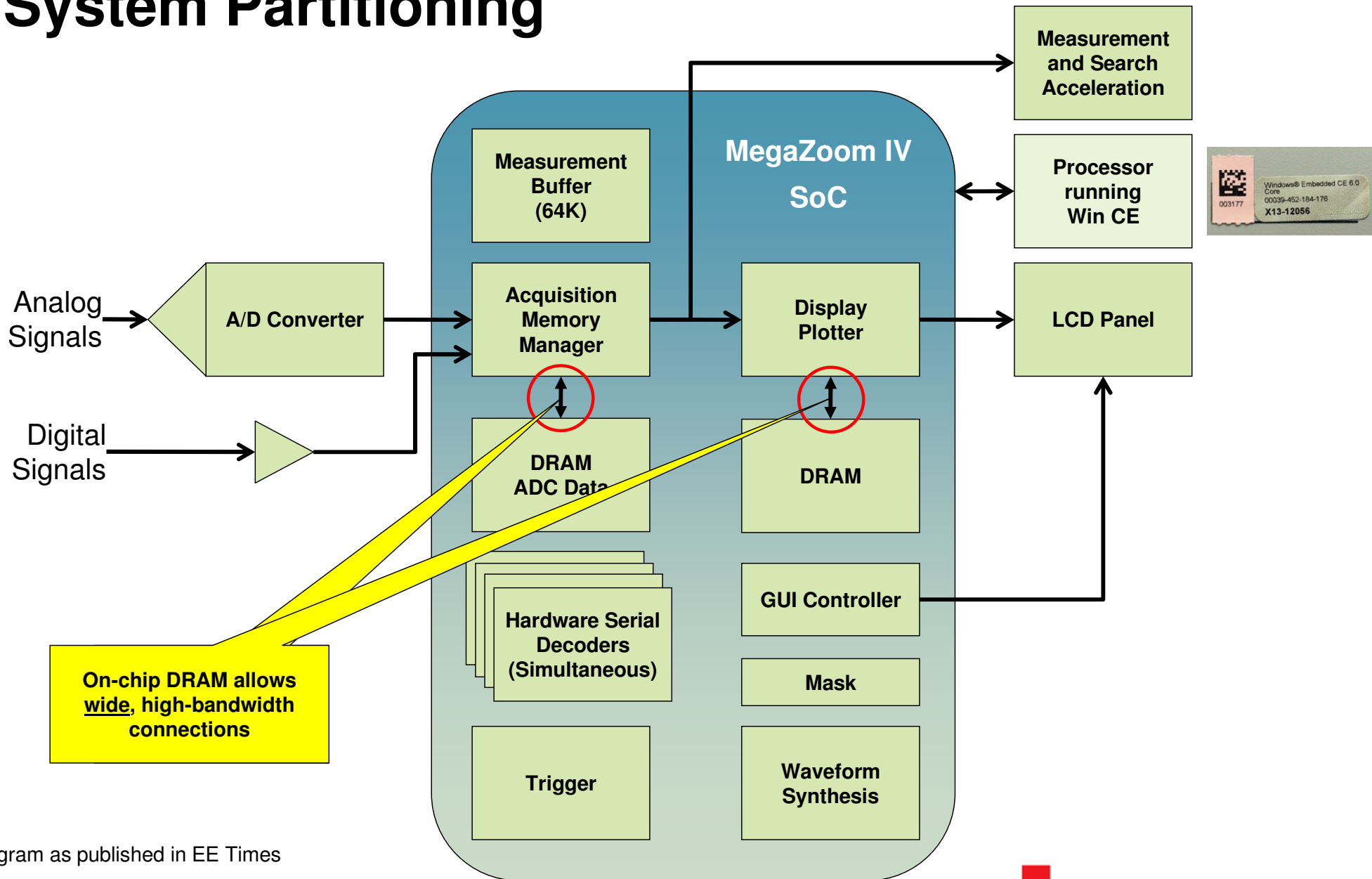
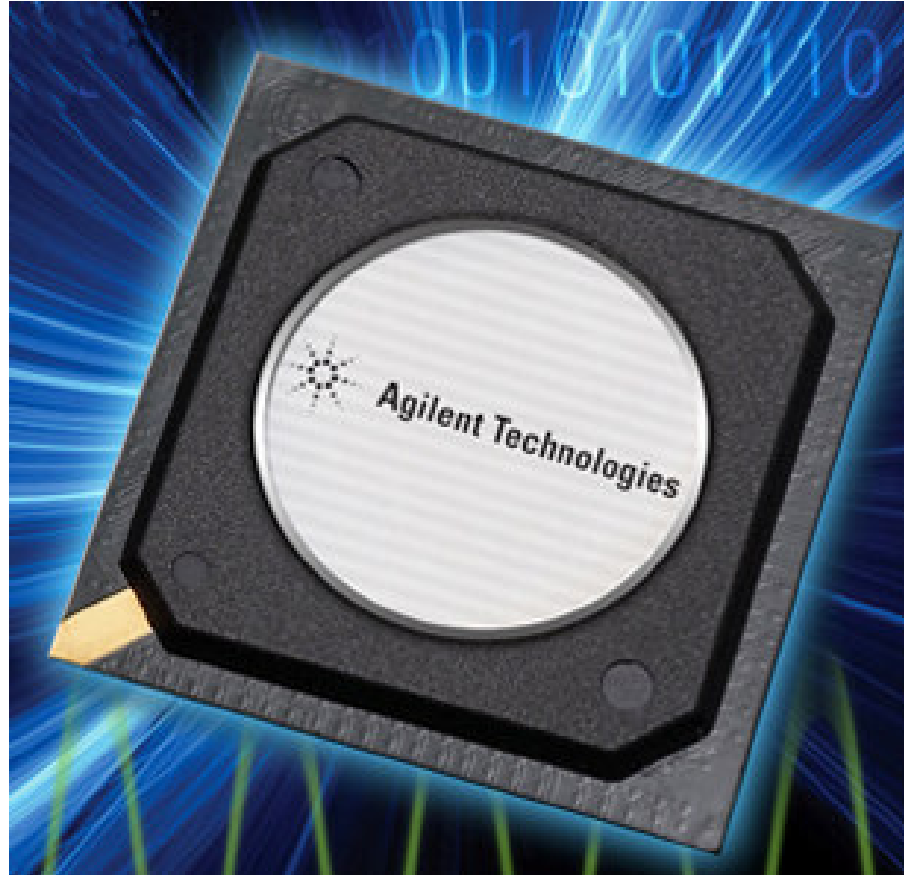


Diagram as published in EE Times

Agilent MegaZoom IV SoC



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Agilent InfiniiVision 2000 X-Series DSO Circuit Board

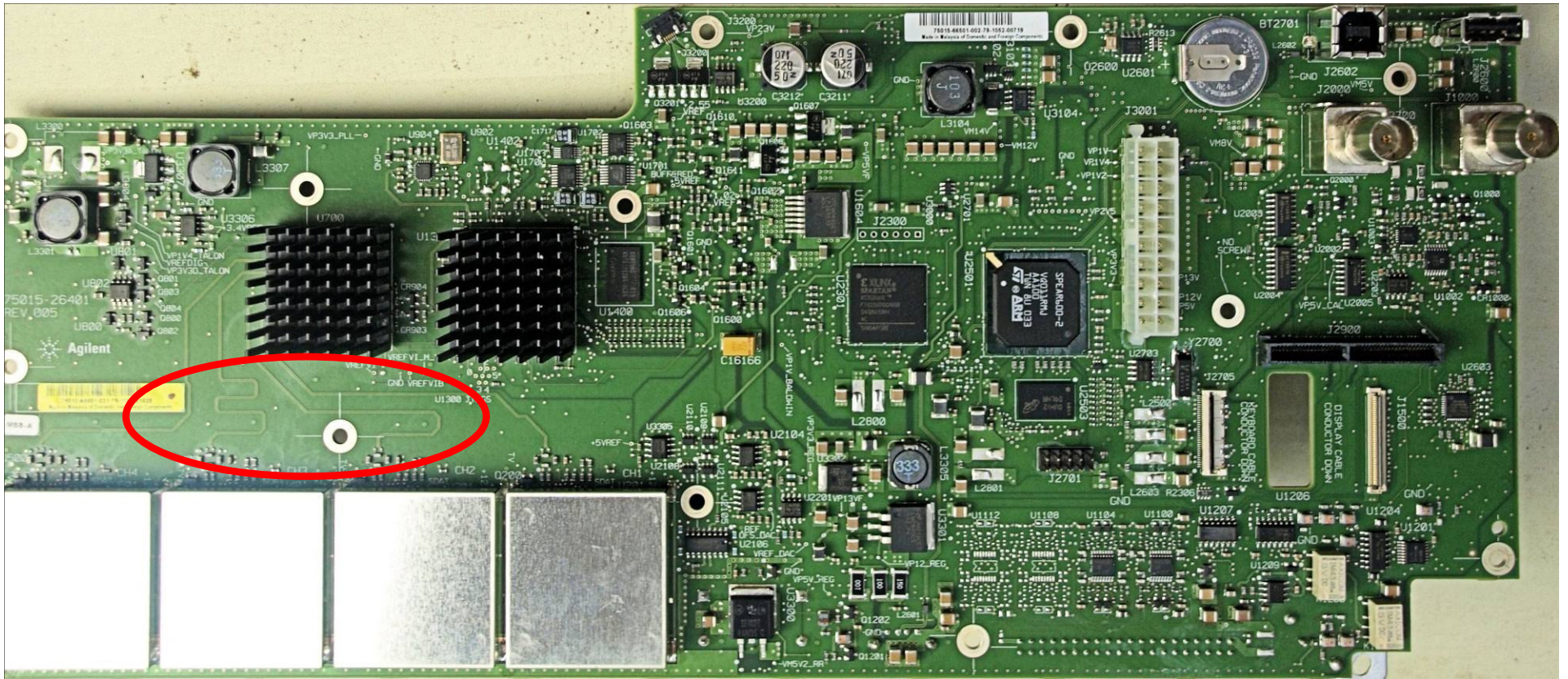
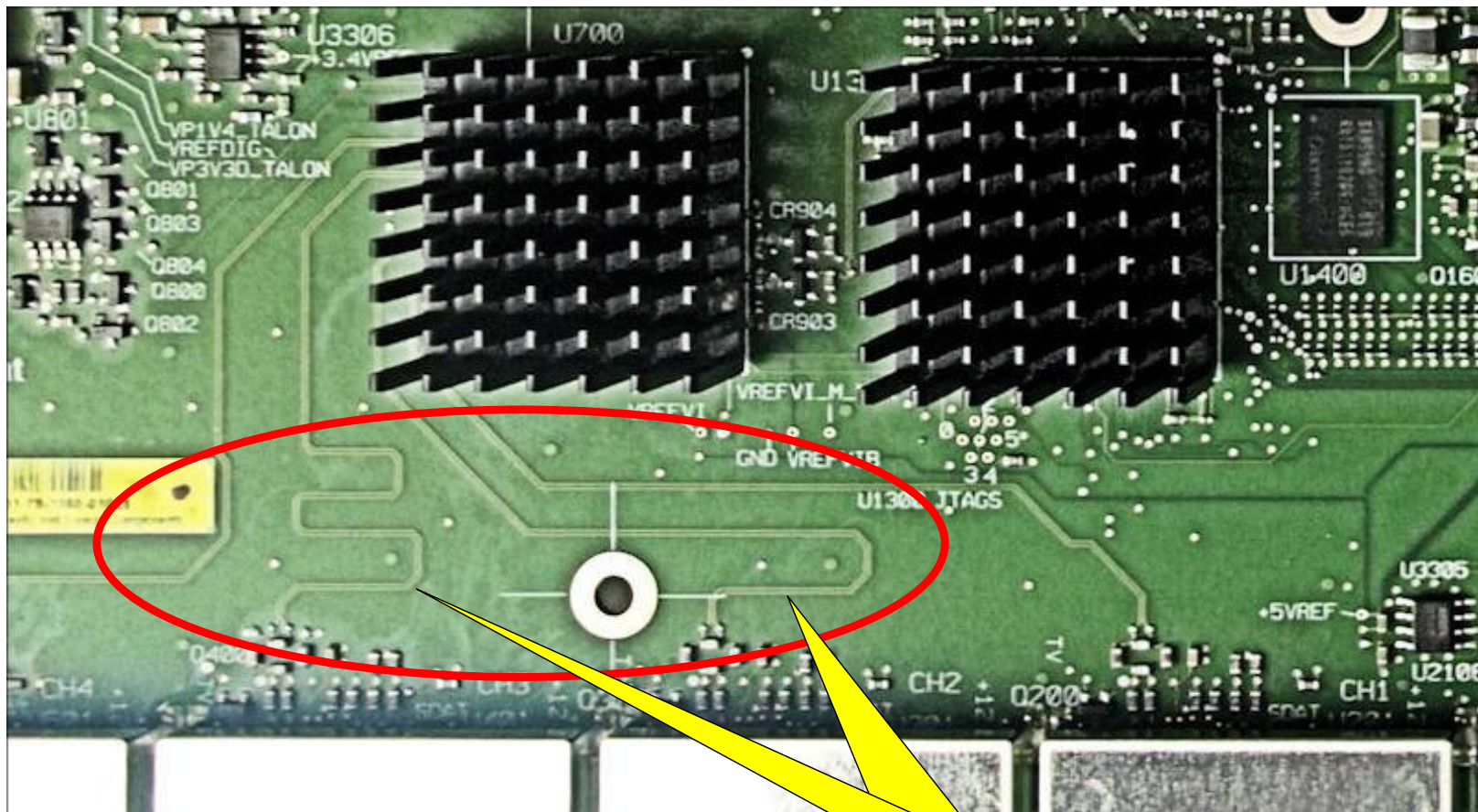


Image courtesy of David Jones, www.eevblog.com



Detail: Board-Level Design Intent



Differential-pair serpentine traces ensure that all analog inputs reach the ADC simultaneously

Image courtesy of David Jones, www.eevblog.com

Agilent InfiniiVision 2000 X-Series DSO Circuit Board

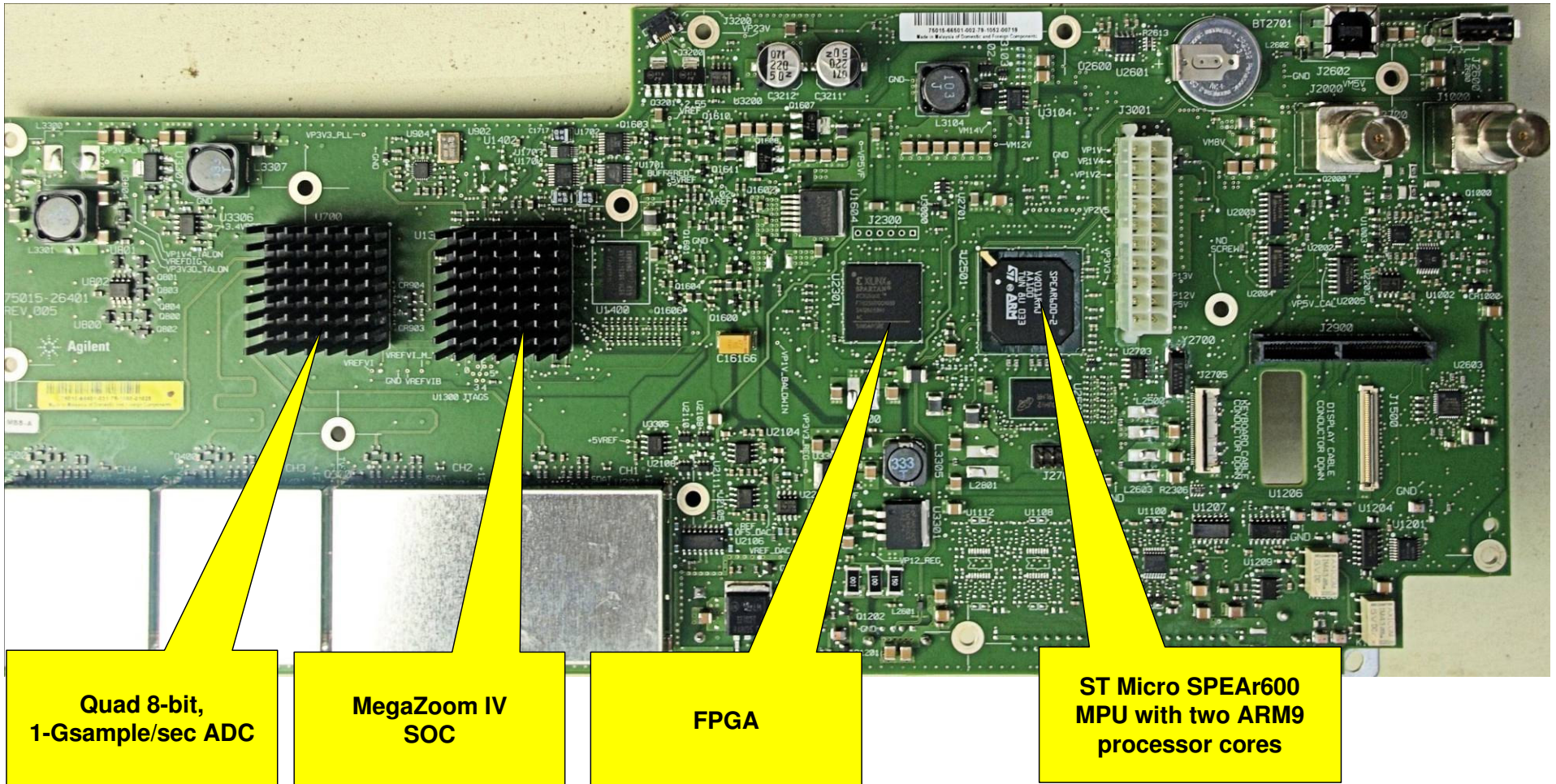
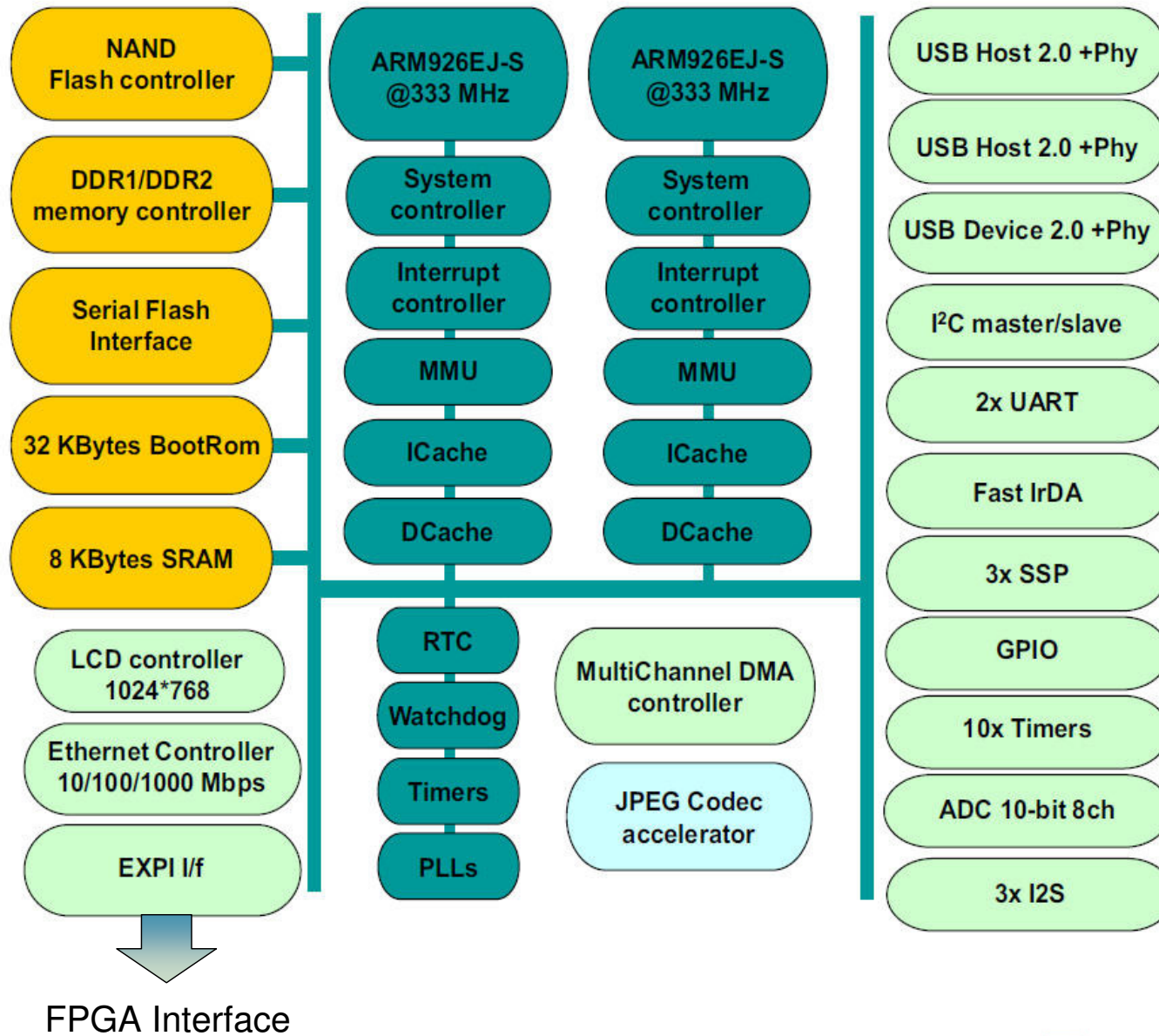


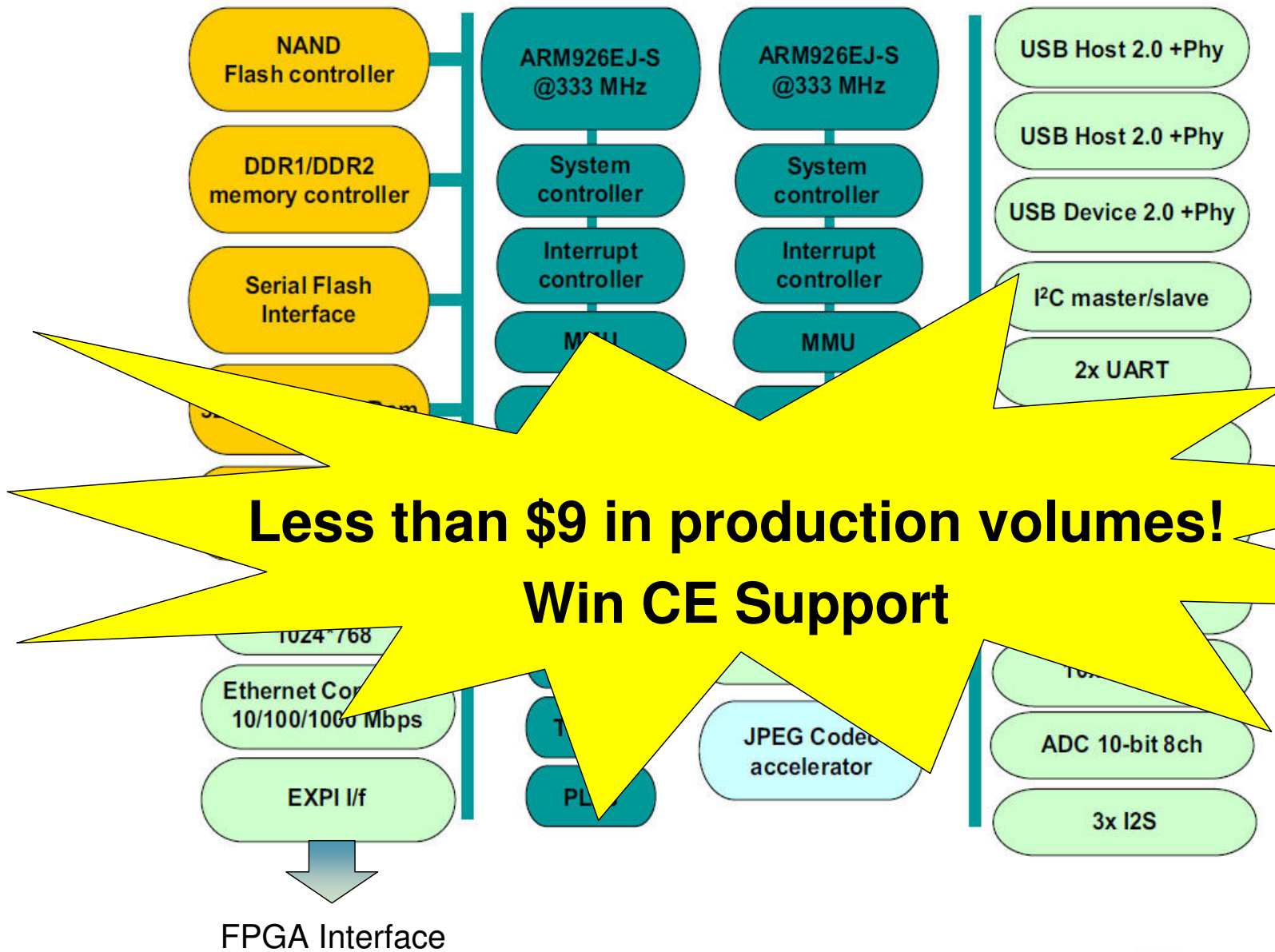
Image courtesy of David Jones, www.eevblog.com



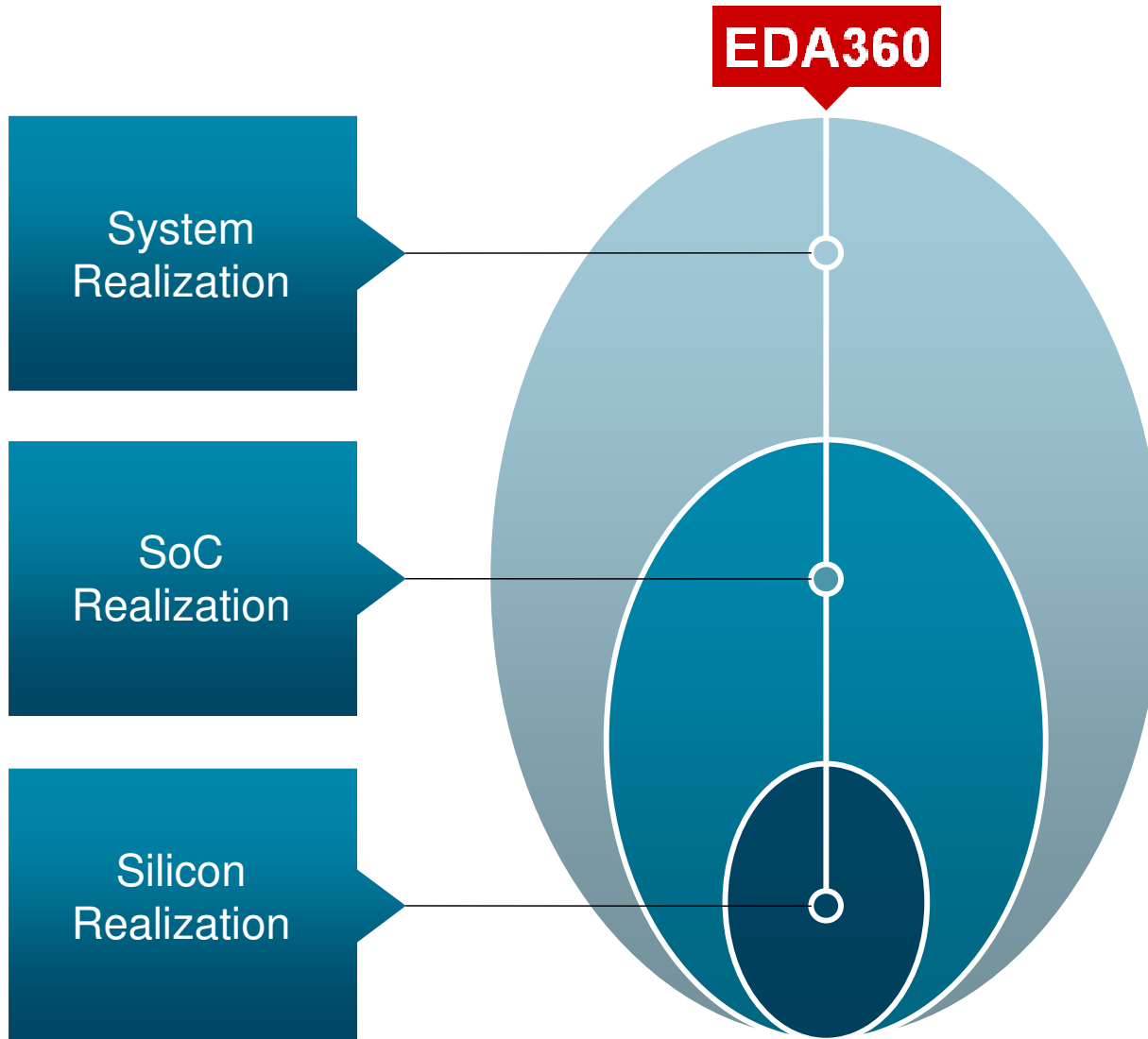
ST Microelectronics SPEAr600 Block Diagram



Why use an ST Micro SPEAr600?



Three Key Pillars of EDA360



NAND Flash controller	ARM926EJ-S @333 MHz	ARM926EJ-S @333 MHz	USB Host 2.0 +Pty
DDR1/DDR2 memory controller	System controller	System controller	USB Host 2.0 +Pty
Serial Flash Interface	Interrupt controller	Interrupt controller	USB Device 2.0 +Pty
32 Kbytes BootRom	MMU	MMU	PC master/slave
8 Kbytes SRAM	ICache	ICache	2x UART
LCD controller 1024*768	DCache	DCache	Fast I/OA
Ethernet Controller 10/100/1000 Mbps	RTC	MultiChannel DMA controller	2x SSP
EXPI I/F	Watchdog	JPEG Codec accelerator	GPIO
	Timers		16x Timers
	PLLs		ADC 10-bit 8ch
			3x I2S





Questions and Answers





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