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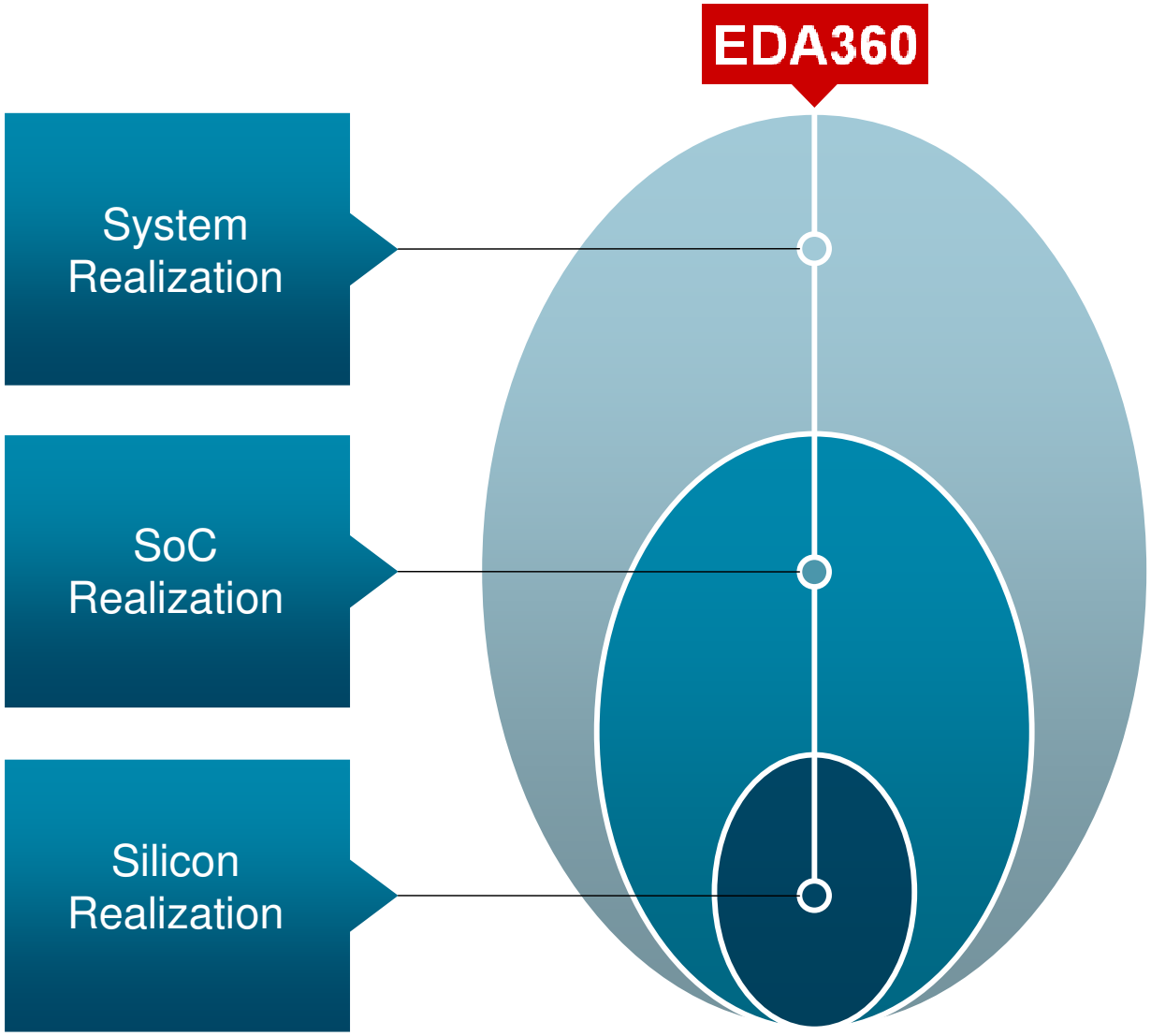
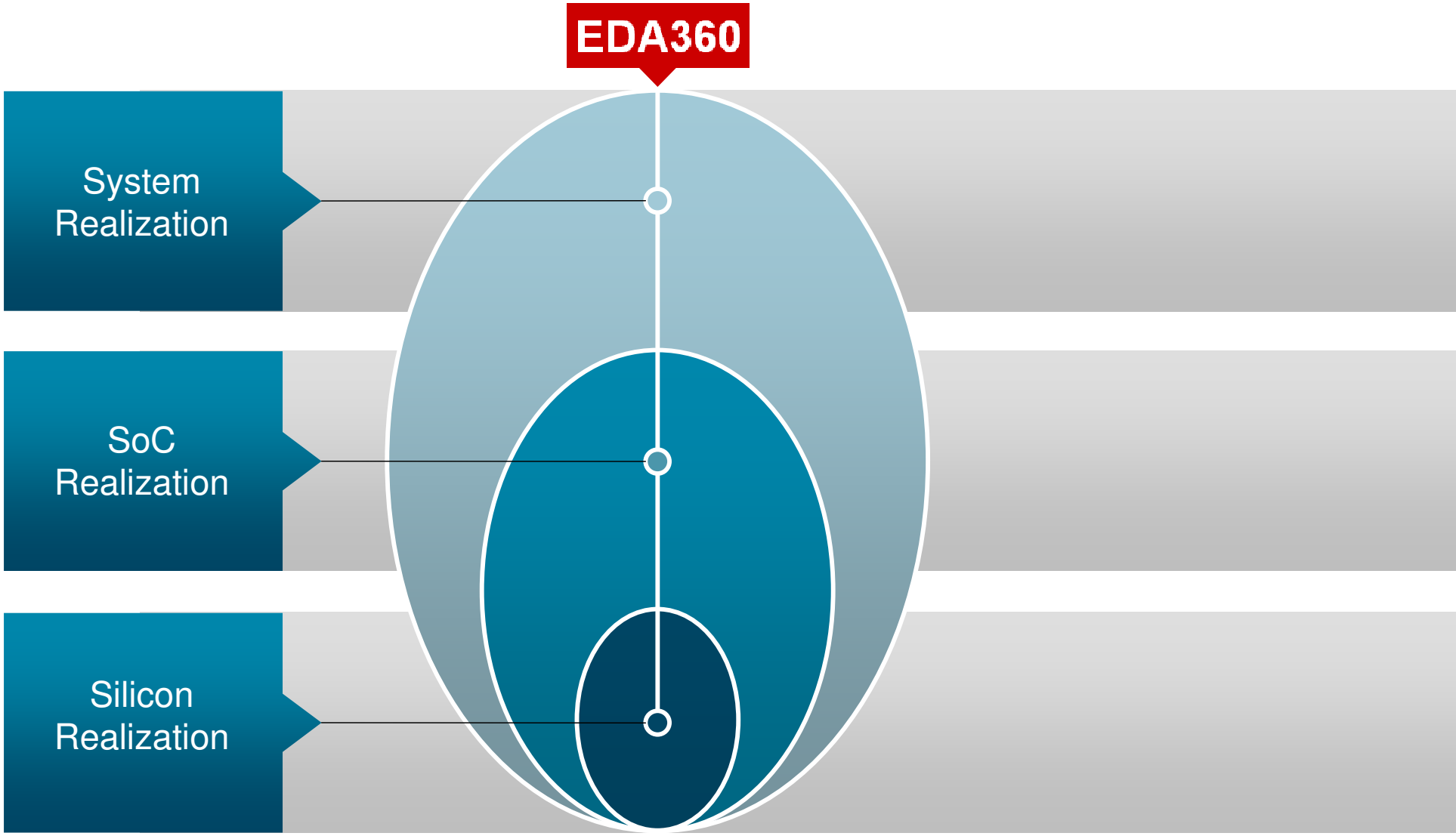
EDA360 - Is End-to-End Design a Riddle, a Rebus, or a Reality?

April 7, 2011

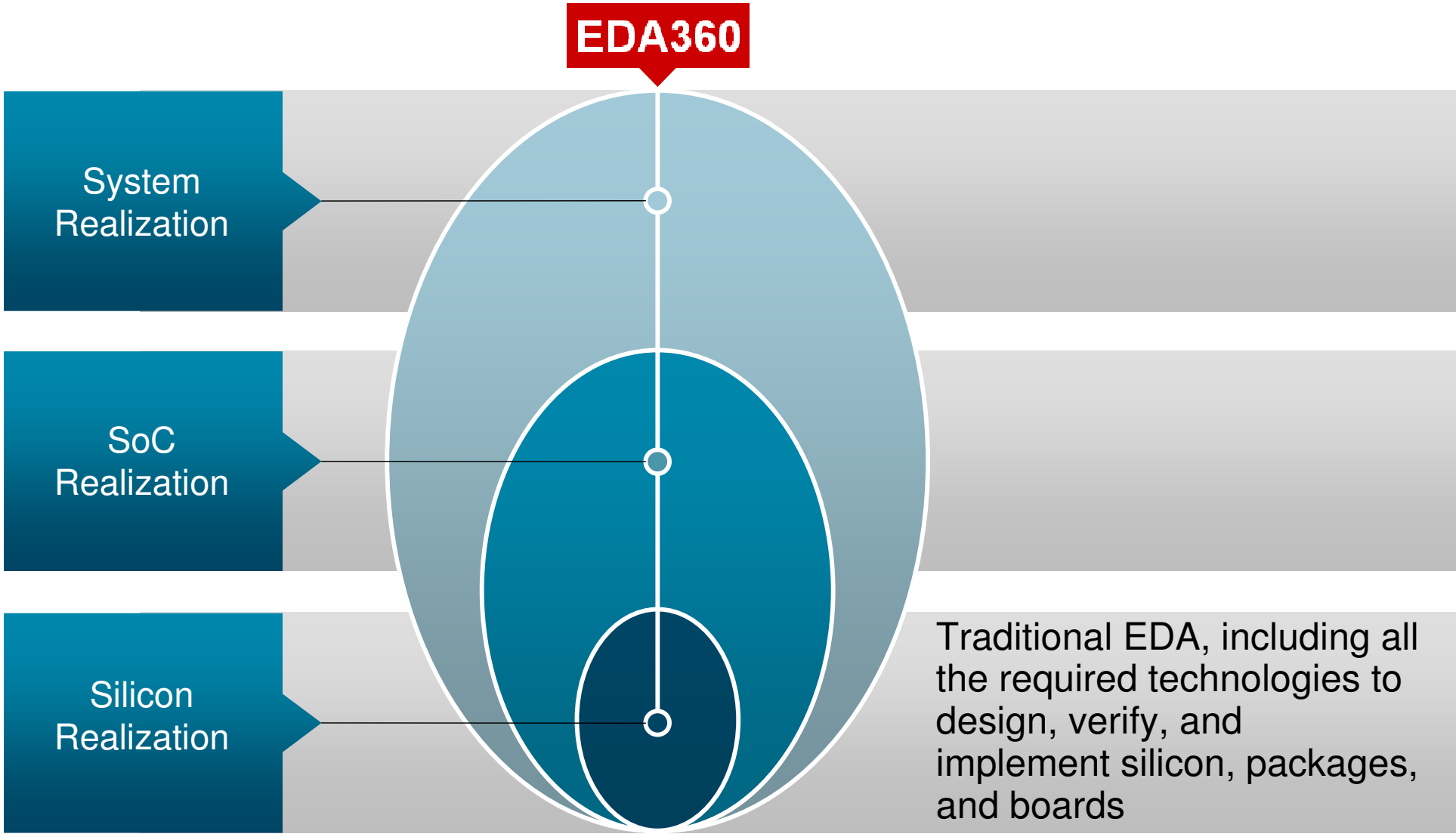
Three Key Pillars of EDA360



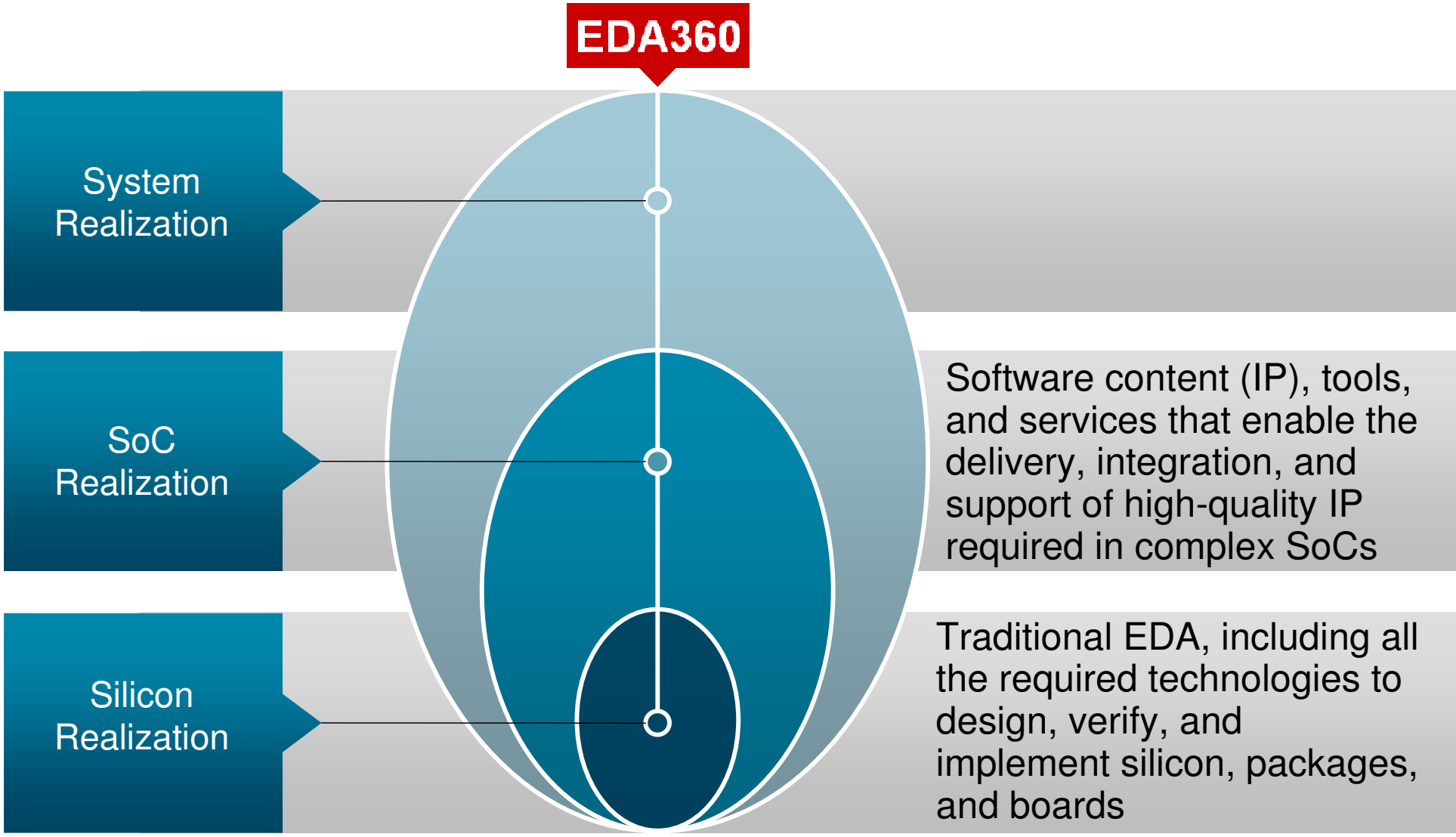
Three Key Pillars of EDA360



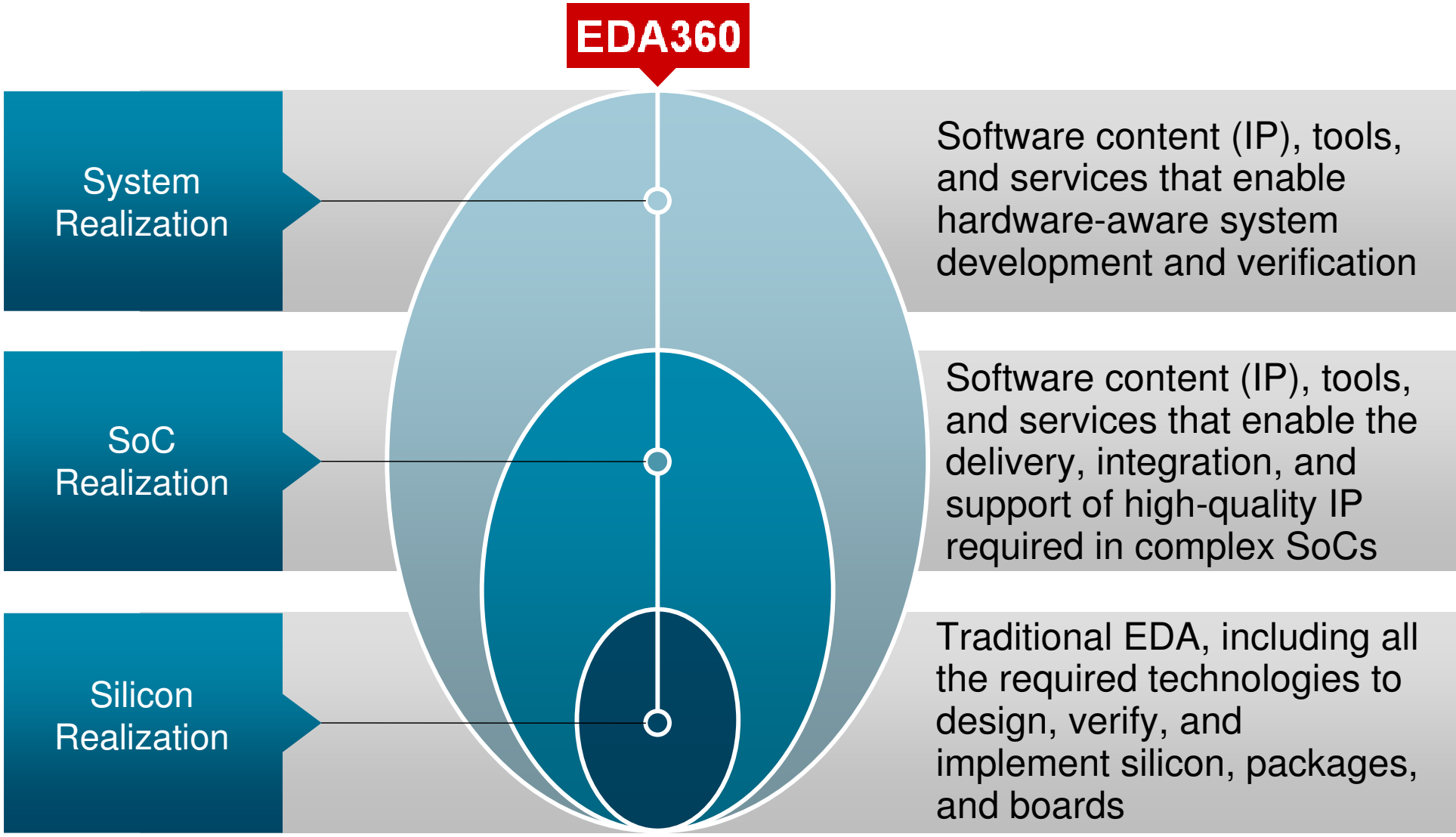
Three Key Pillars of EDA360



Three Key Pillars of EDA360

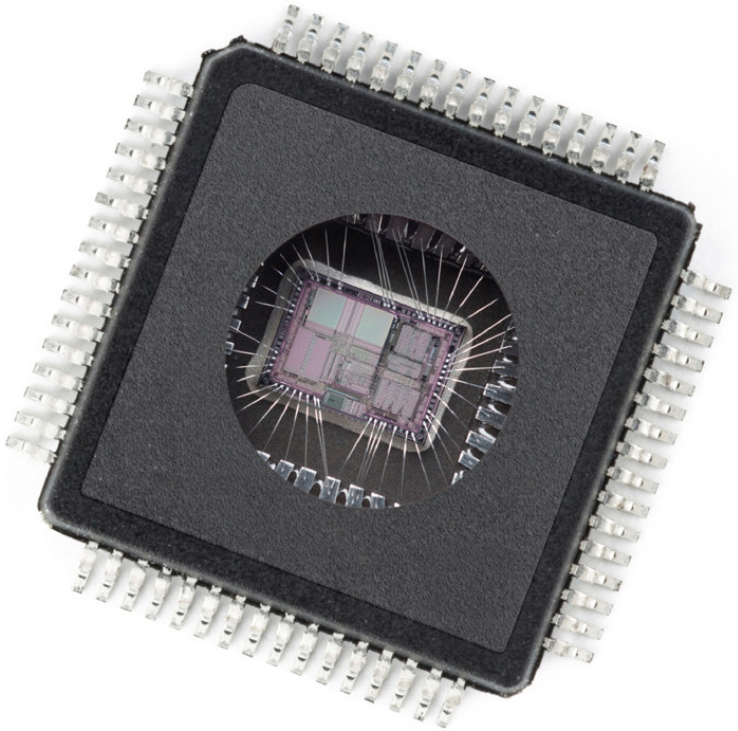


Three Key Pillars of EDA360



Silicon Realization – Customer Challenges

- Time to market
  - Disaggregated, global design chain limits visibility and predictability for complex designs – causing schedule delays and respins
  - Lack of true holistic and integrated silicon-package-board flows causes productivity gap
  - Reuse
- Profitability
  - Design failure catastrophic
  - Functionality, performance, and power improvements contribute to higher margins
  - Manufacturability

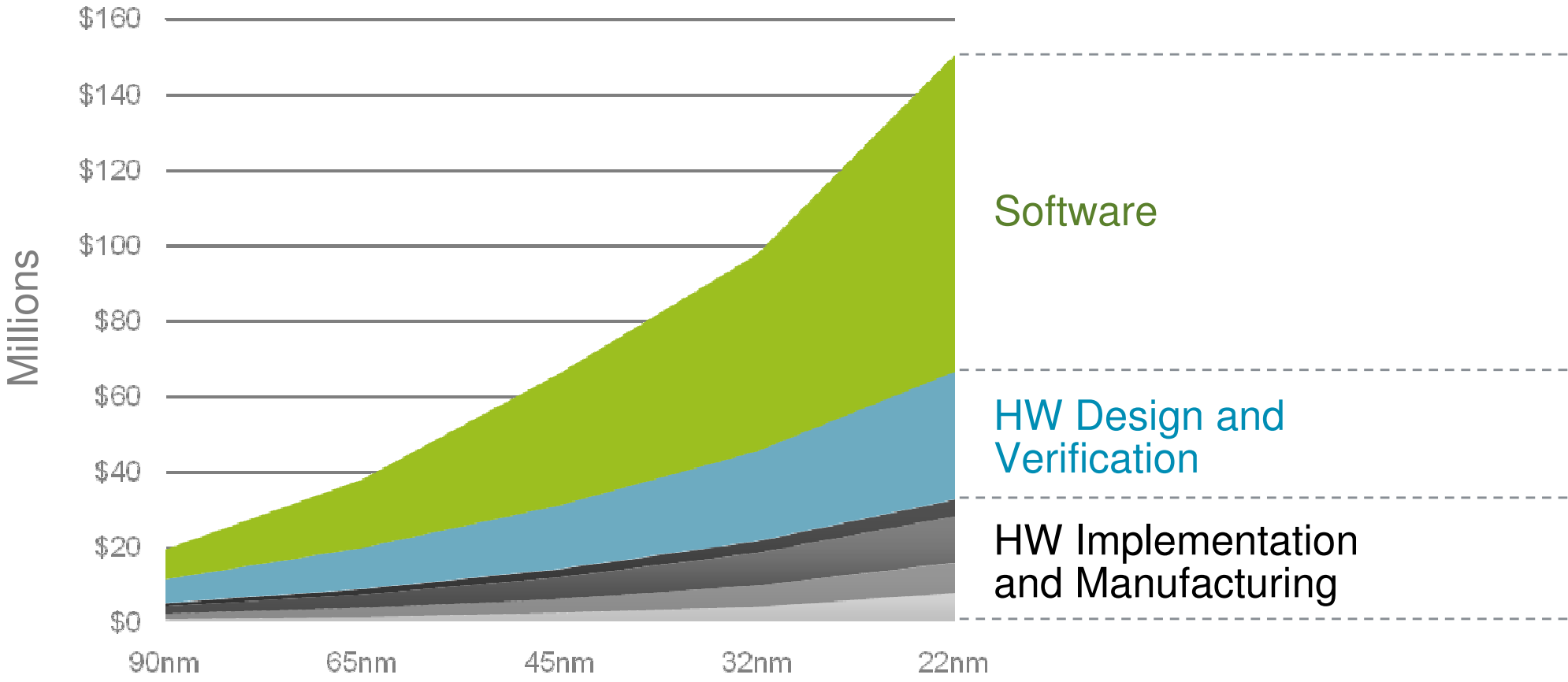


System Realization – Customer Challenges

- Software development trails hardware development, impacting time-to-market
- Hardware-software integration complexity impeding product shipments, quality
- Effective and predictable system and sub-system verification

System Realization – Market Landscape

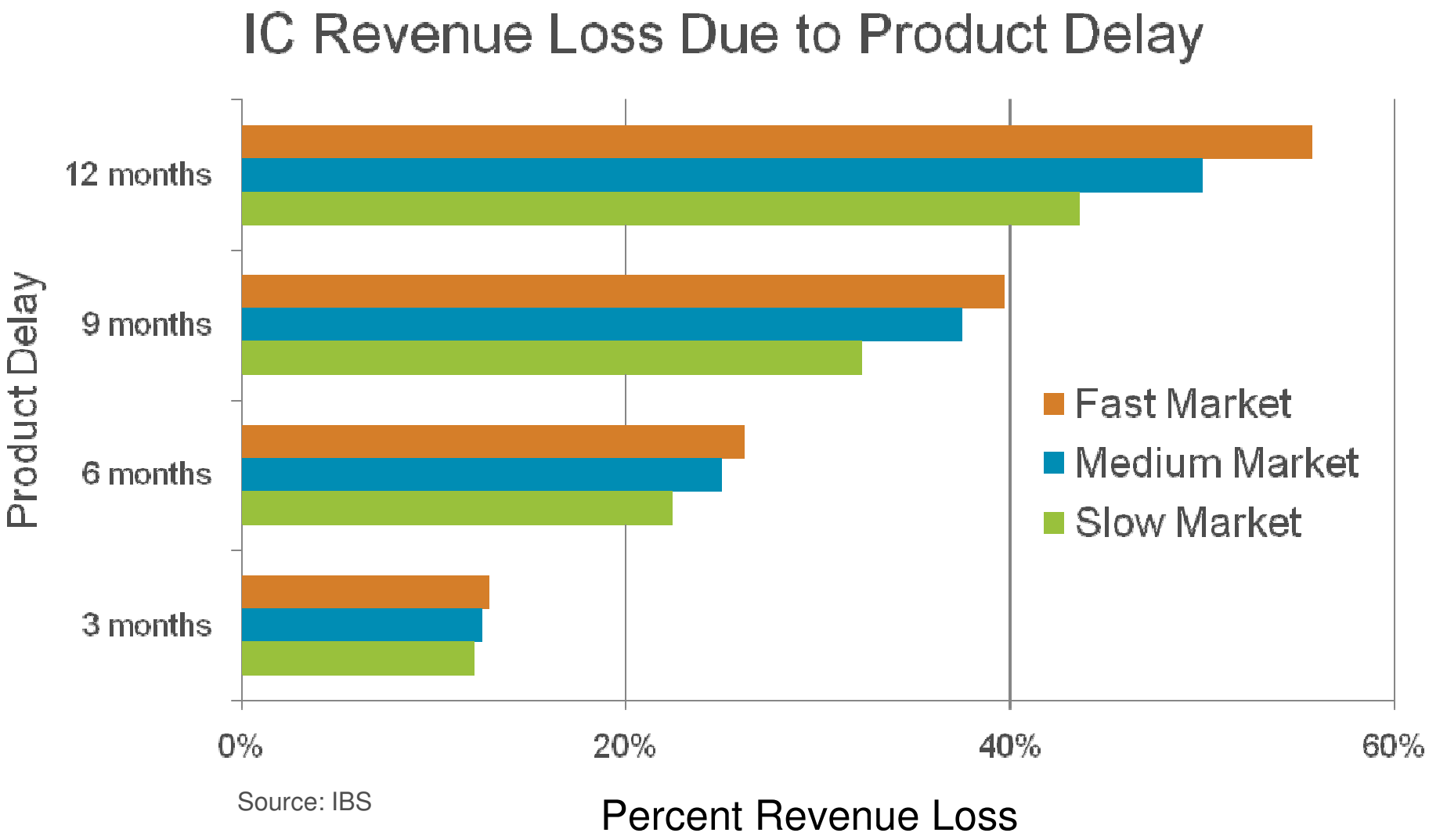
Development costs rising



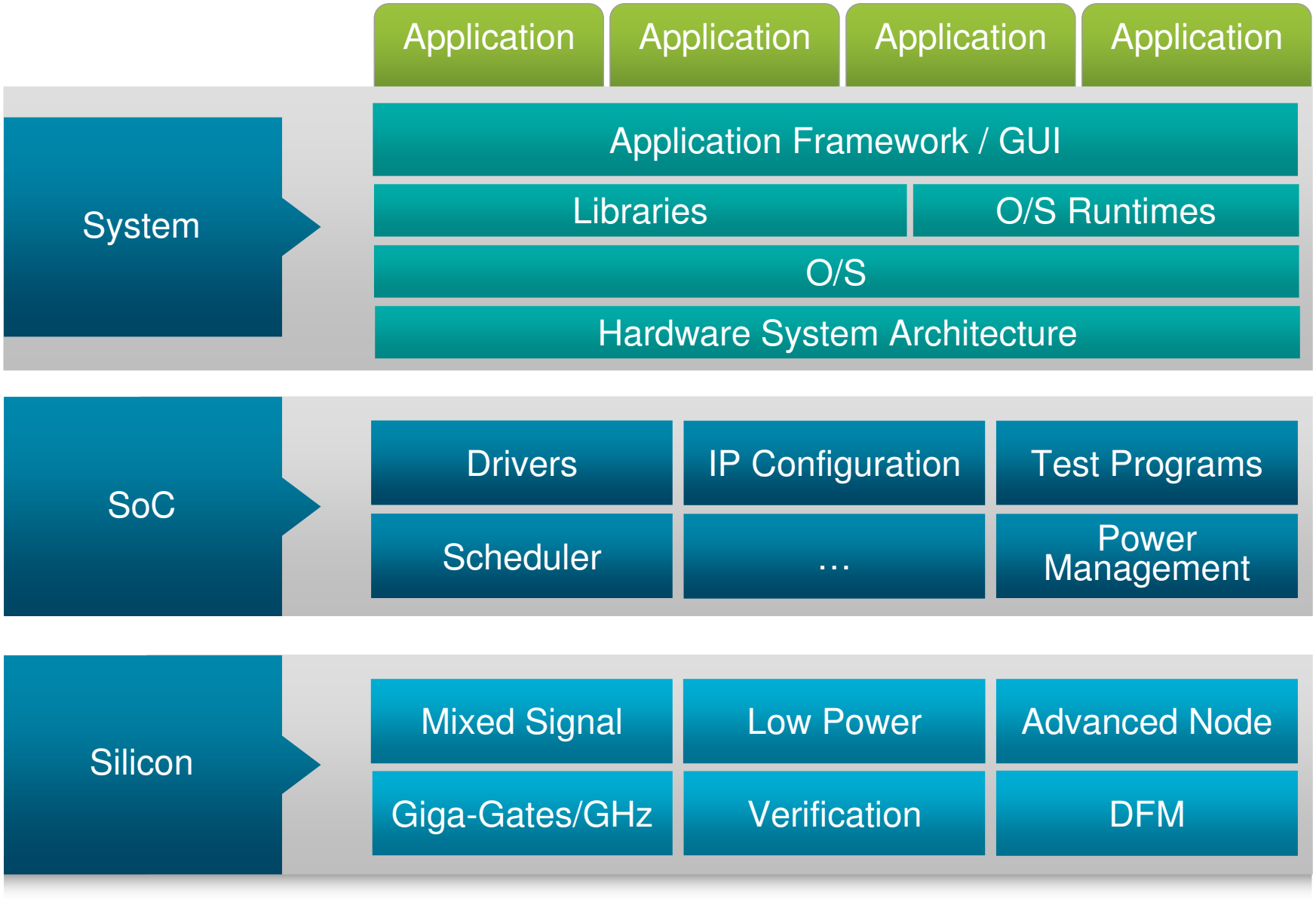
Source: IBS 2009

System Realization – Market Landscape

Market window shrinking; growing penalties for delay



Sample Challenges at Each Realization Layer



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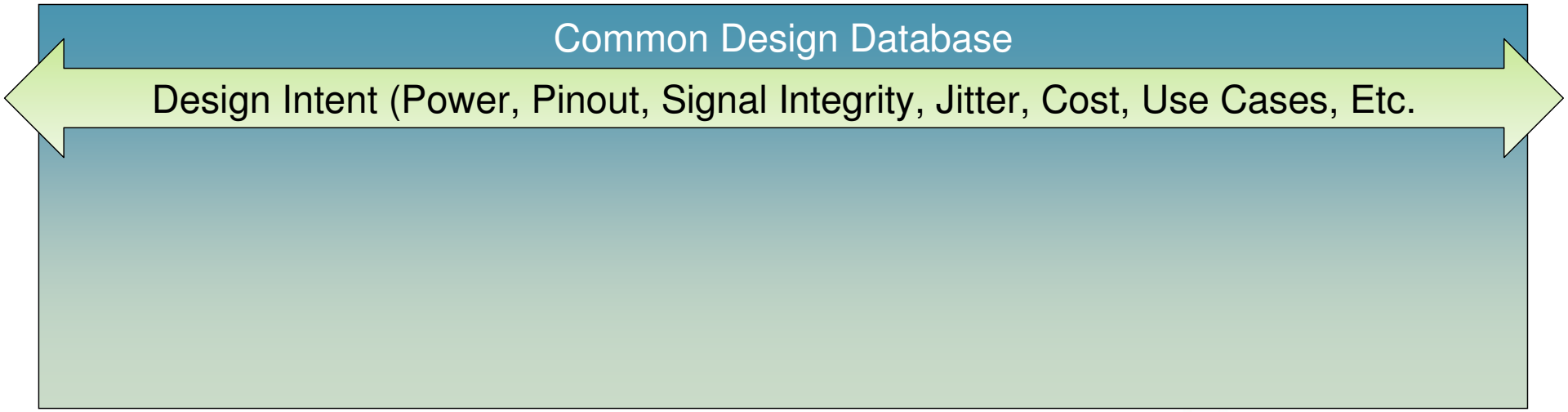

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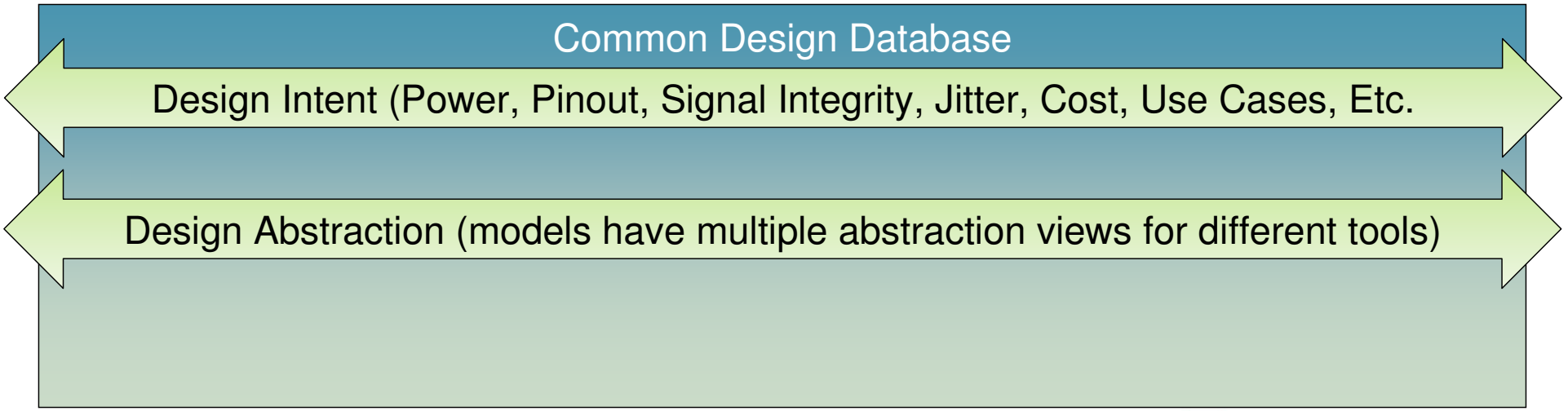

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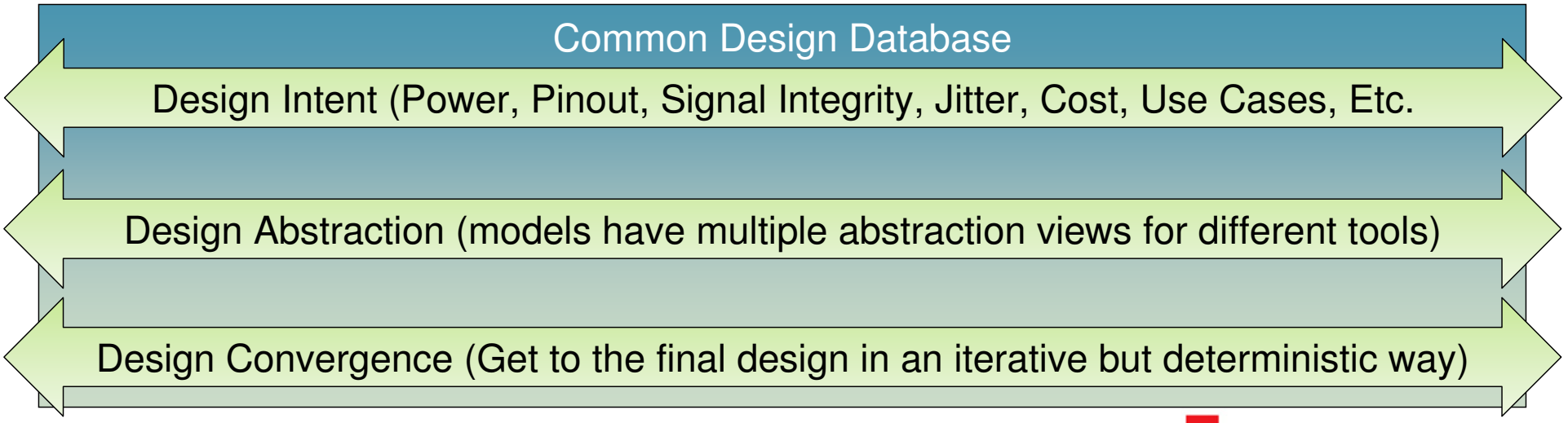

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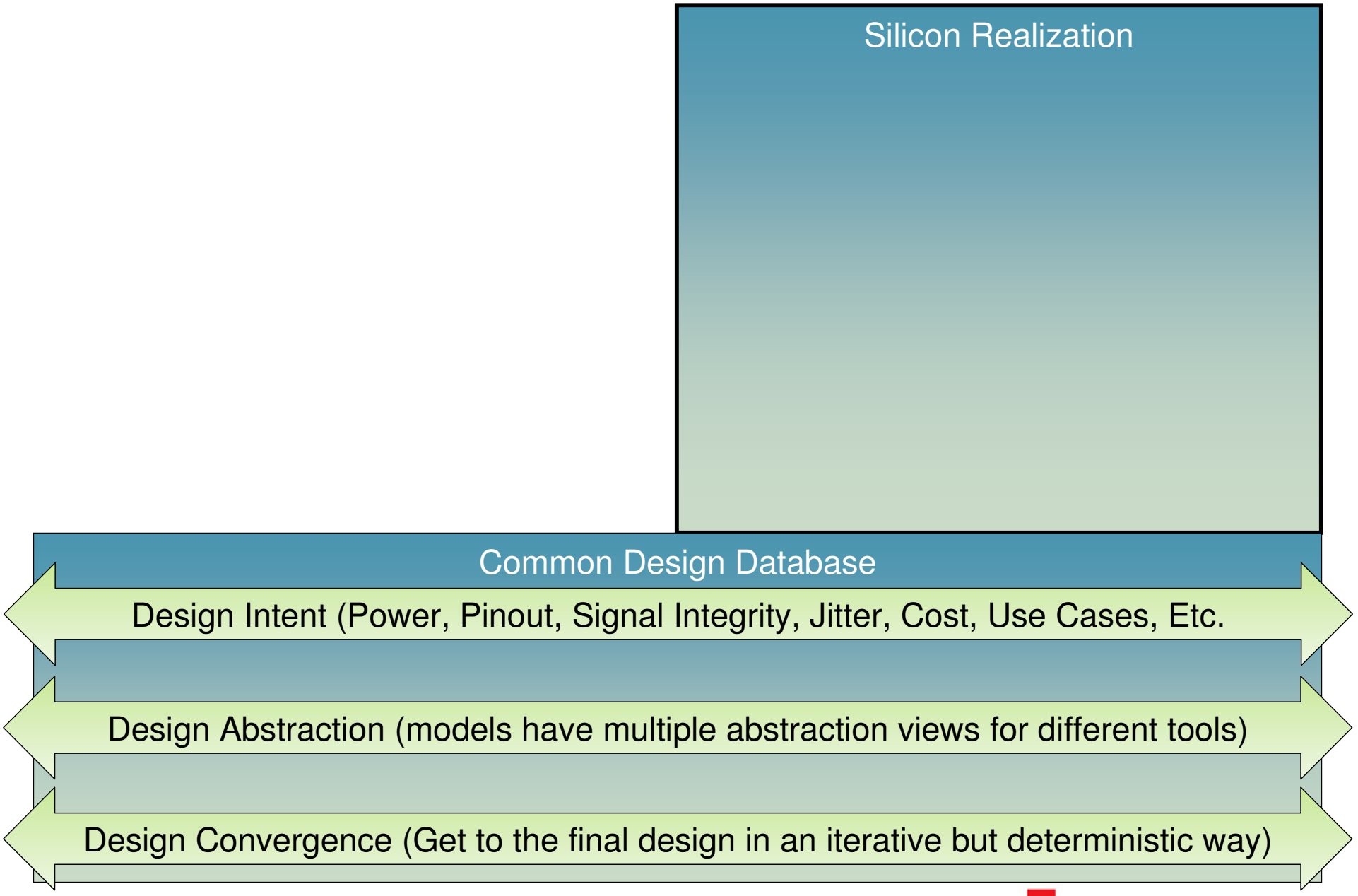

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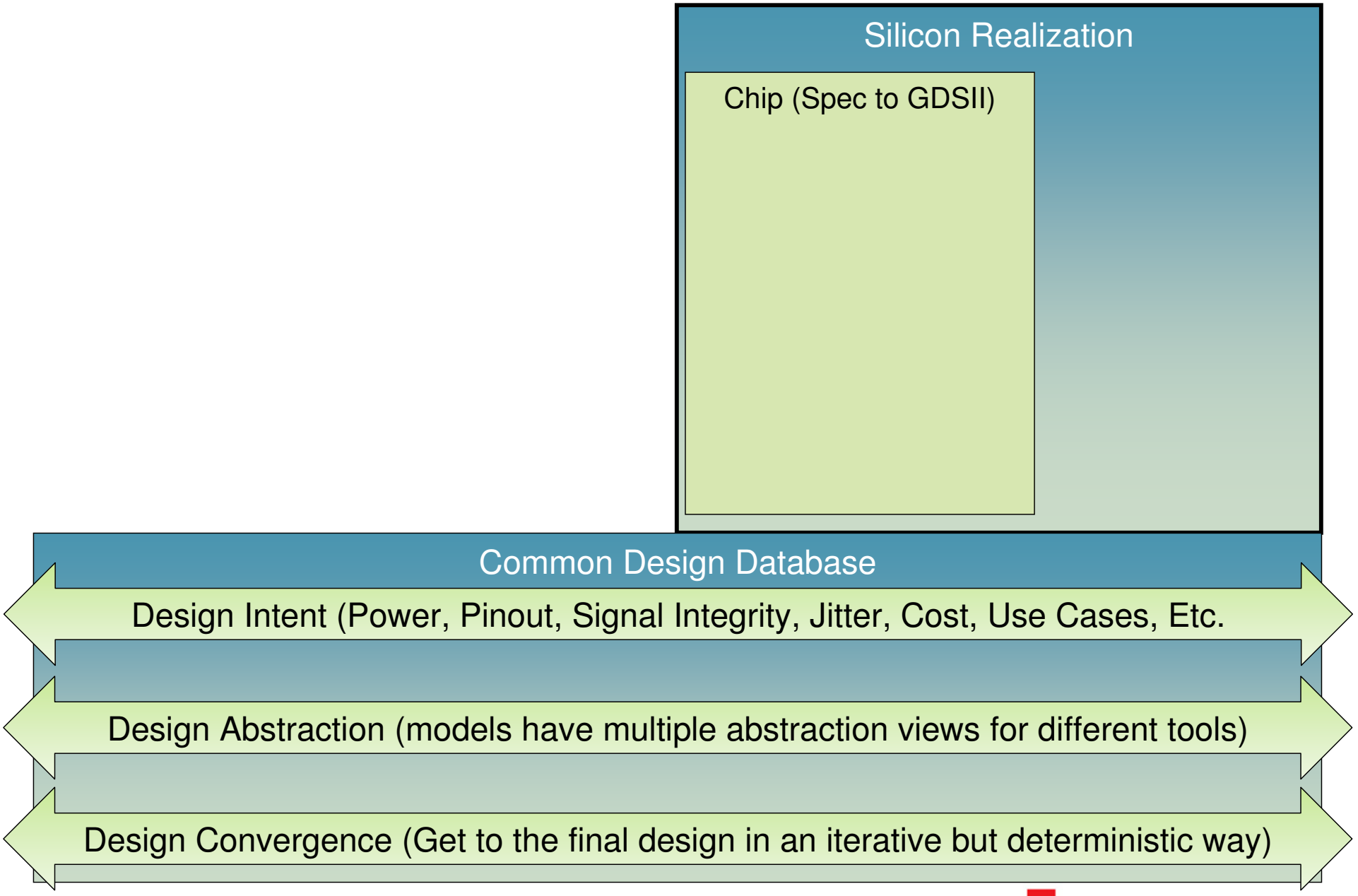

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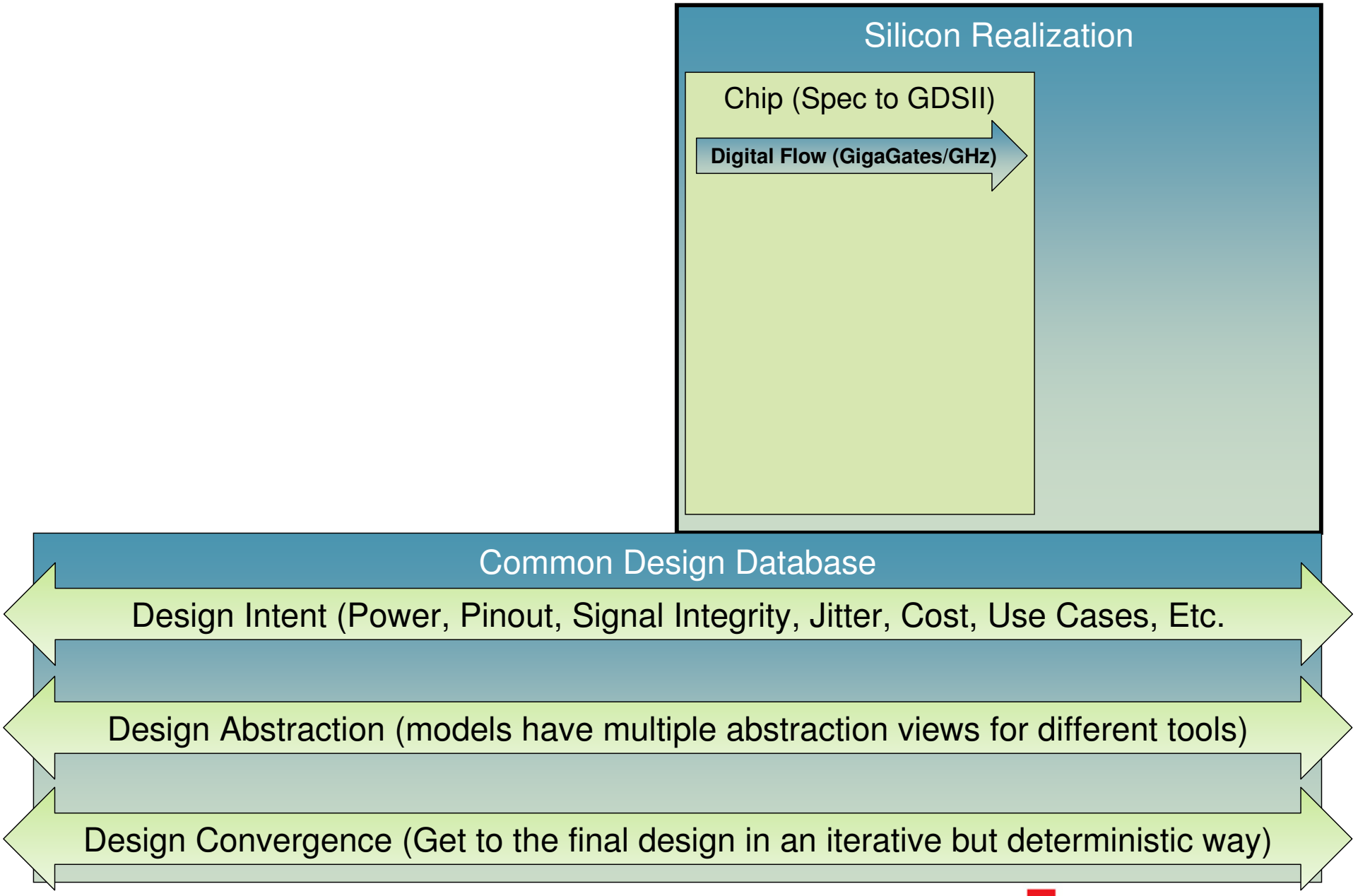

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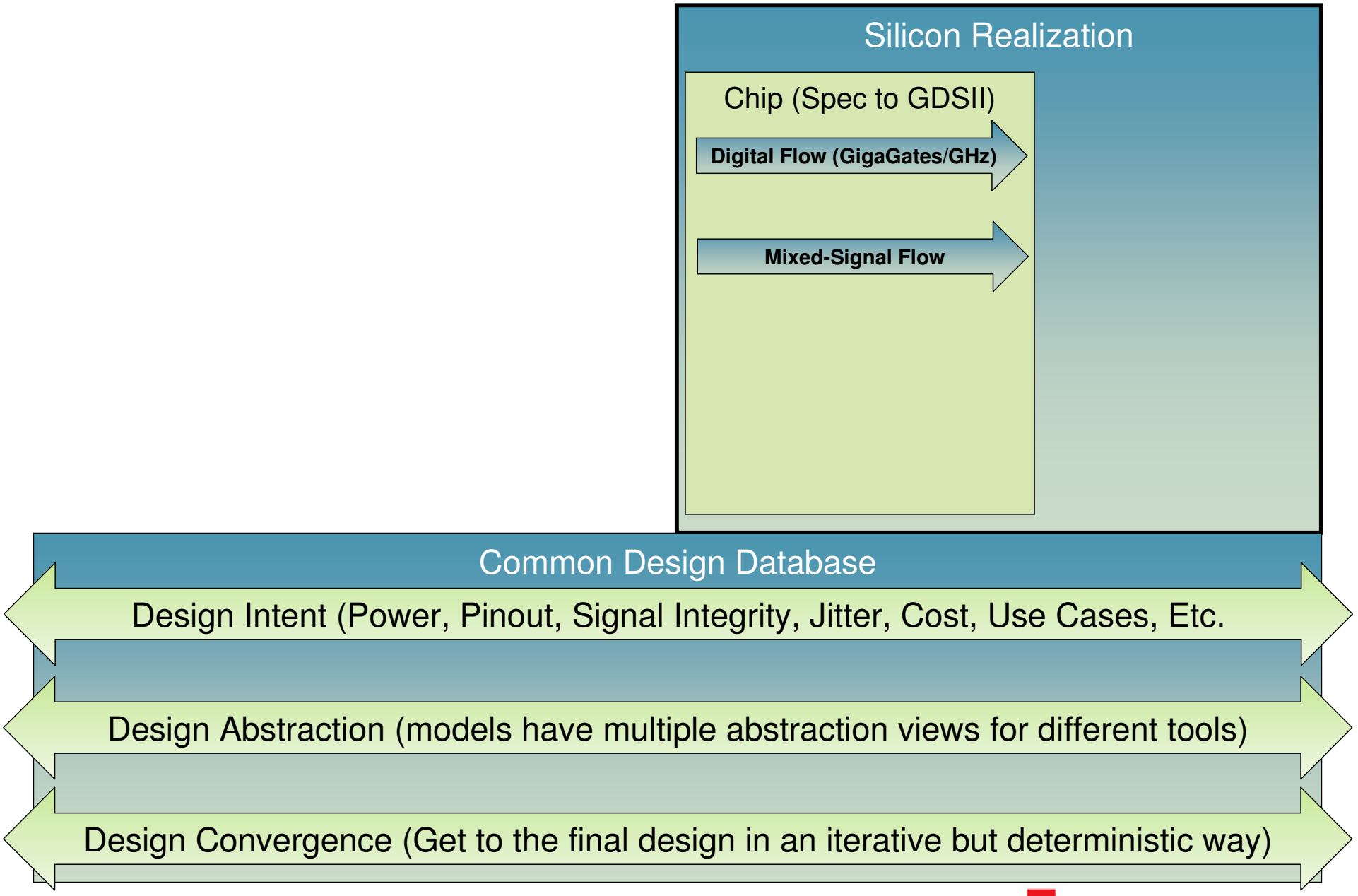

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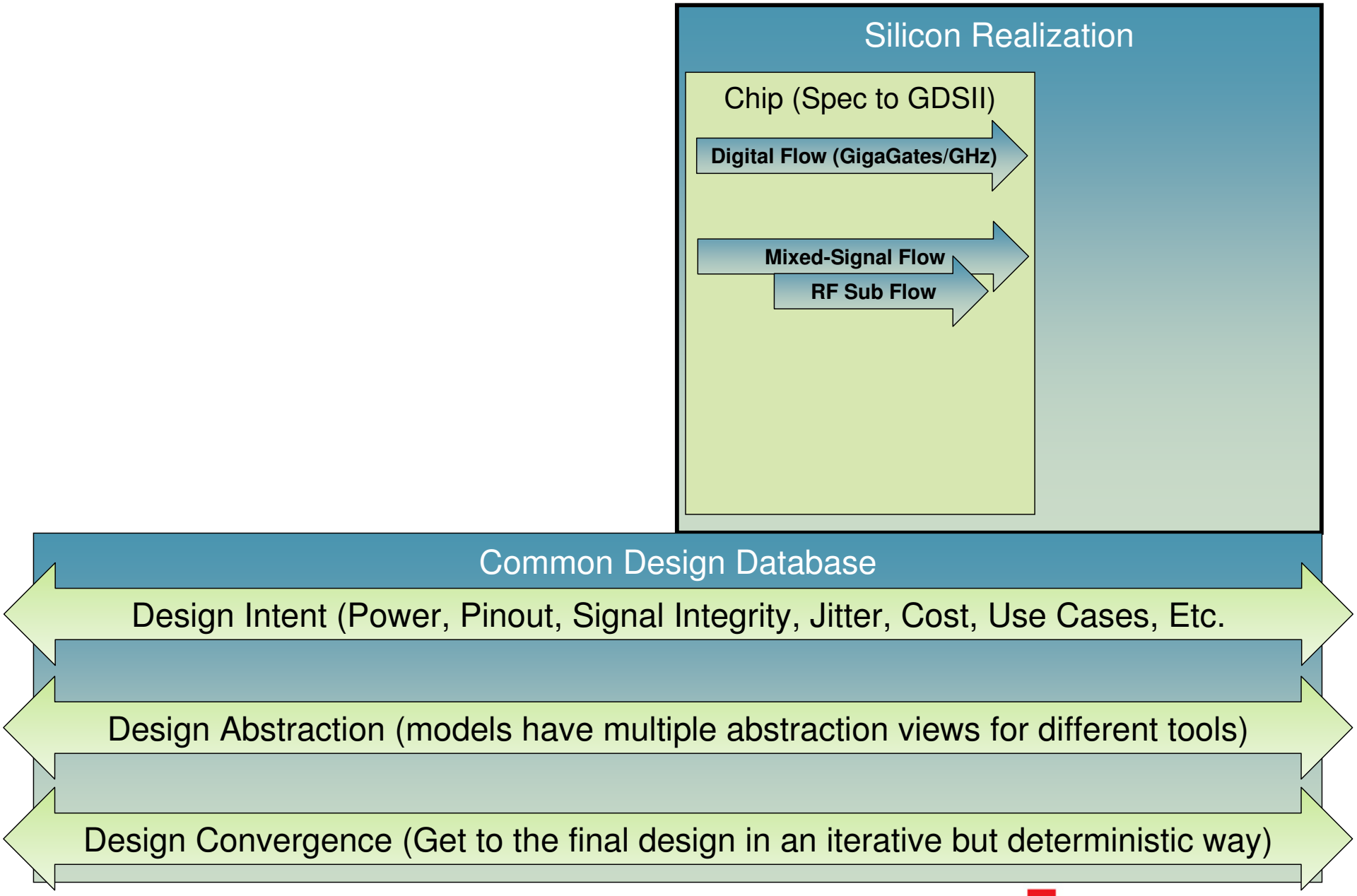

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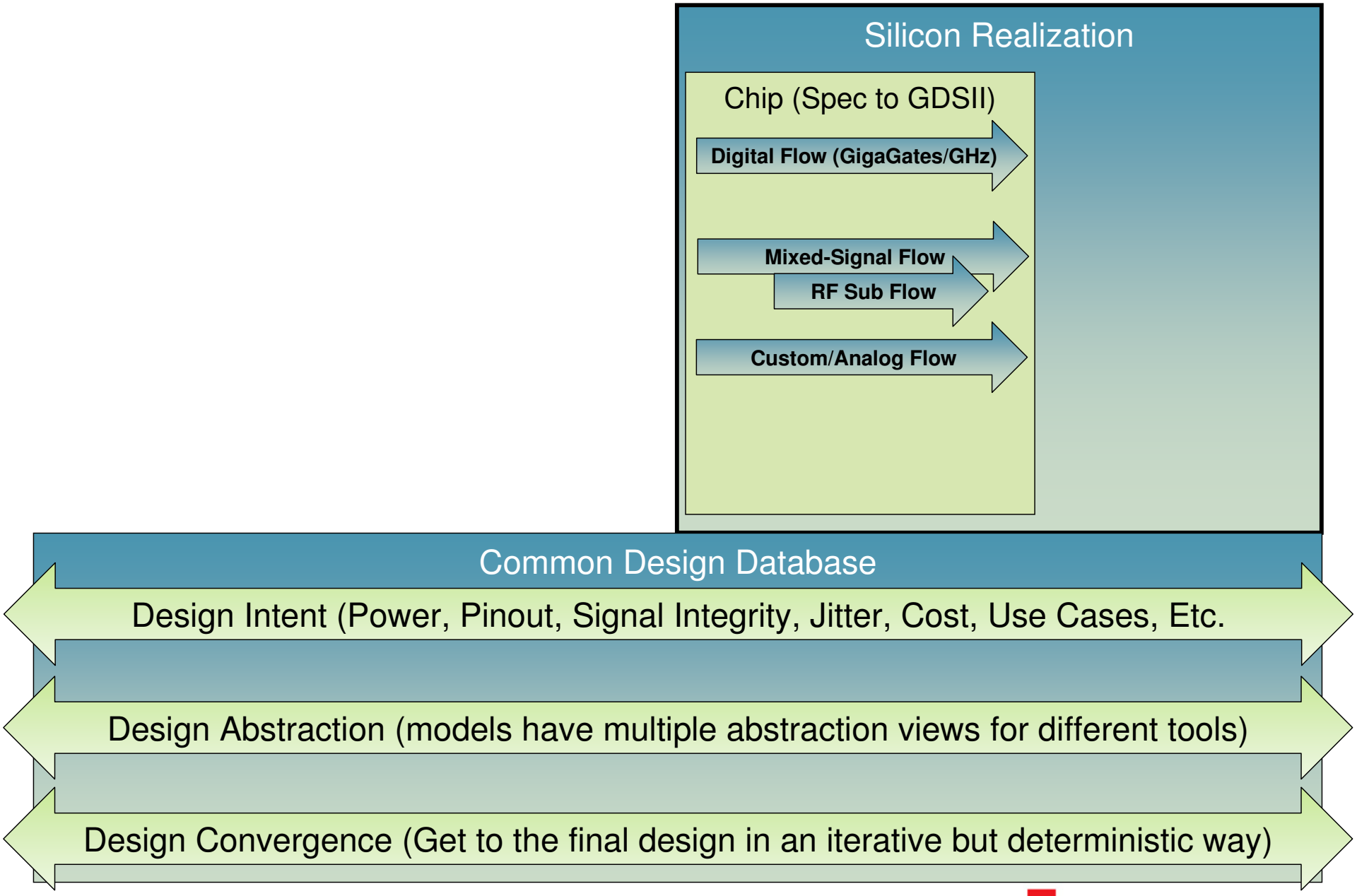

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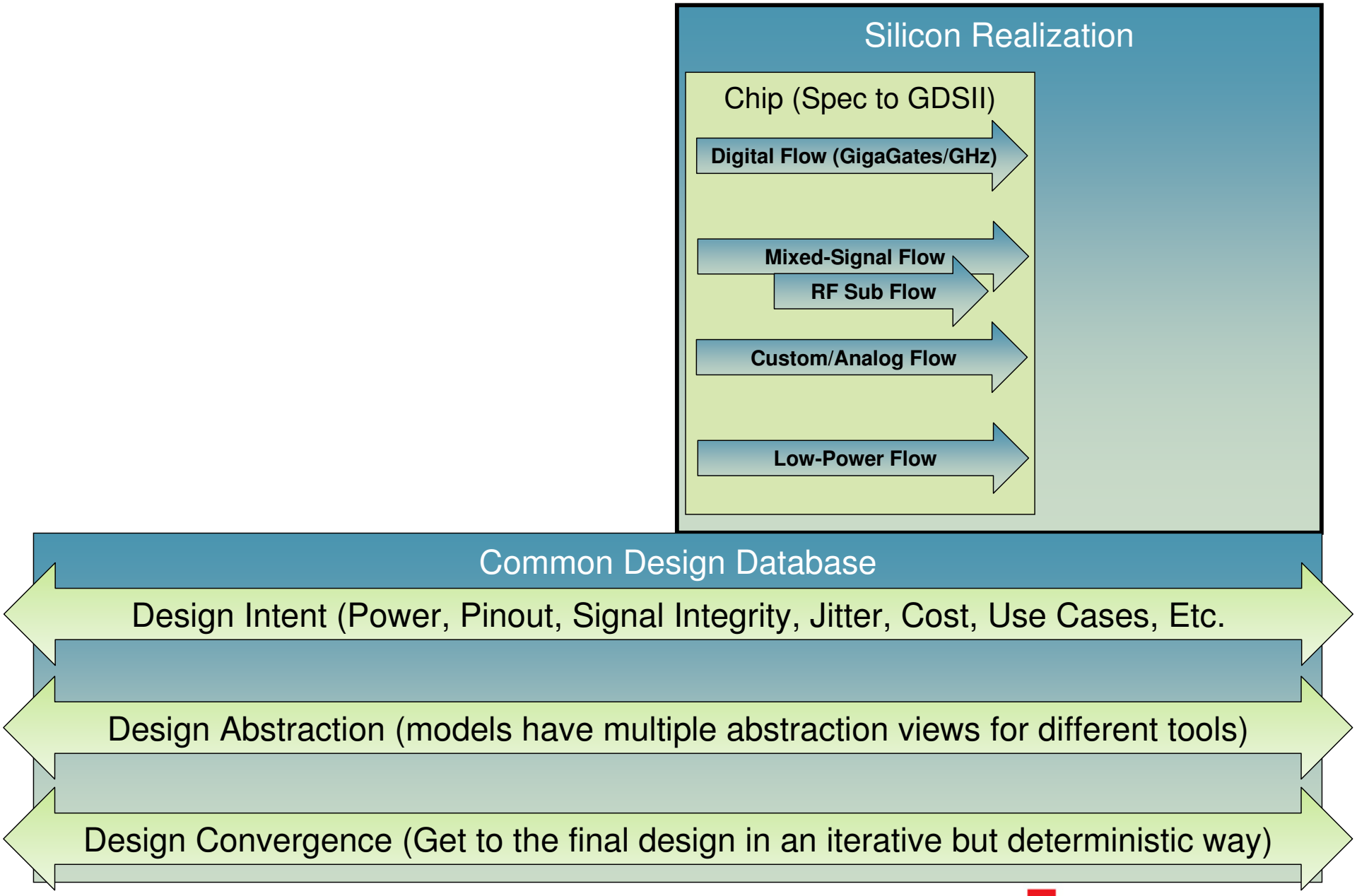

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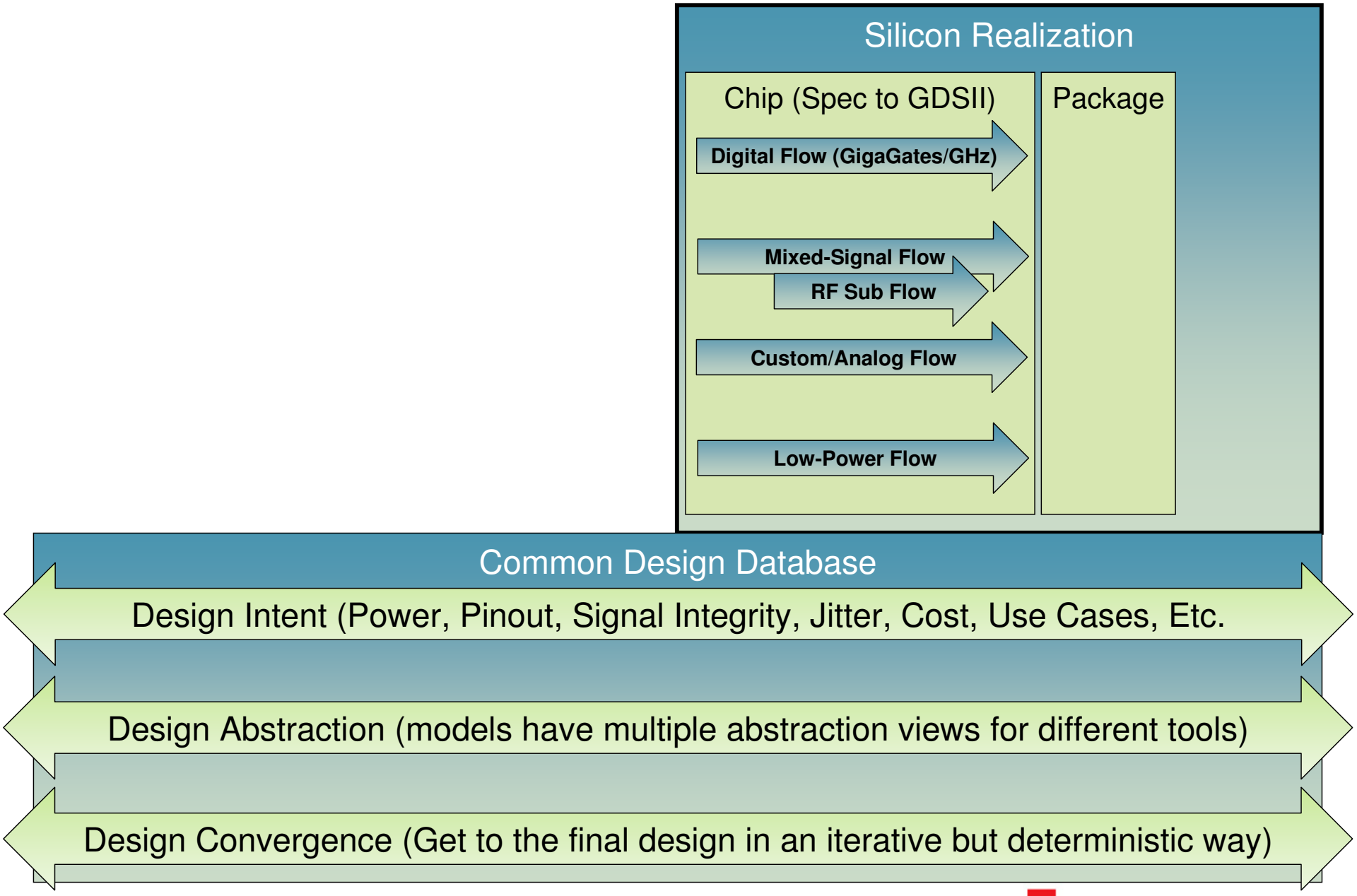

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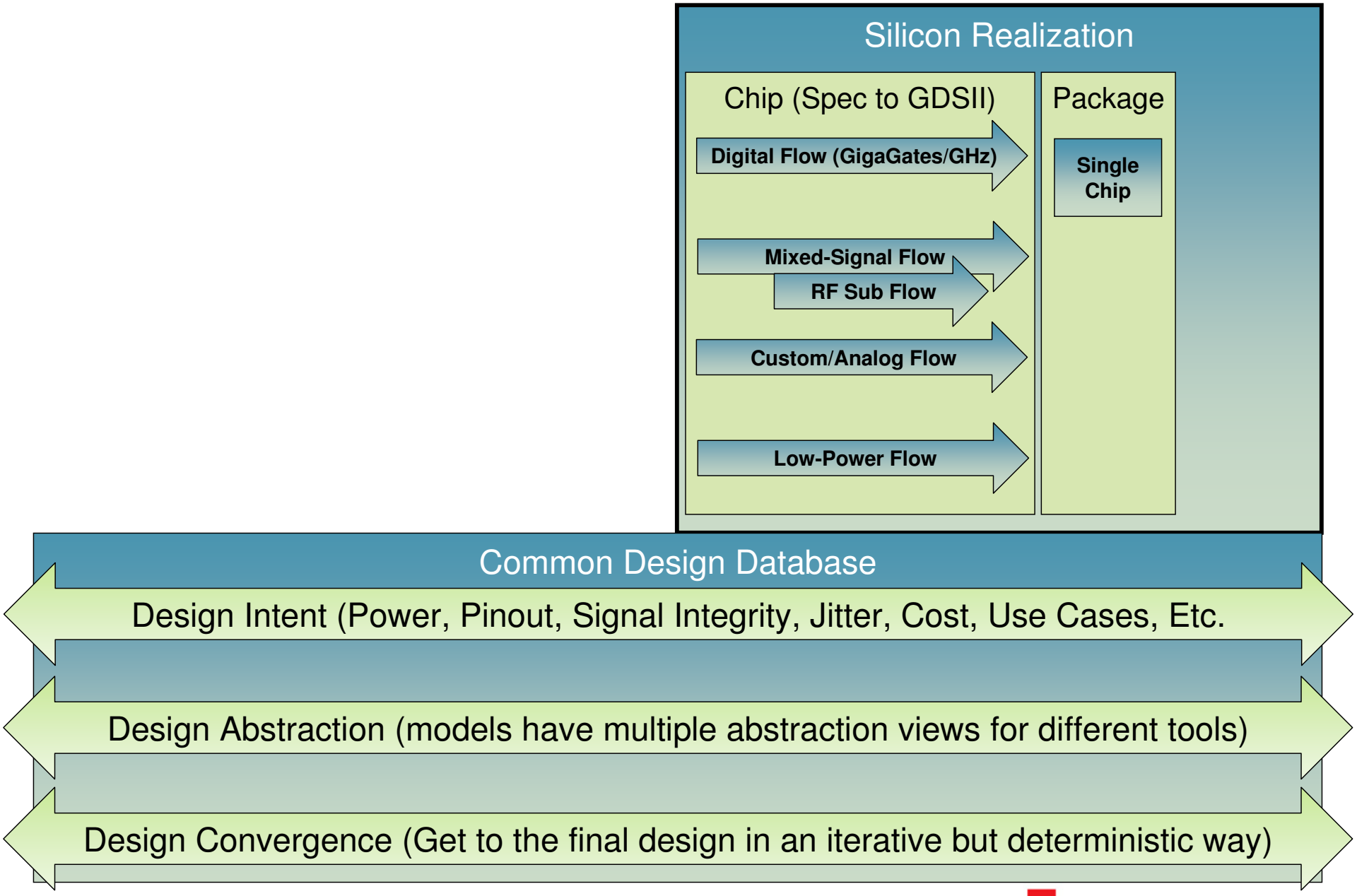

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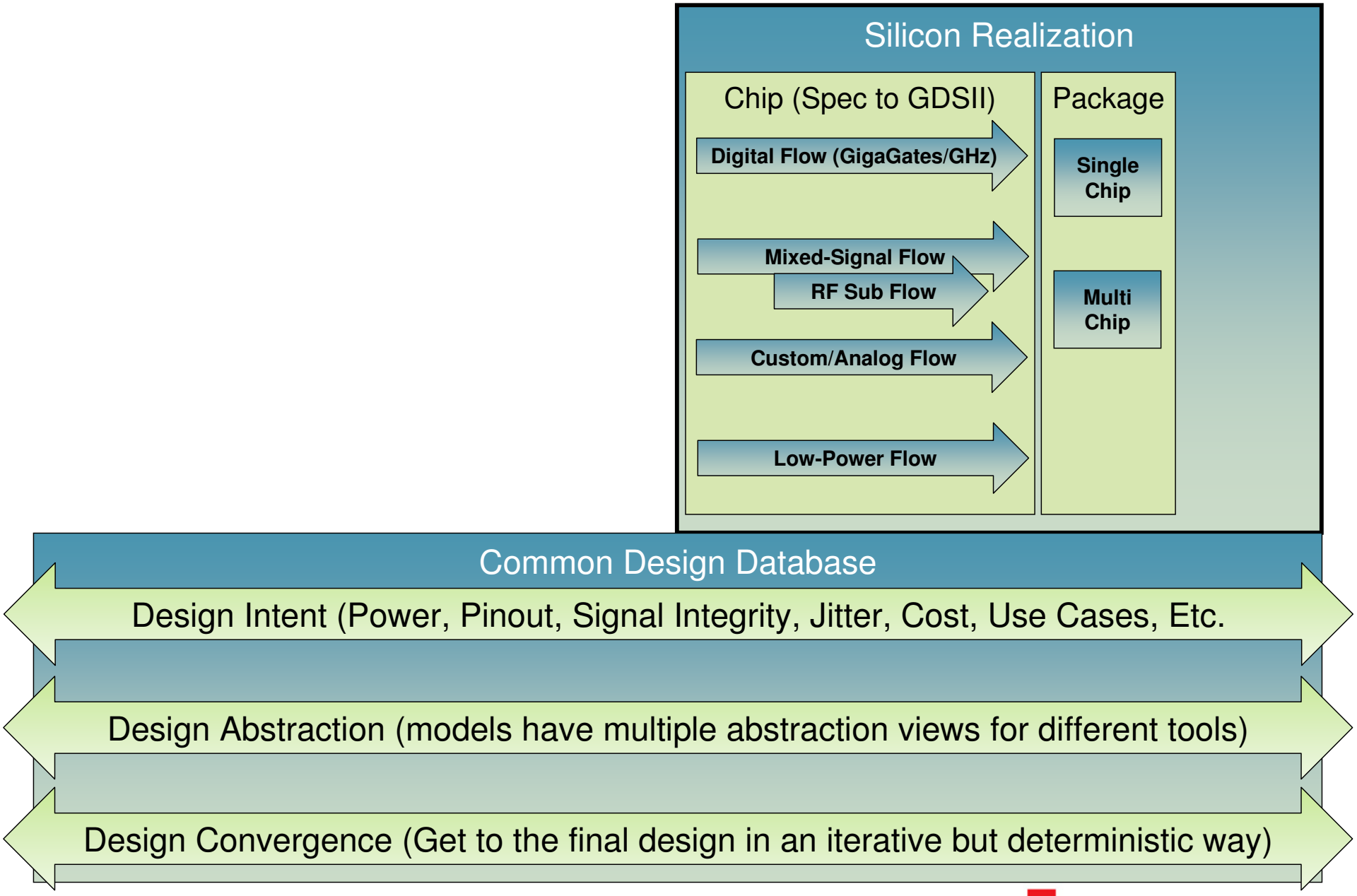

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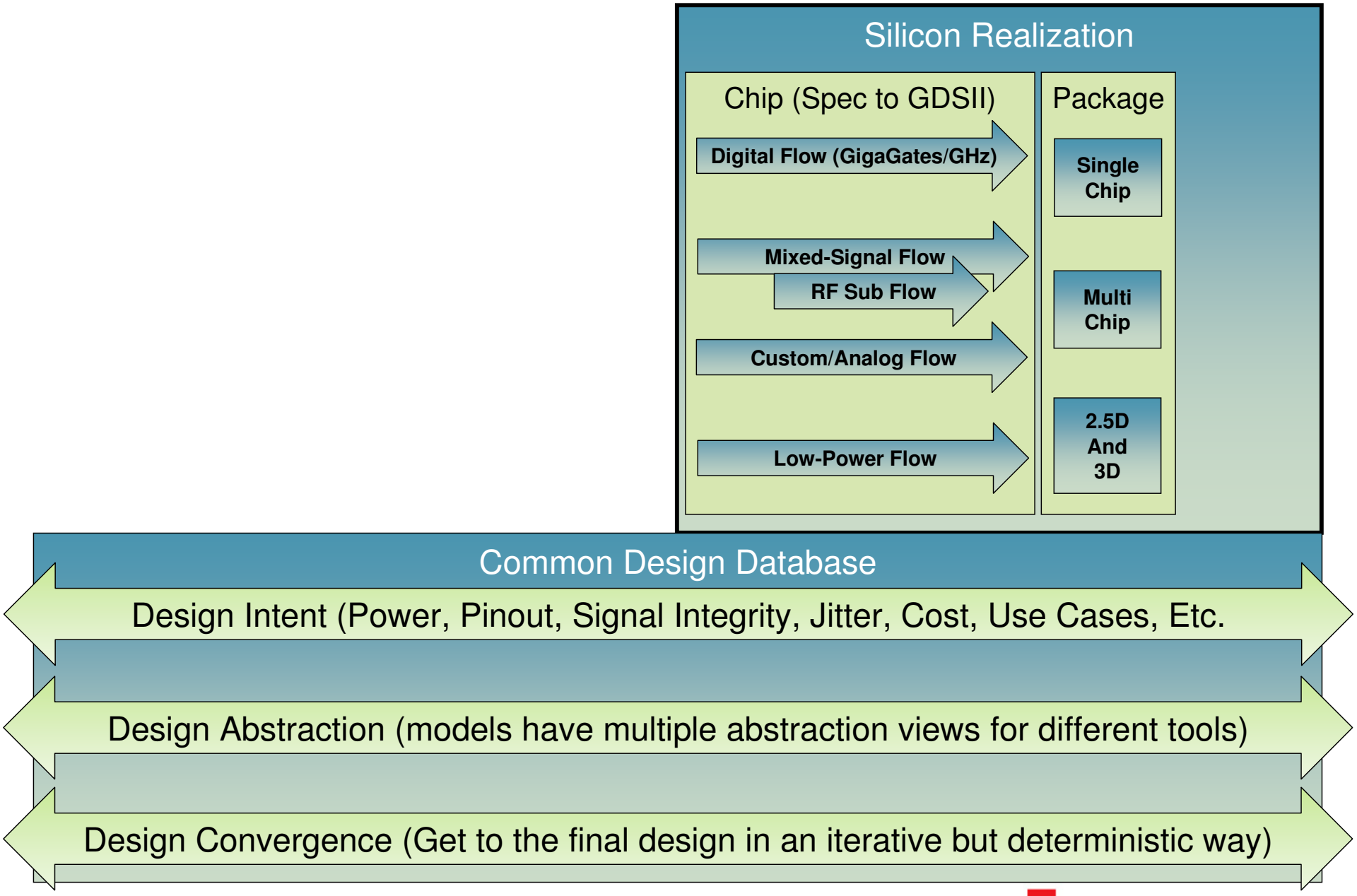

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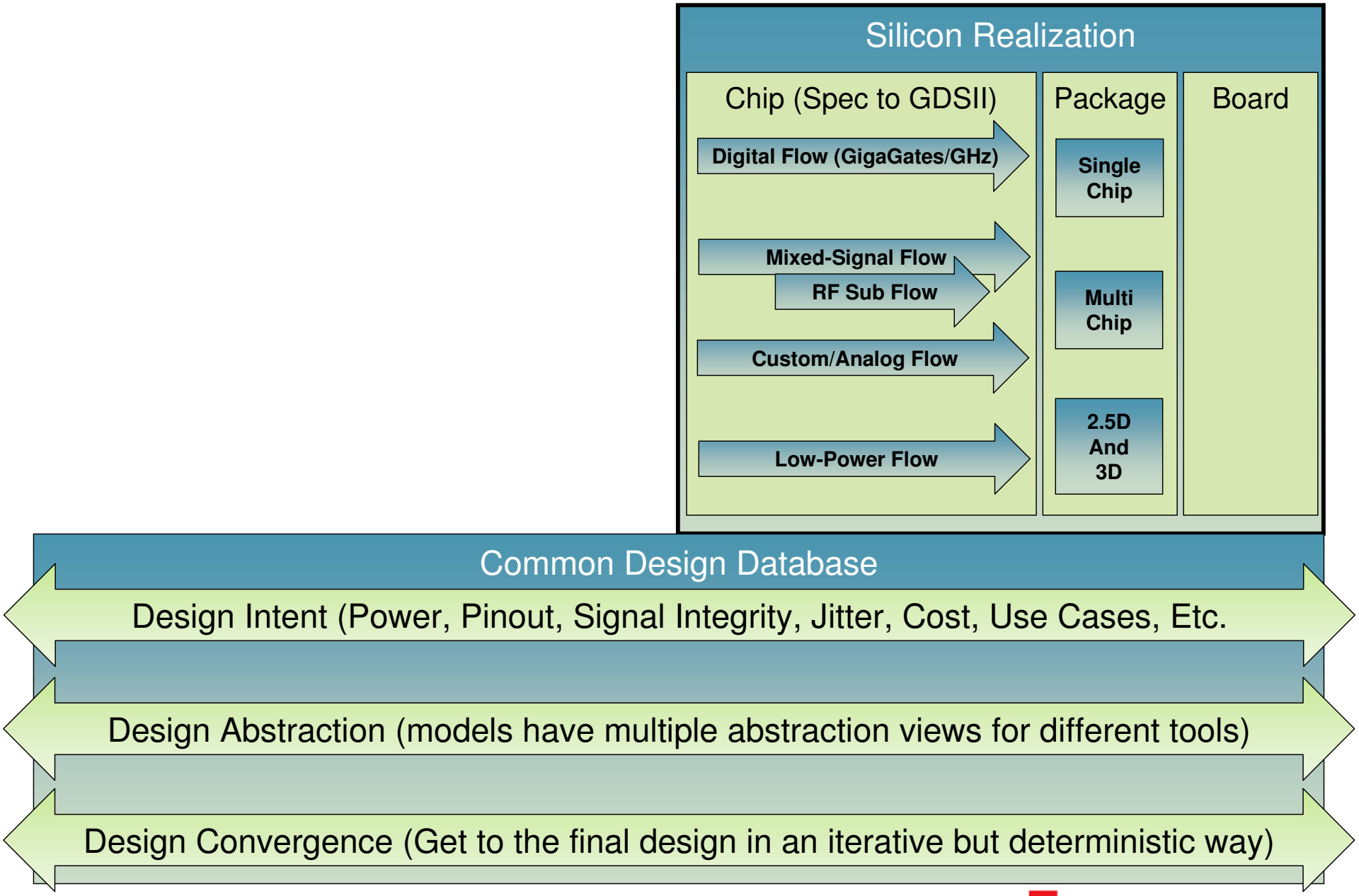

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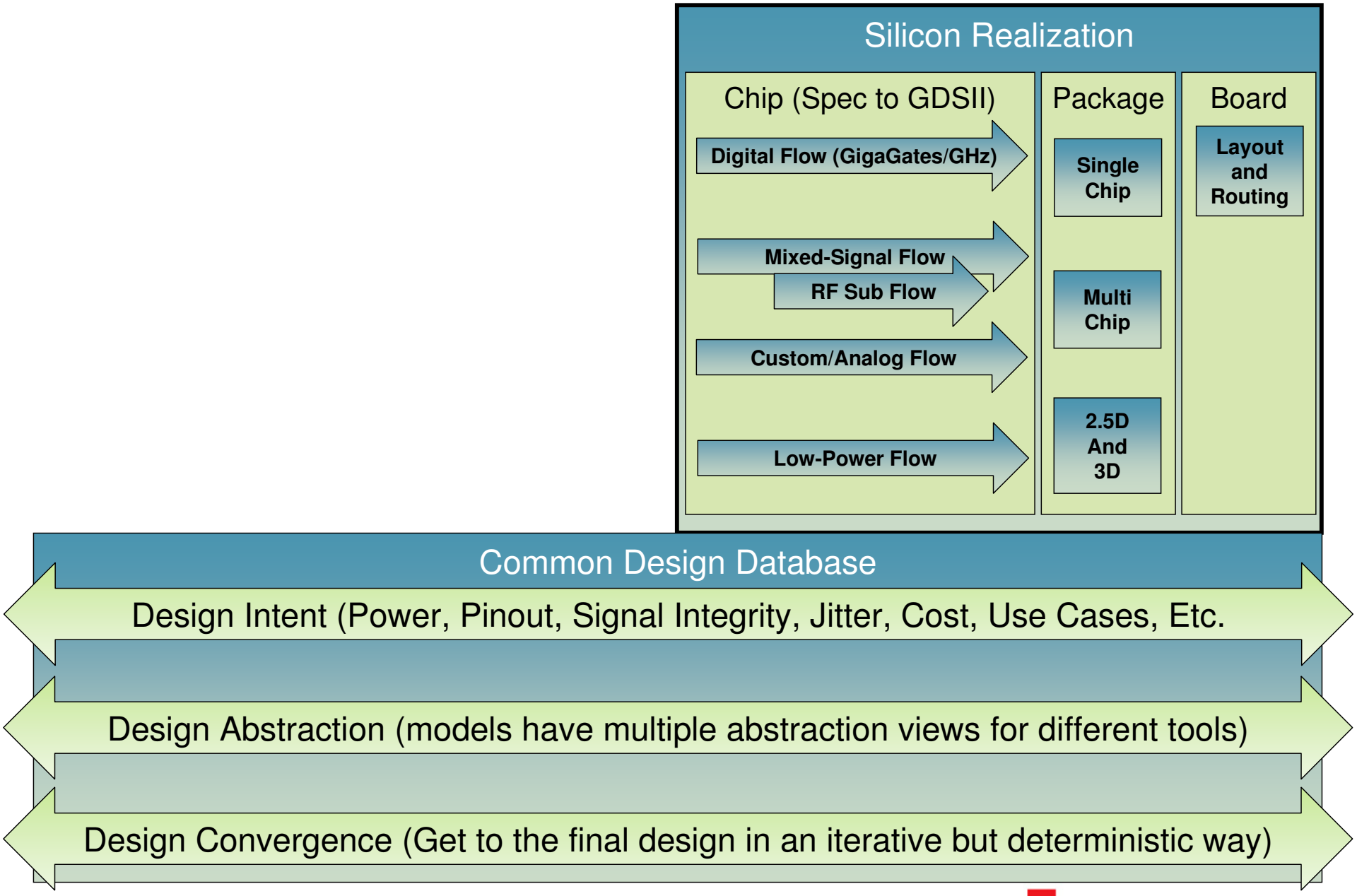

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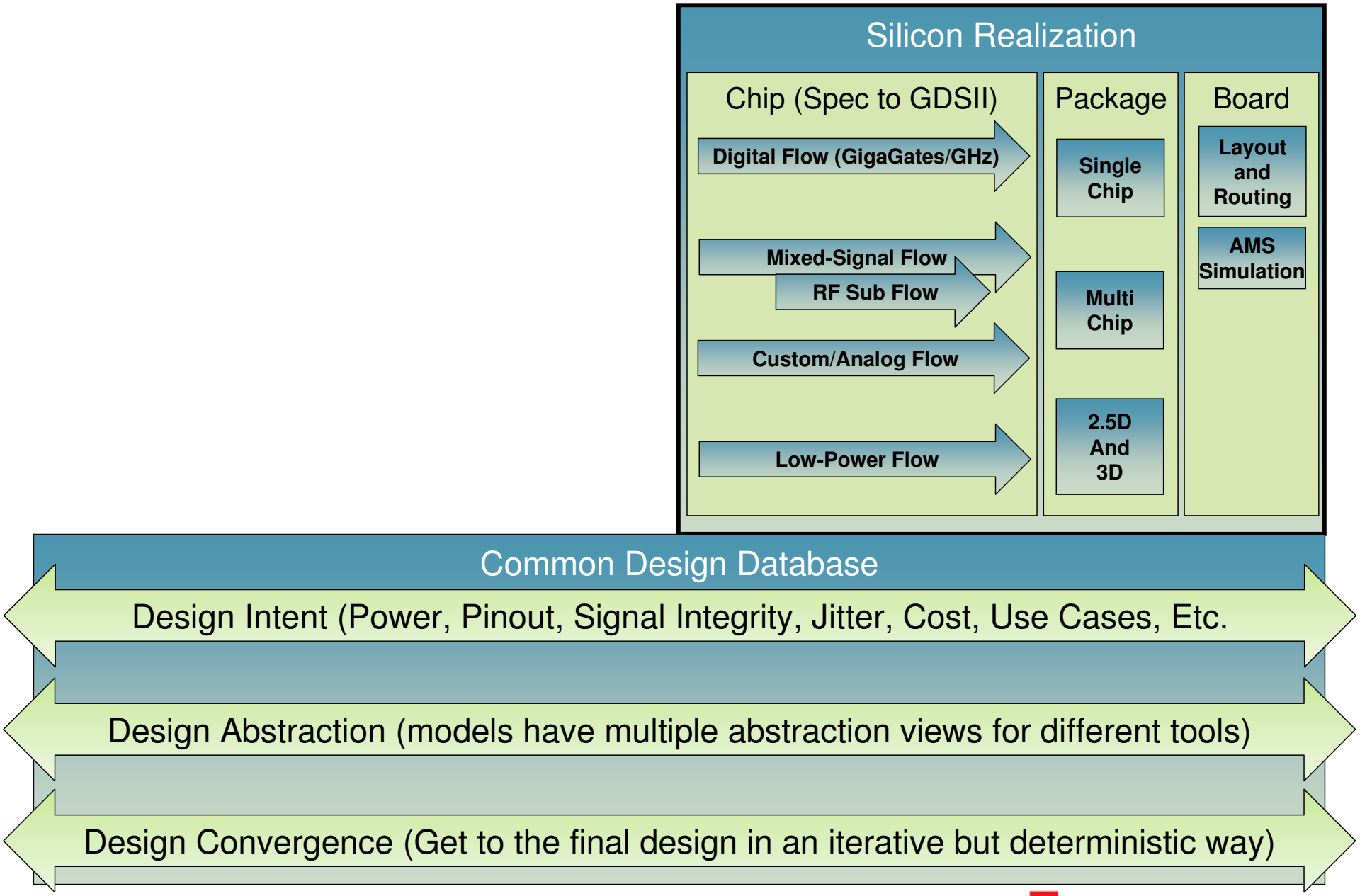

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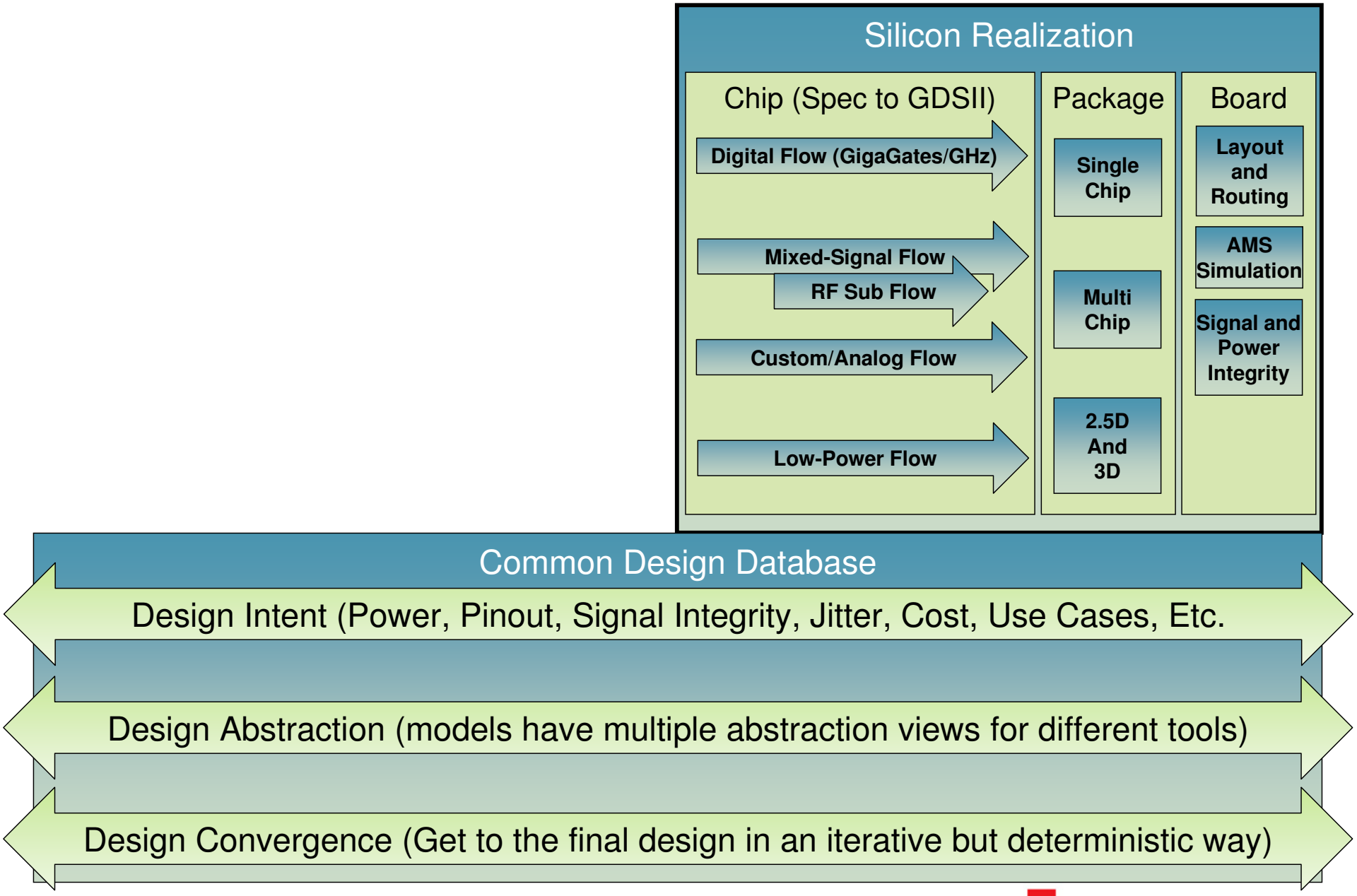

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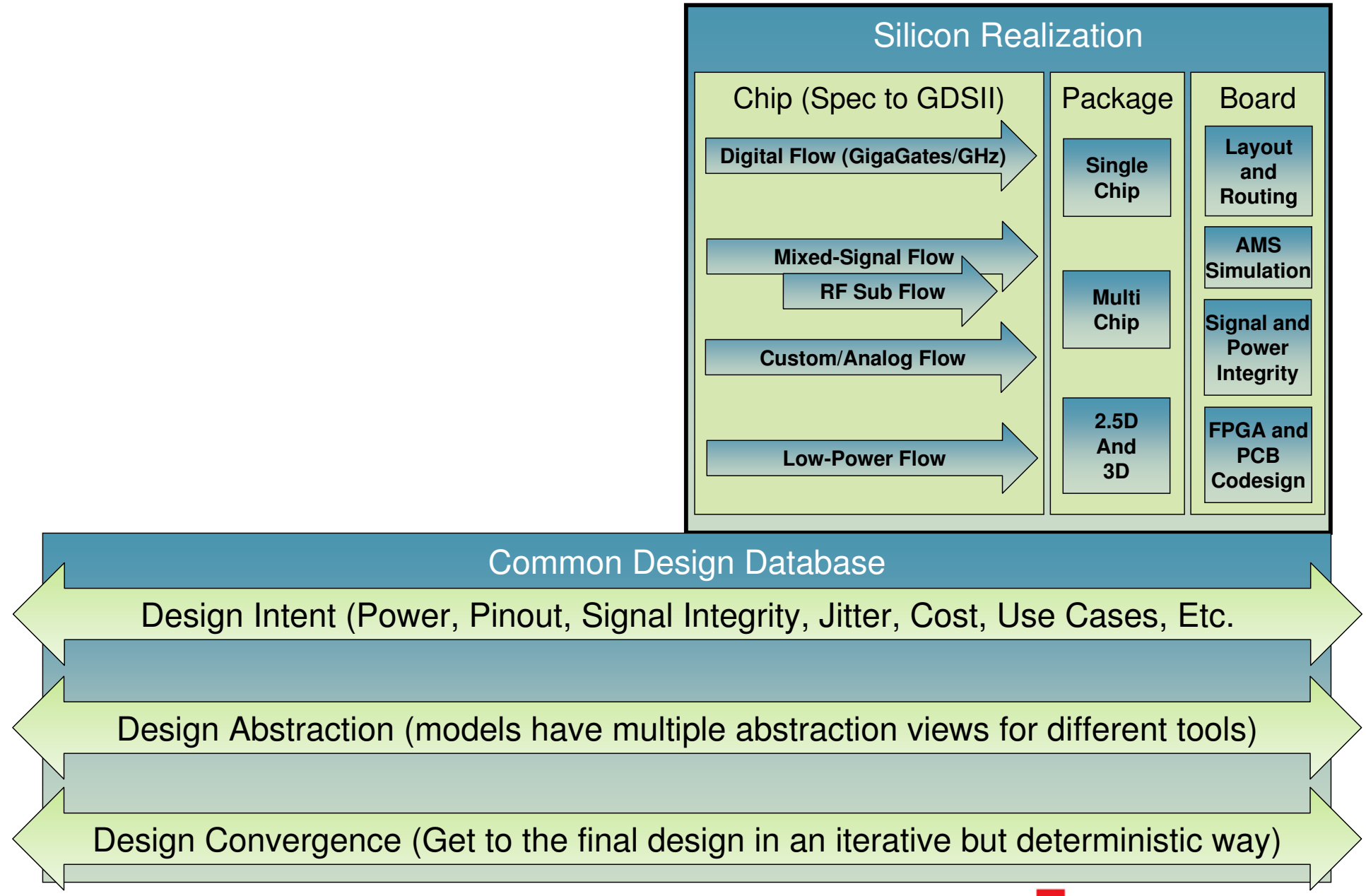

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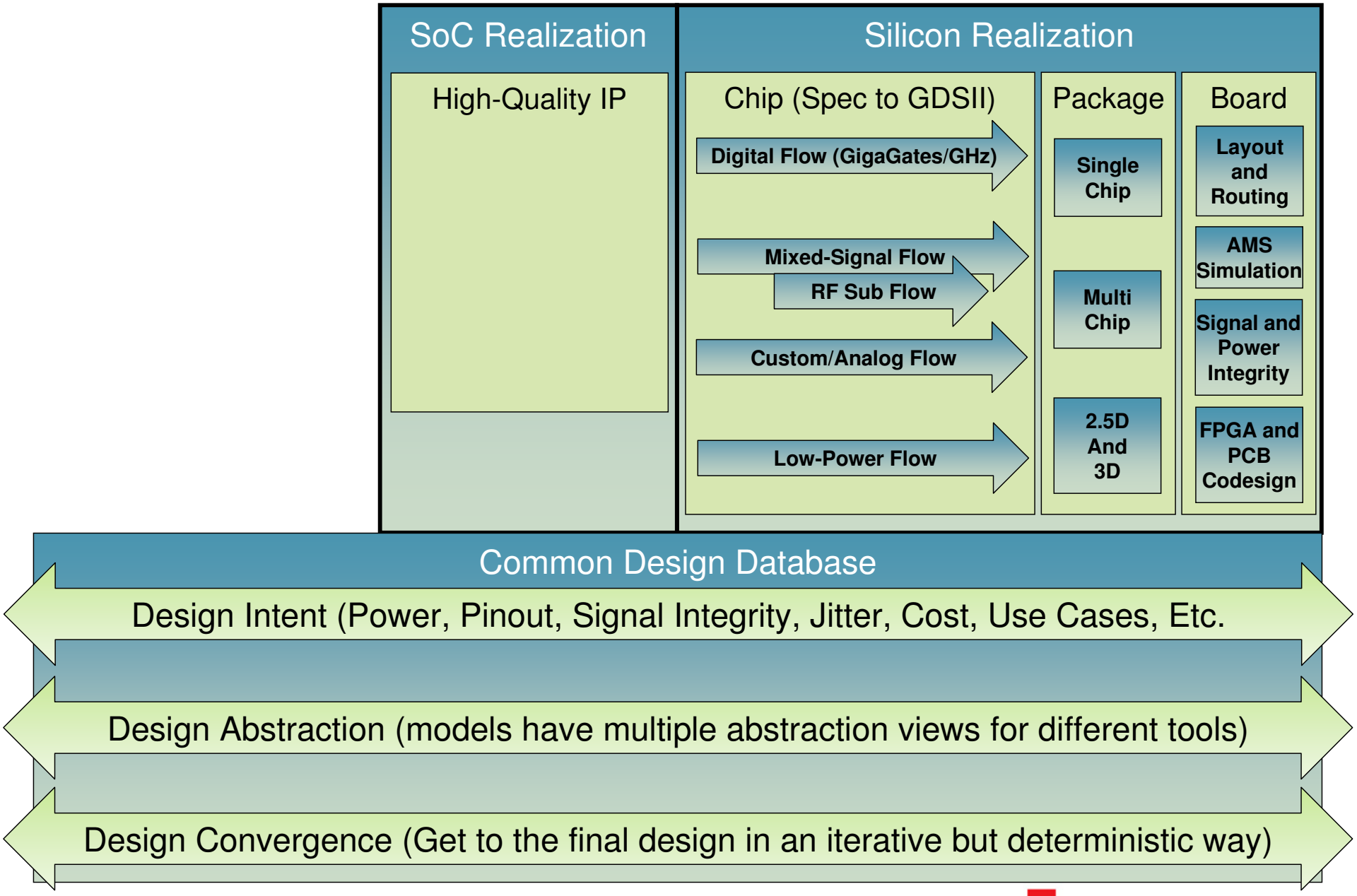

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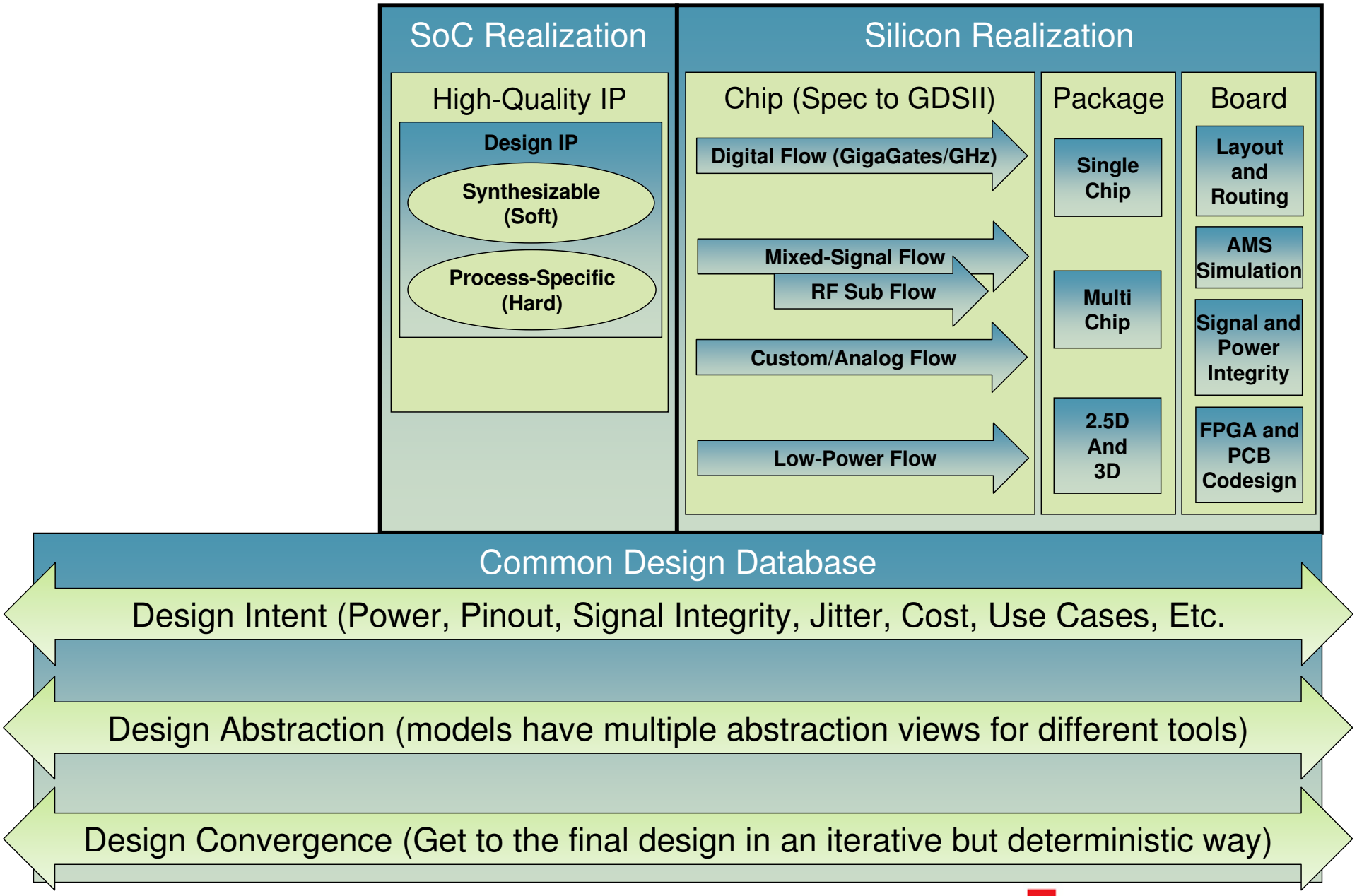

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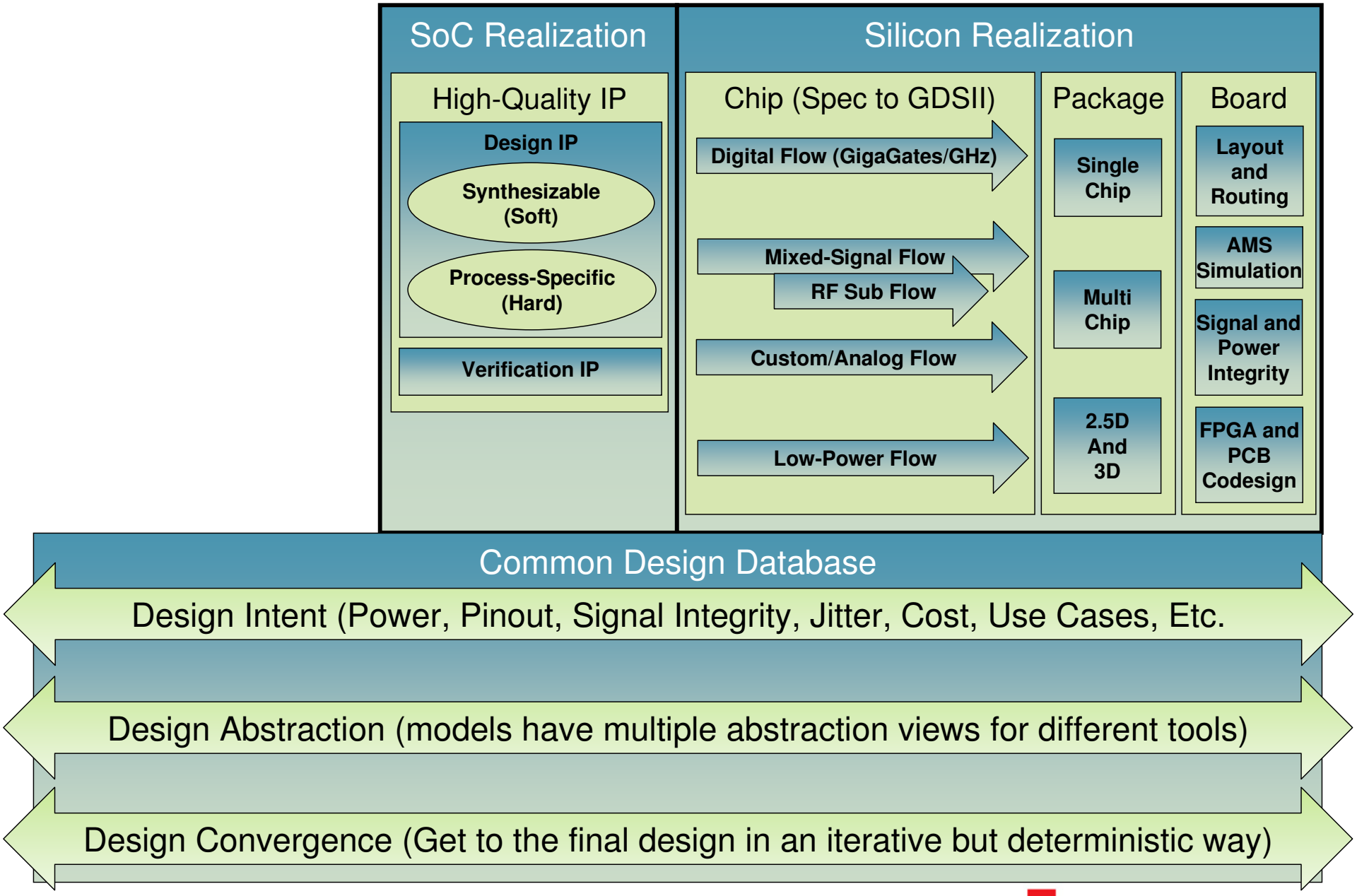

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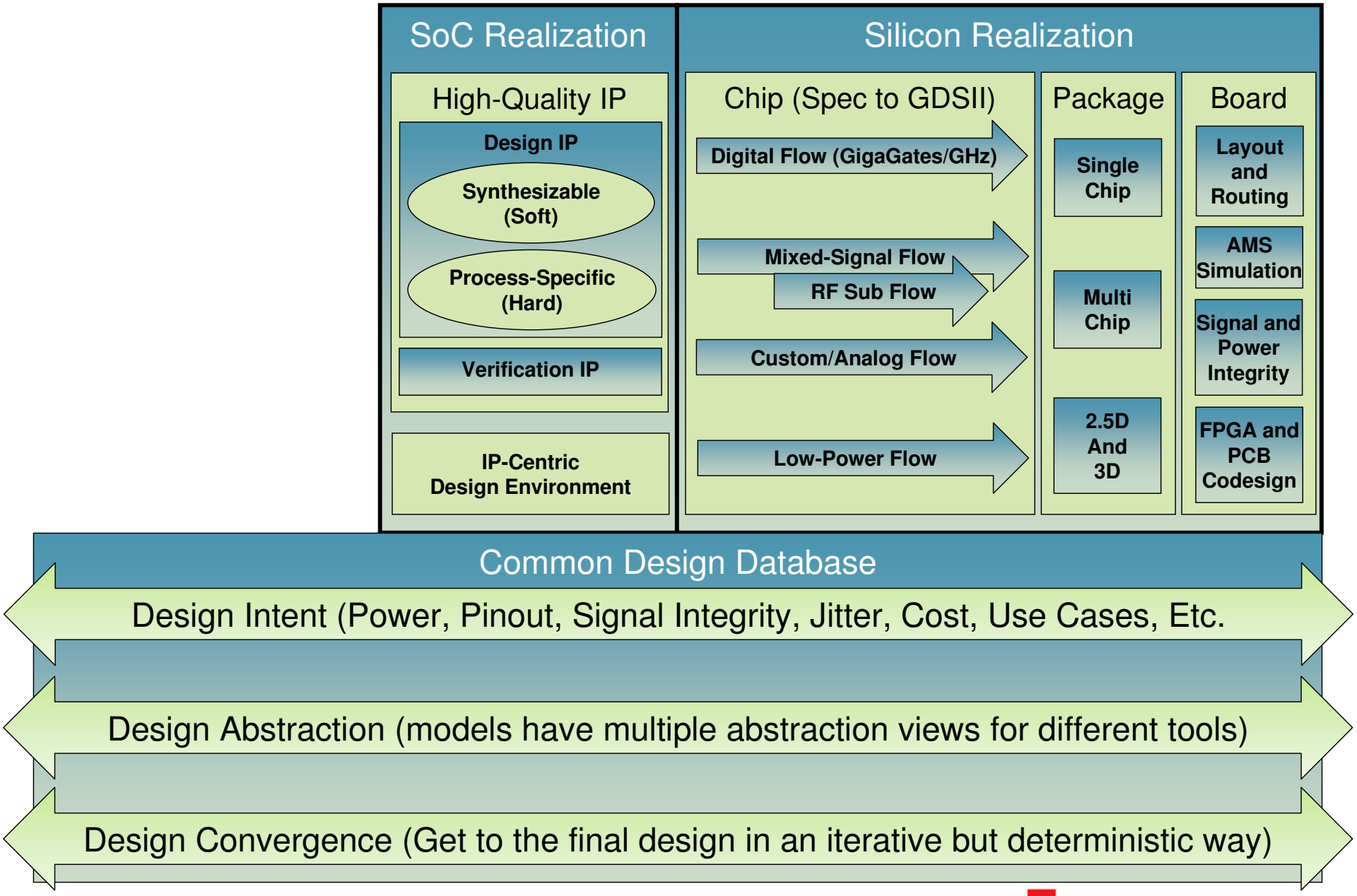

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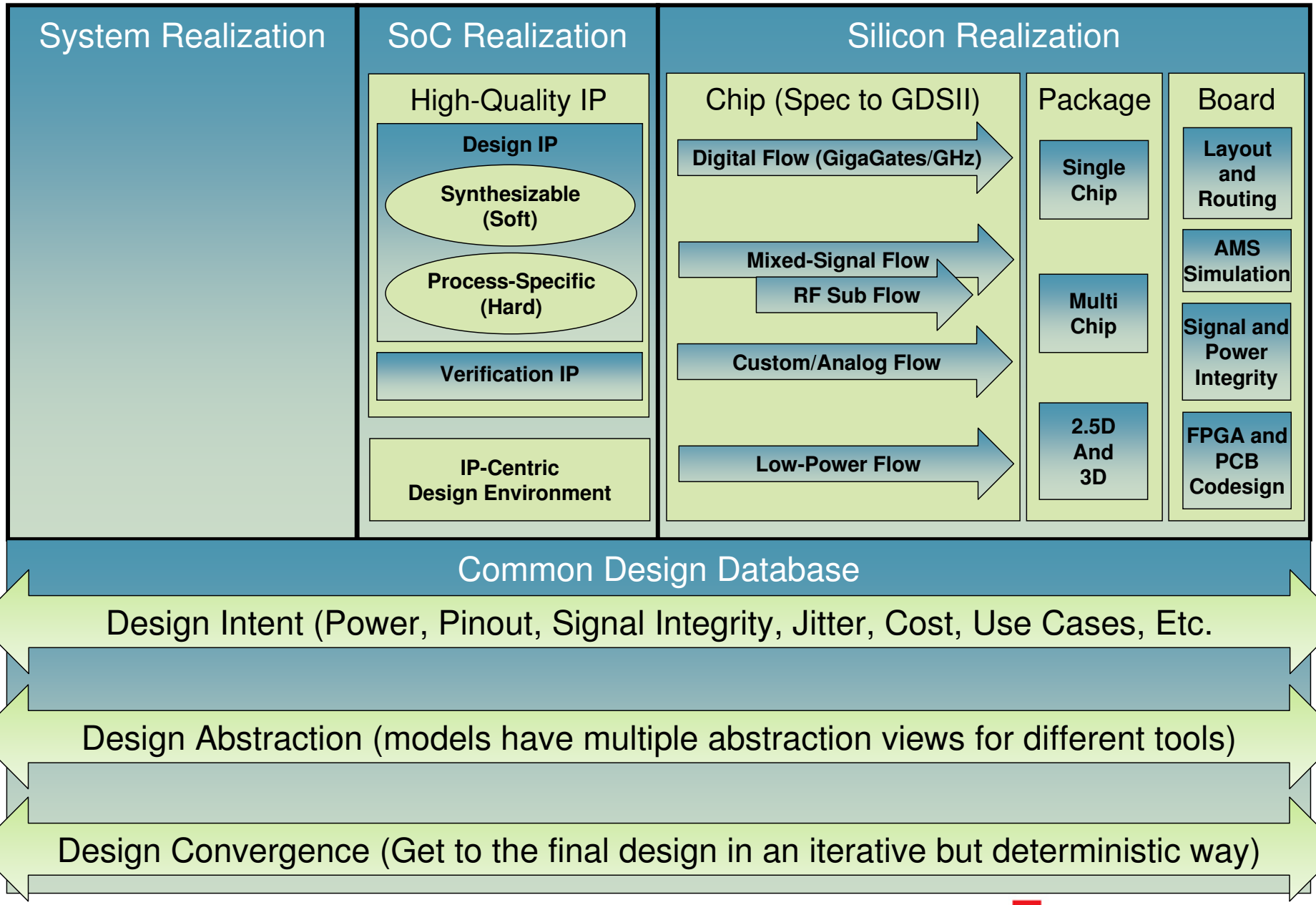

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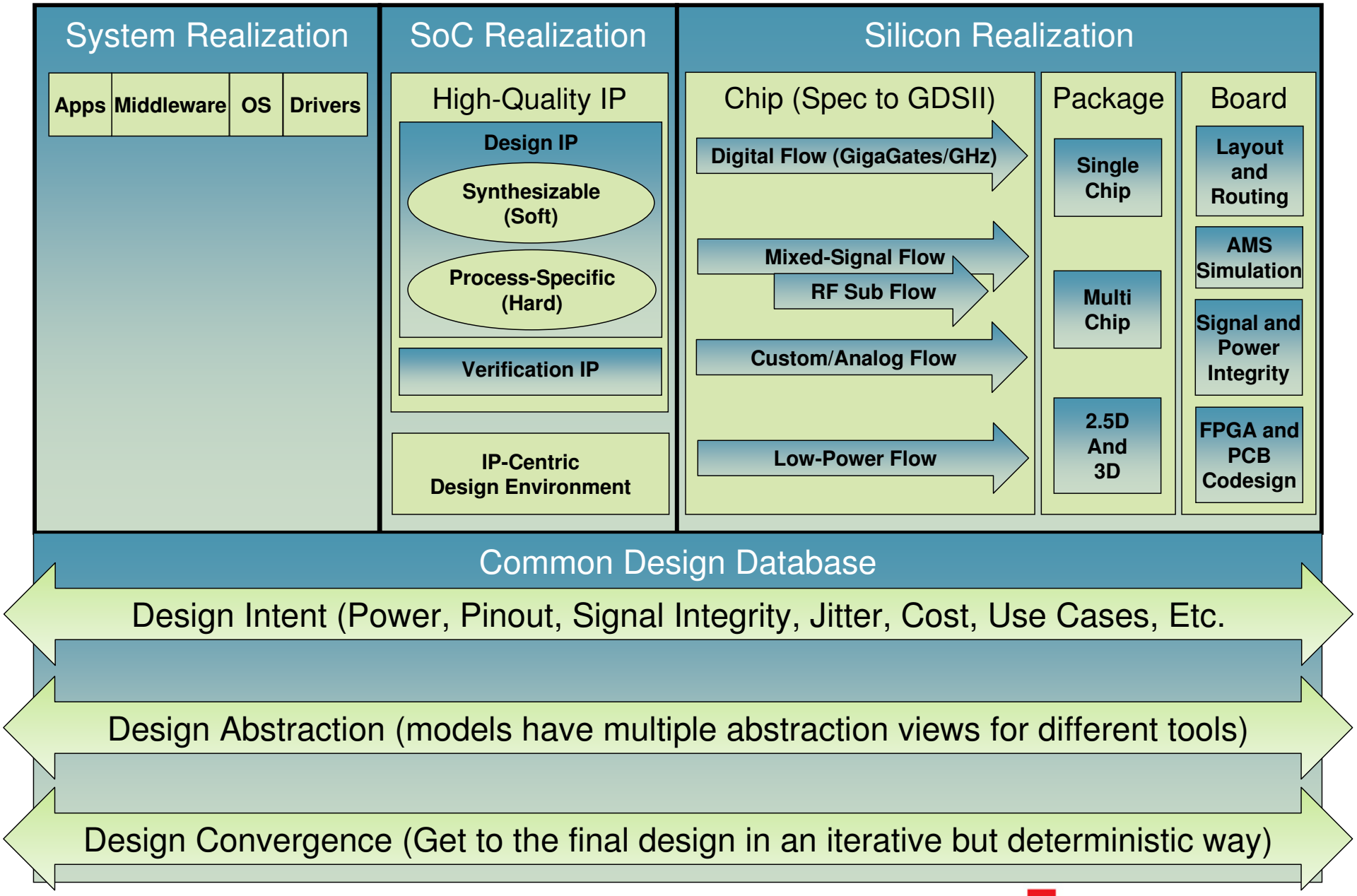

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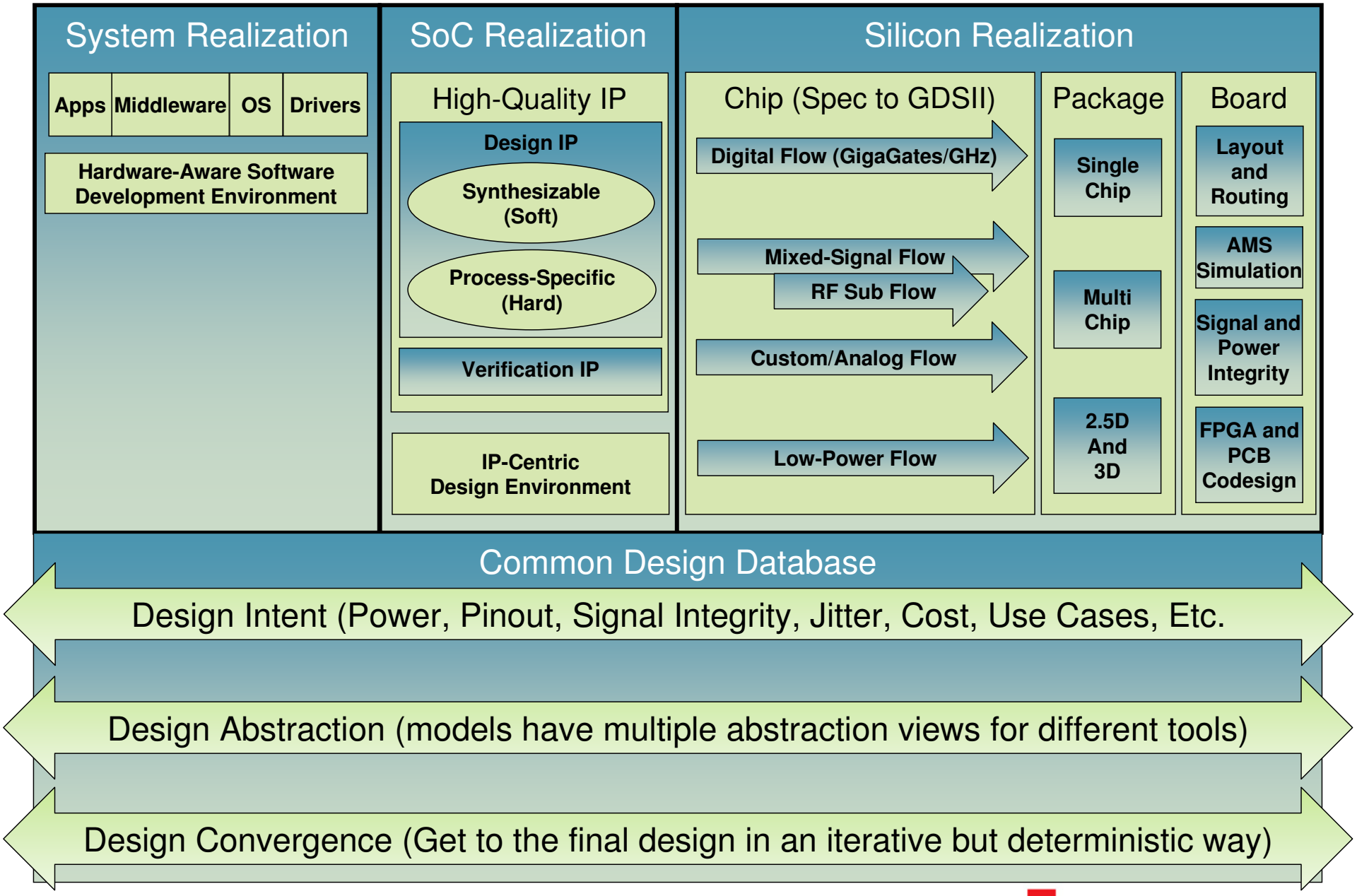

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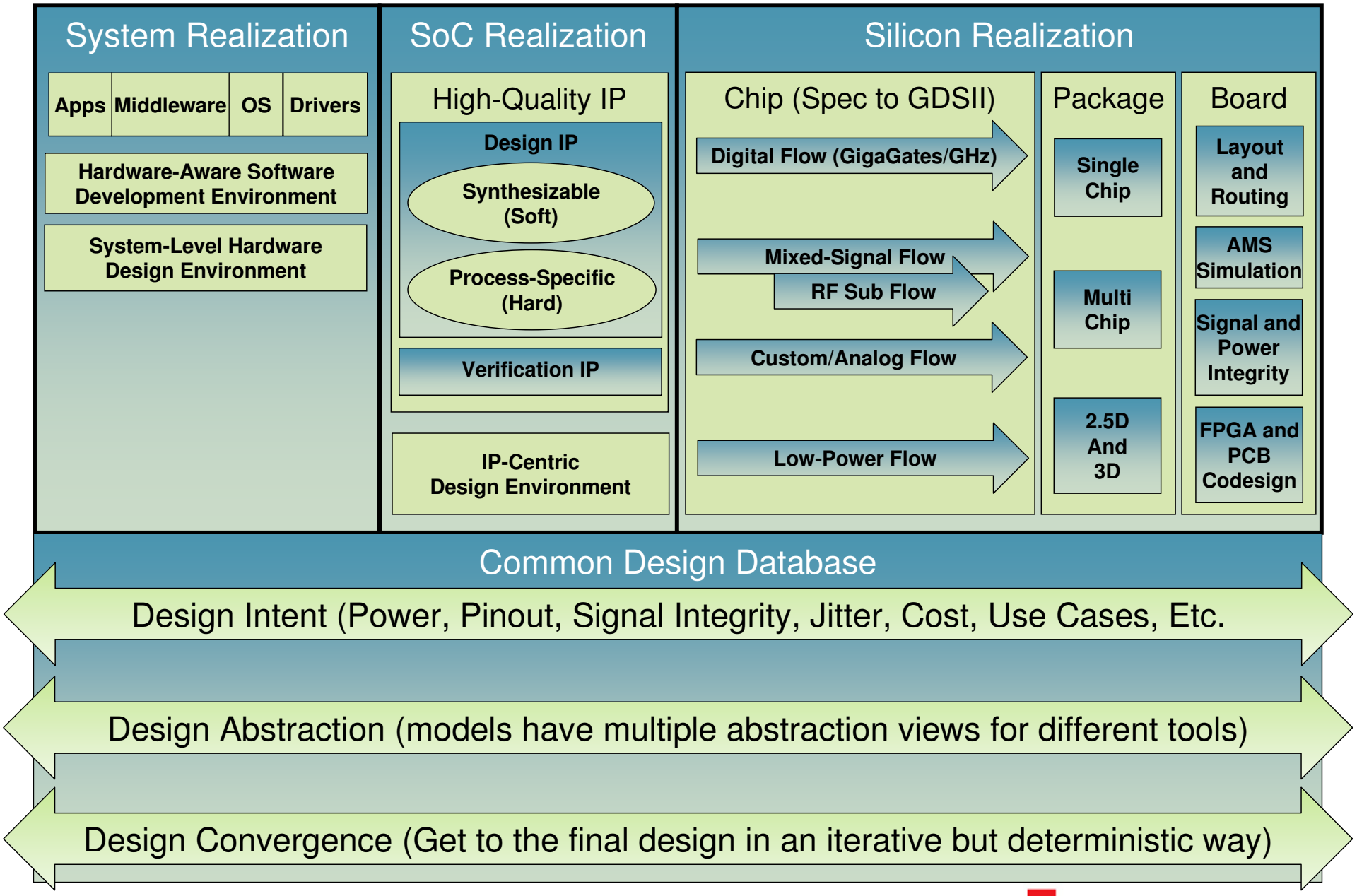

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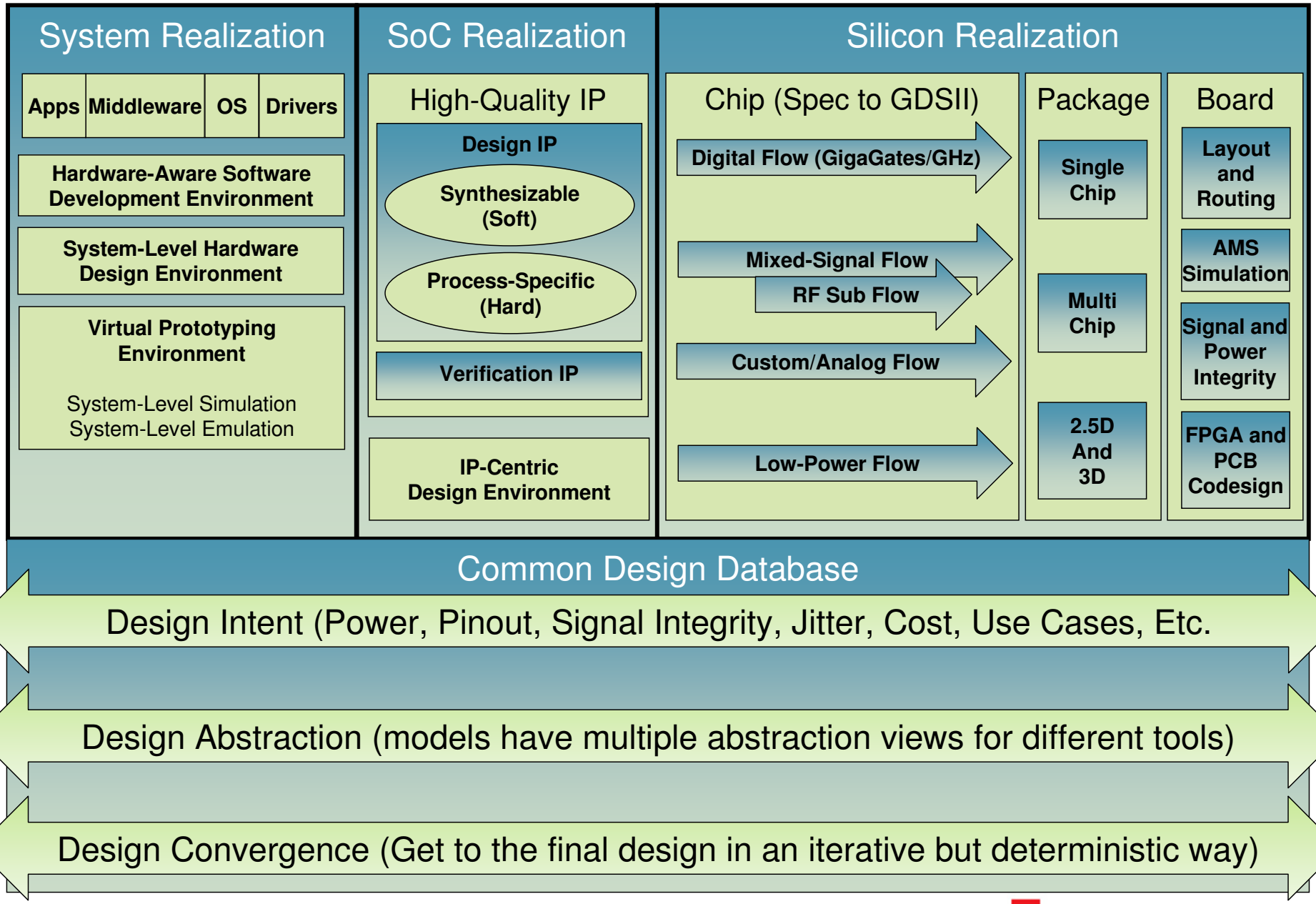

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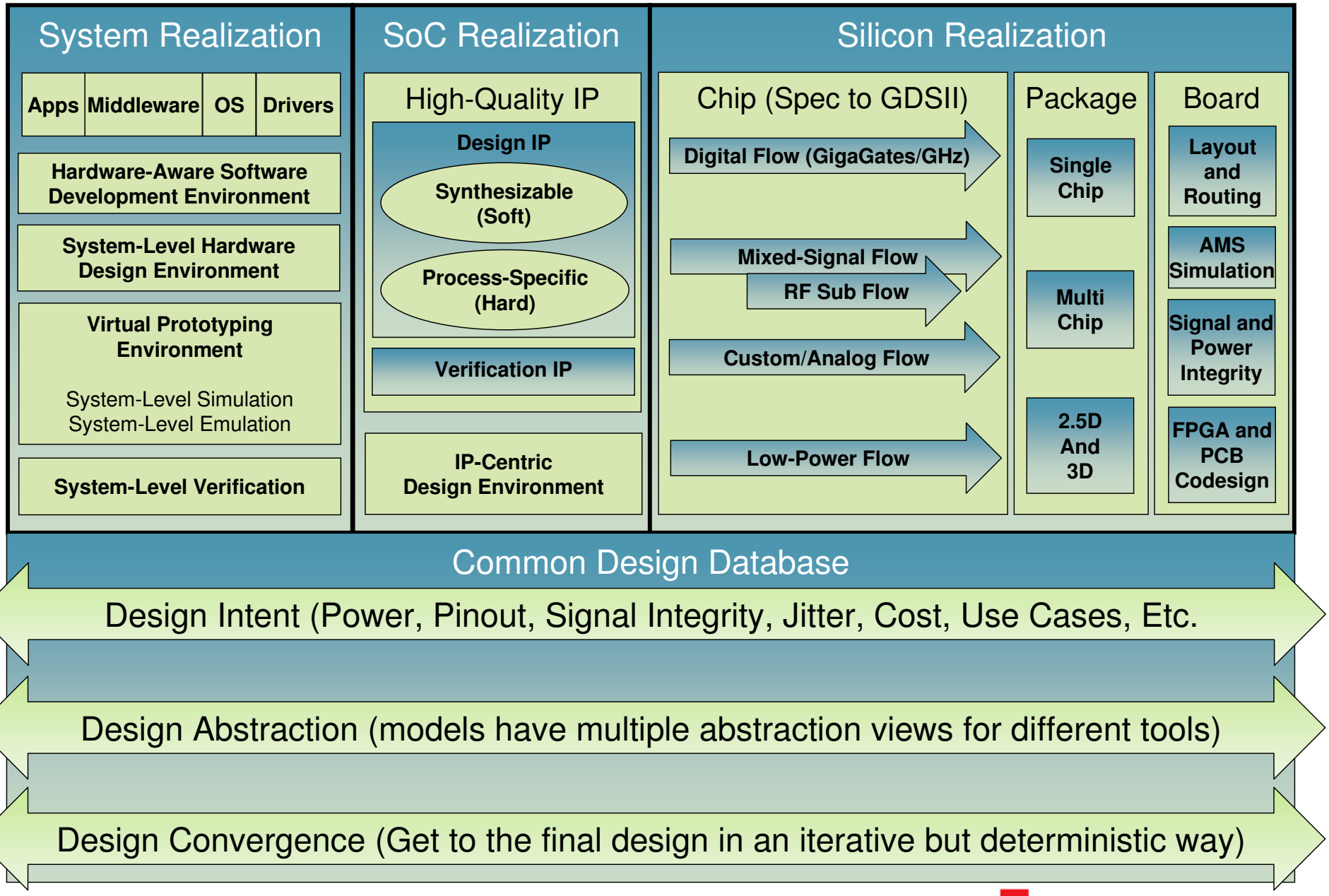
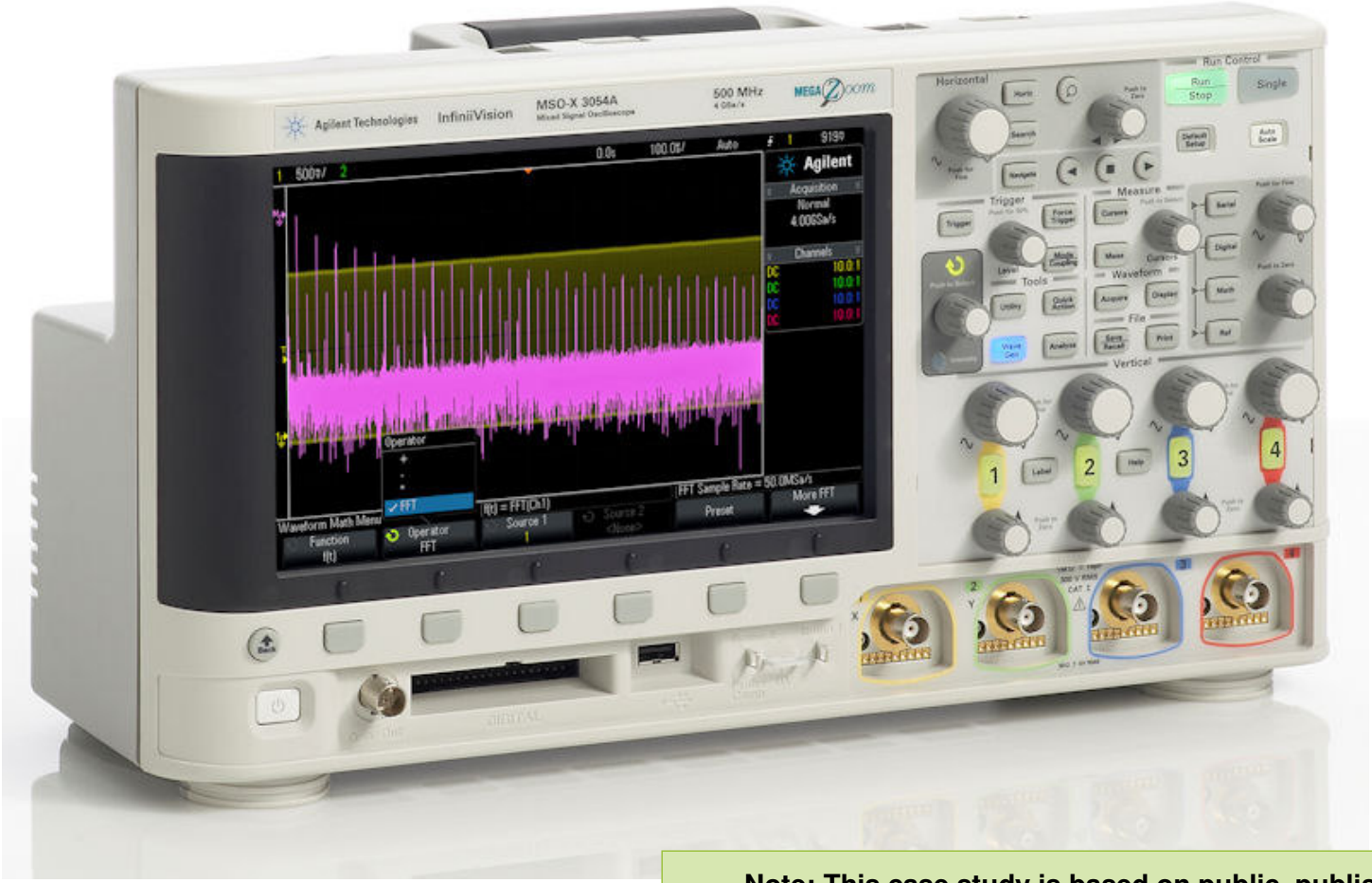


EDA360 Case Study: Agilent InfiniiVision Digital/Mixed-Signal Sampling Oscilloscope



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Note: This case study is based on public, published data and nothing is implied about the EDA tools used to develop this product.

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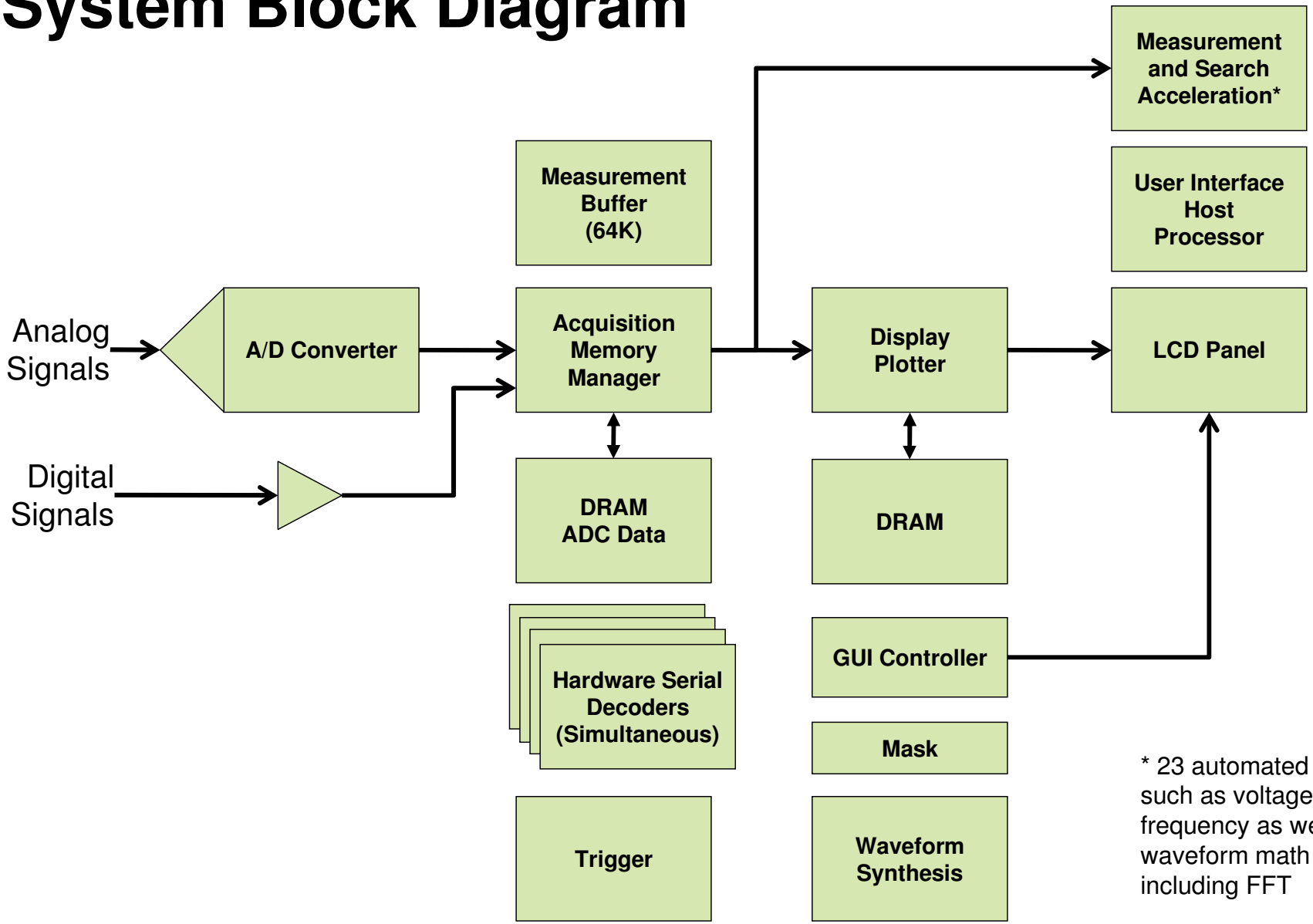
Agilent InfiniiVision 2000/3000 DSO/MSO System Block Diagram



* 23 automated measurements such as voltage, time, and frequency as well as four waveform math functions including FFT

Diagram as published in EE Times

Agilent InfiniiVision 2000/3000 DSO/MSO System Intent

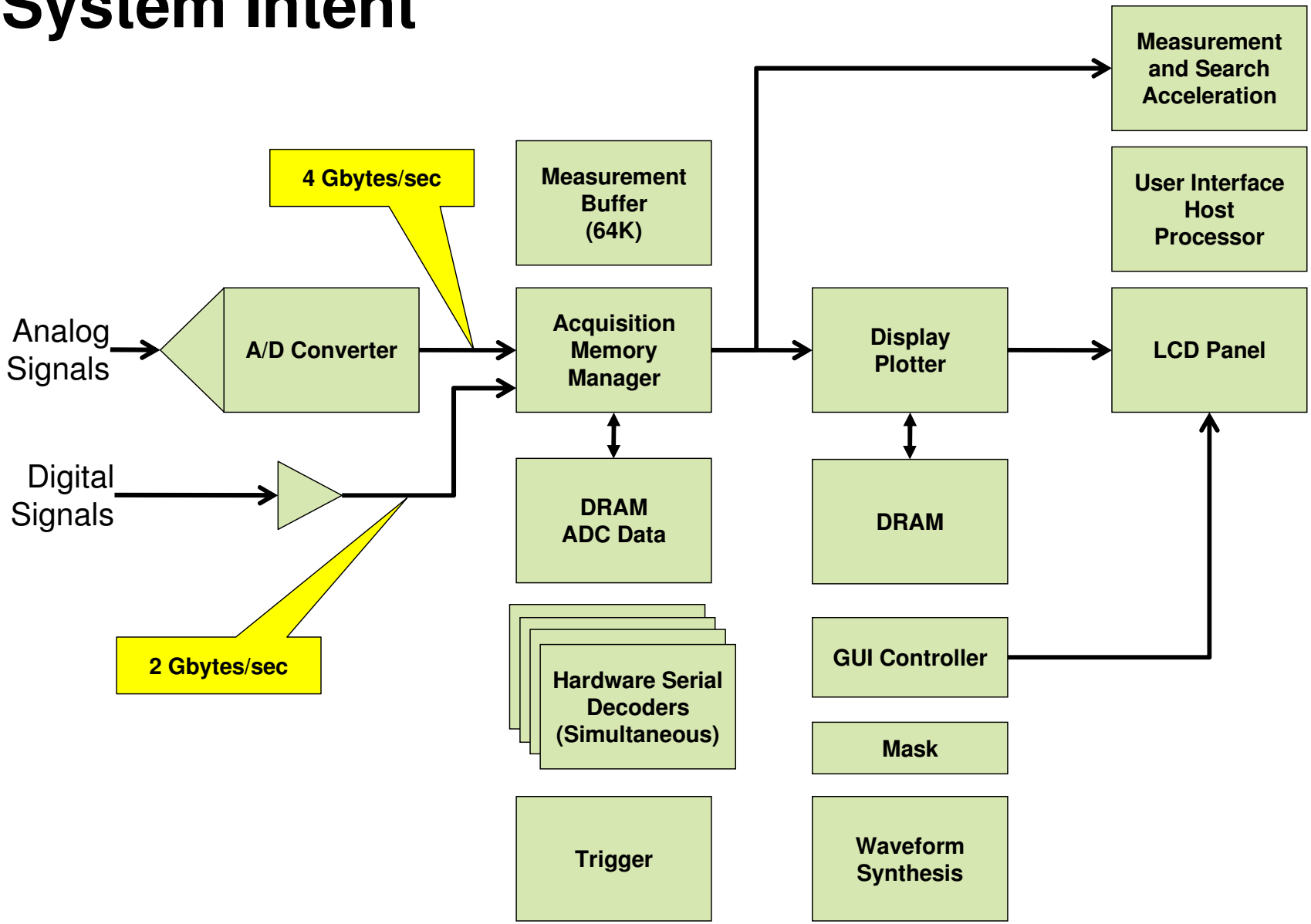
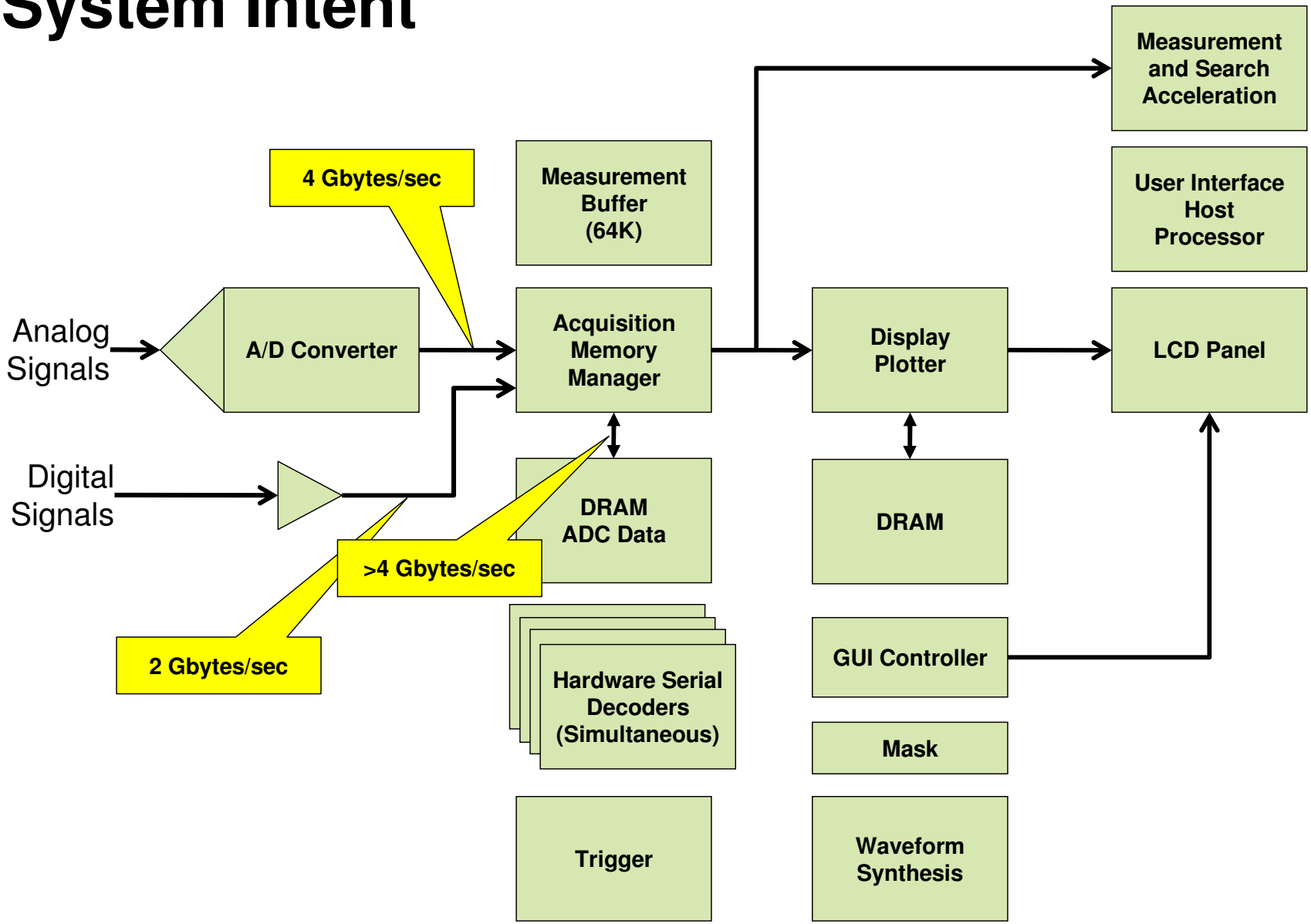


Diagram as published in EE Times

Agilent InfiniiVision 2000/3000 DSO/MSO System Intent



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Agilent InfiniiVision 2000/3000 DSO/MSO System Intent

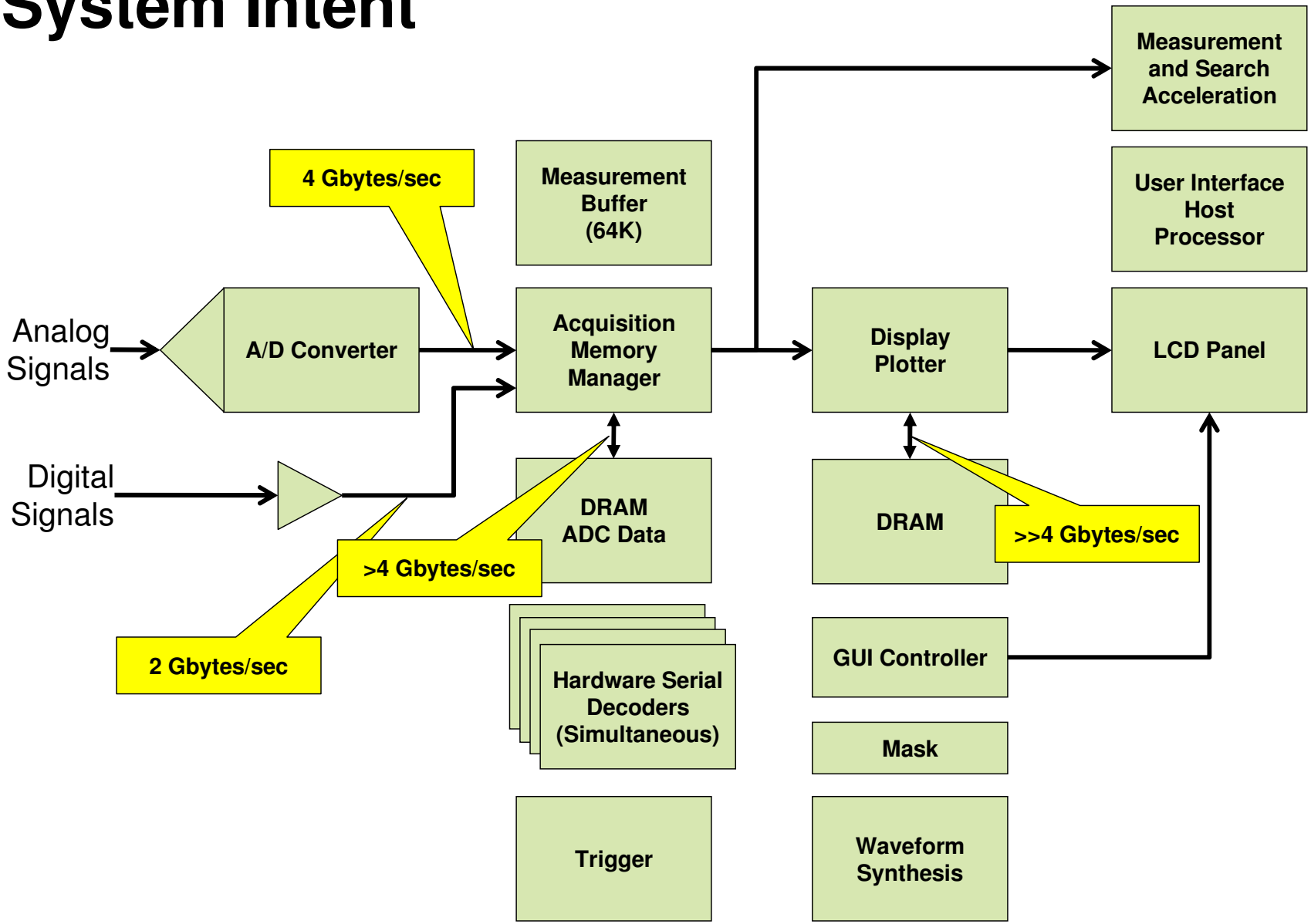


Diagram as published in EE Times

Agilent InfiniiVision 2000/3000 DSO/MSO System Partitioning

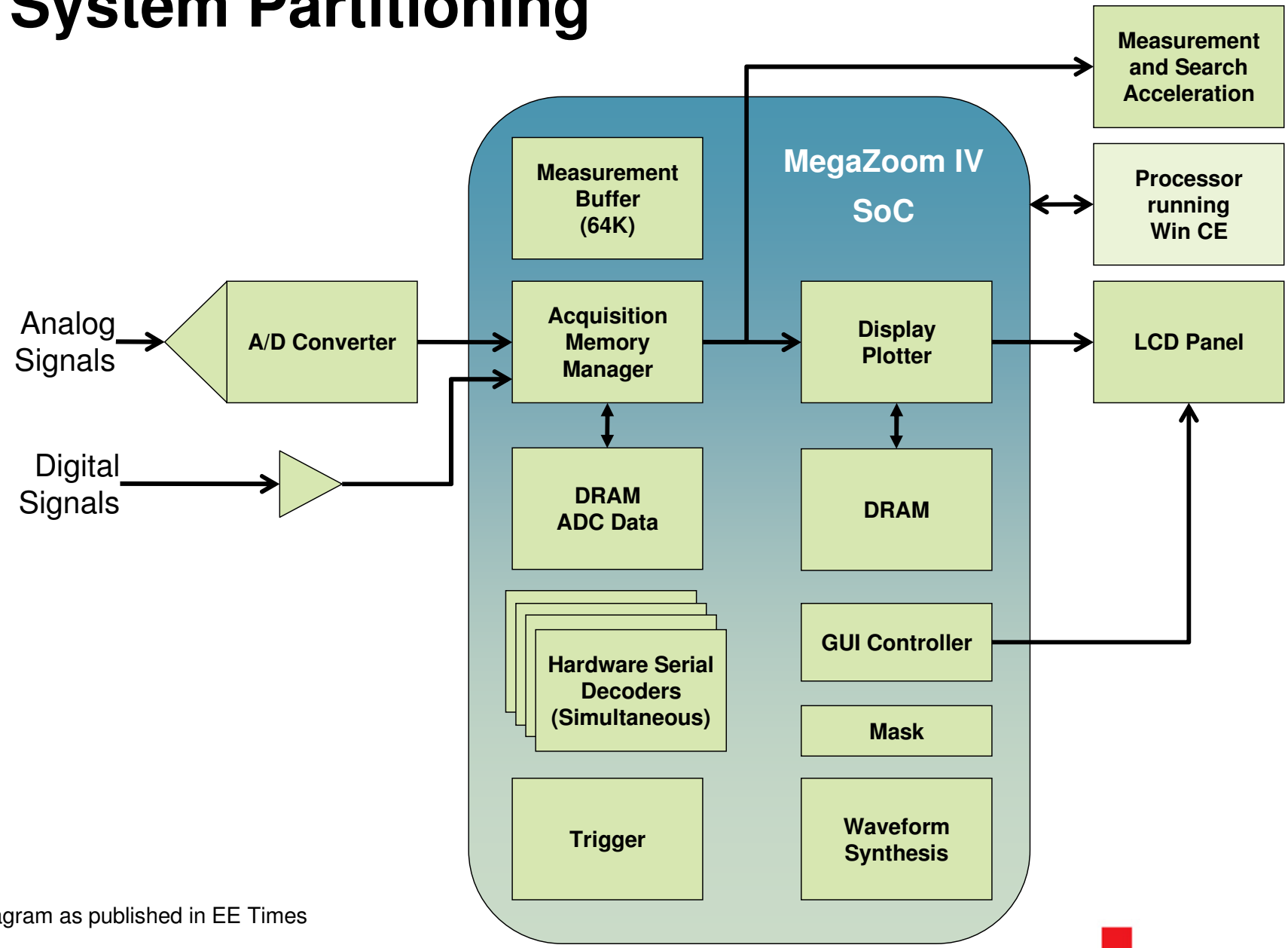


Diagram as published in EE Times

Agilent InfiniiVision 2000/3000 DSO/MSO System Partitioning

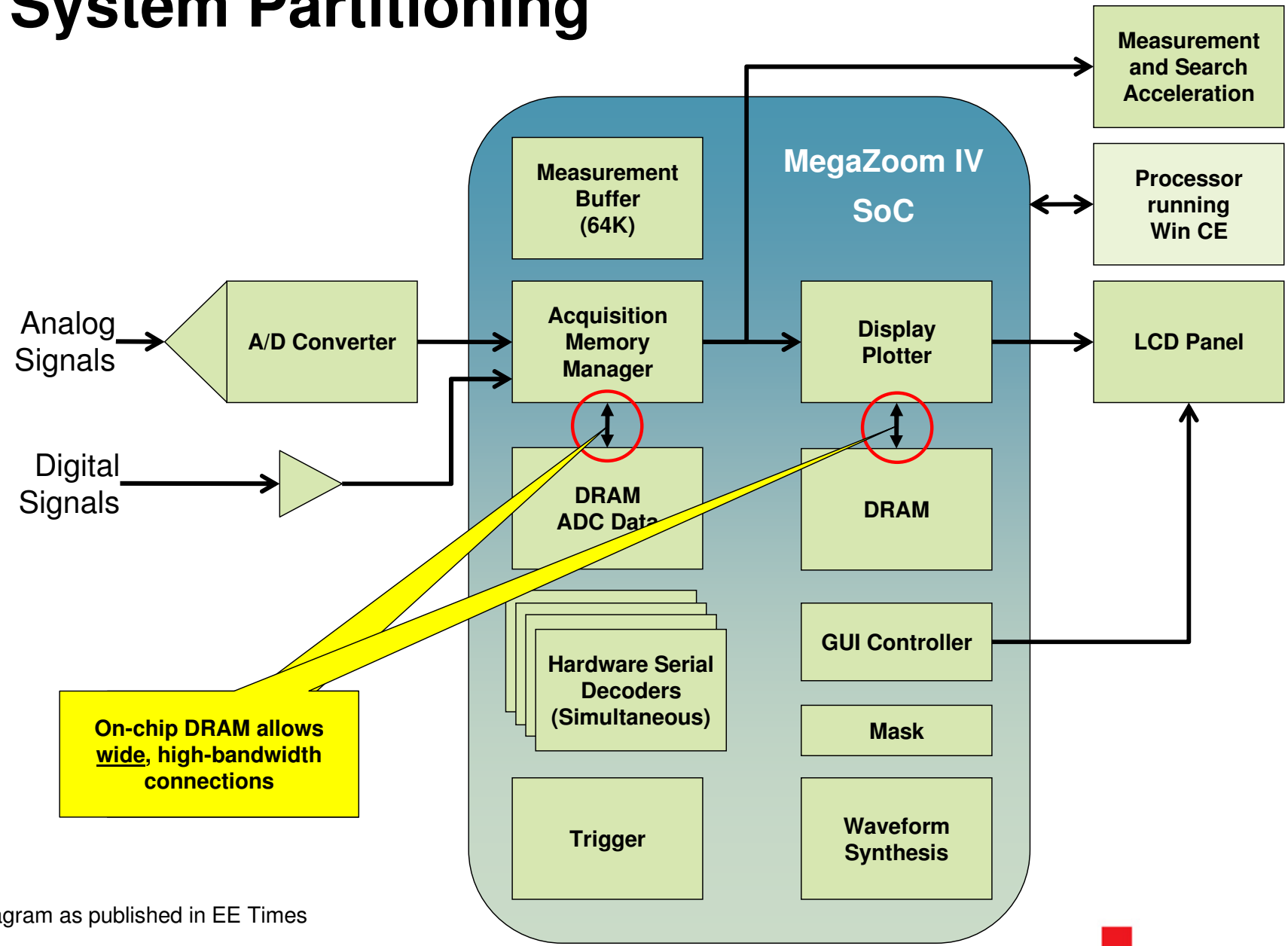
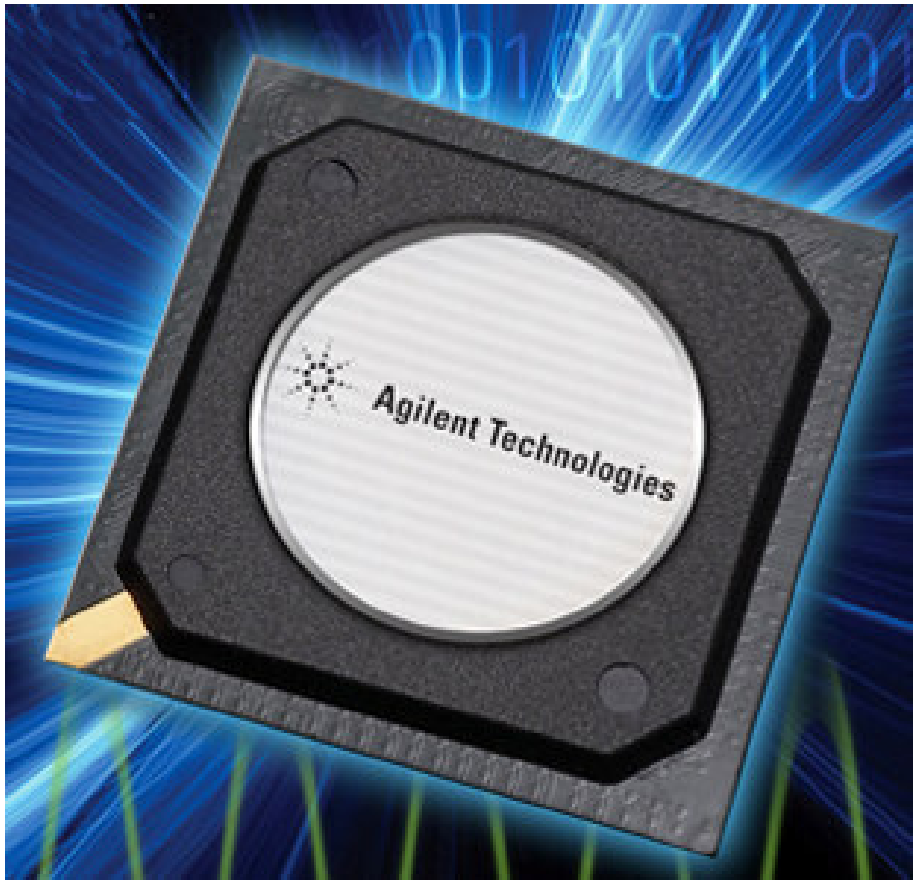


Diagram as published in EE Times

Agilent MegaZoom IV SoC



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Agilent InfiniiVision 2000 X-Series DSO Circuit Board

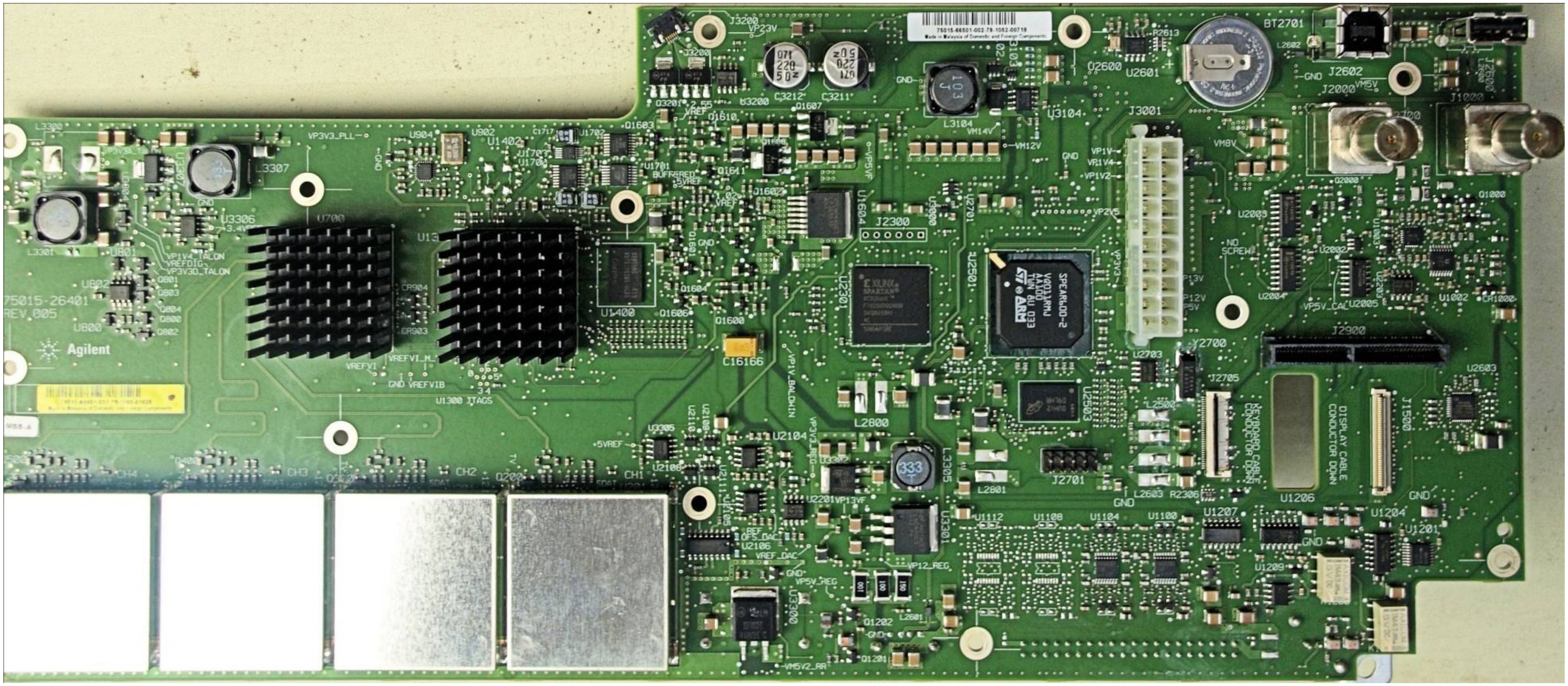

Image courtesy of David Jones, www.eevblog.com

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Agilent InfiniiVision 2000 X-Series DSO Circuit Board

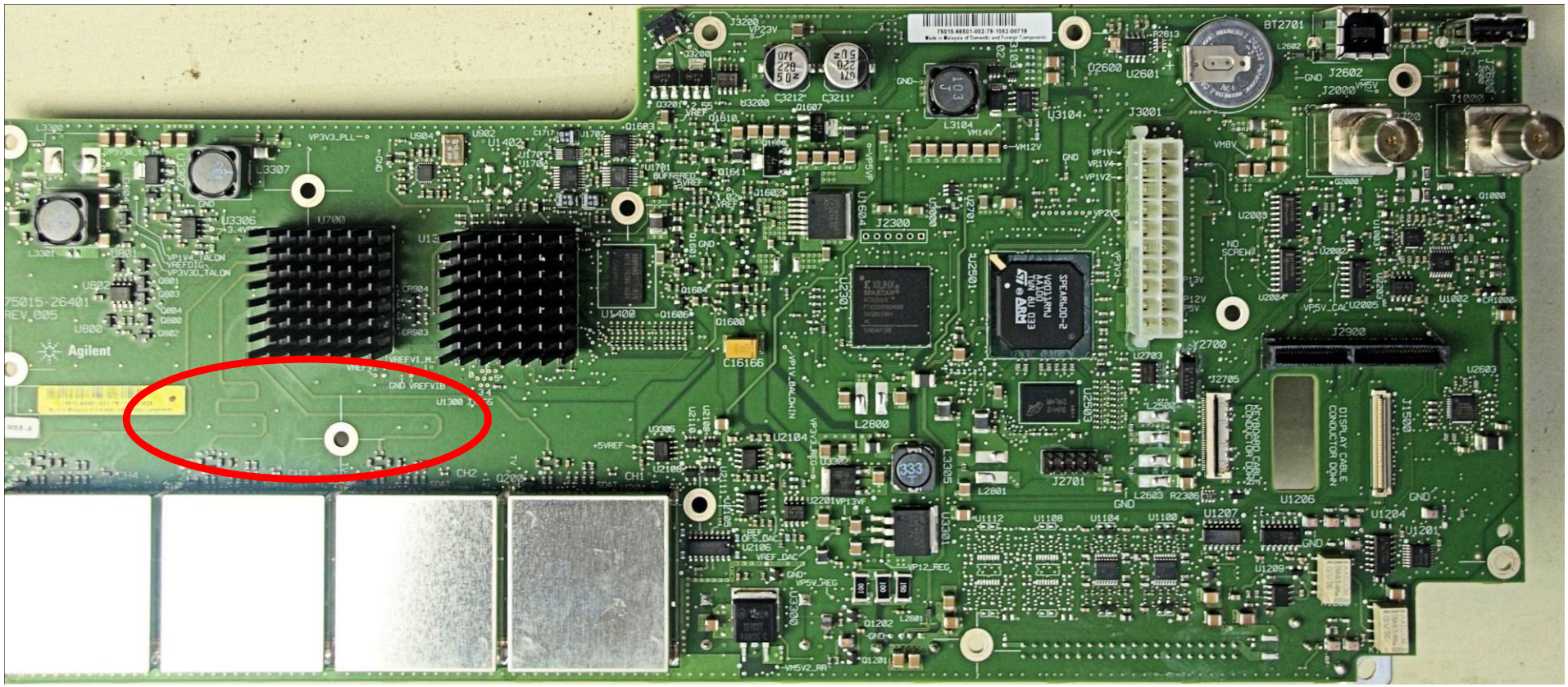

Image courtesy of David Jones, www.eevblog.com

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Detail: Board-Level Design Intent

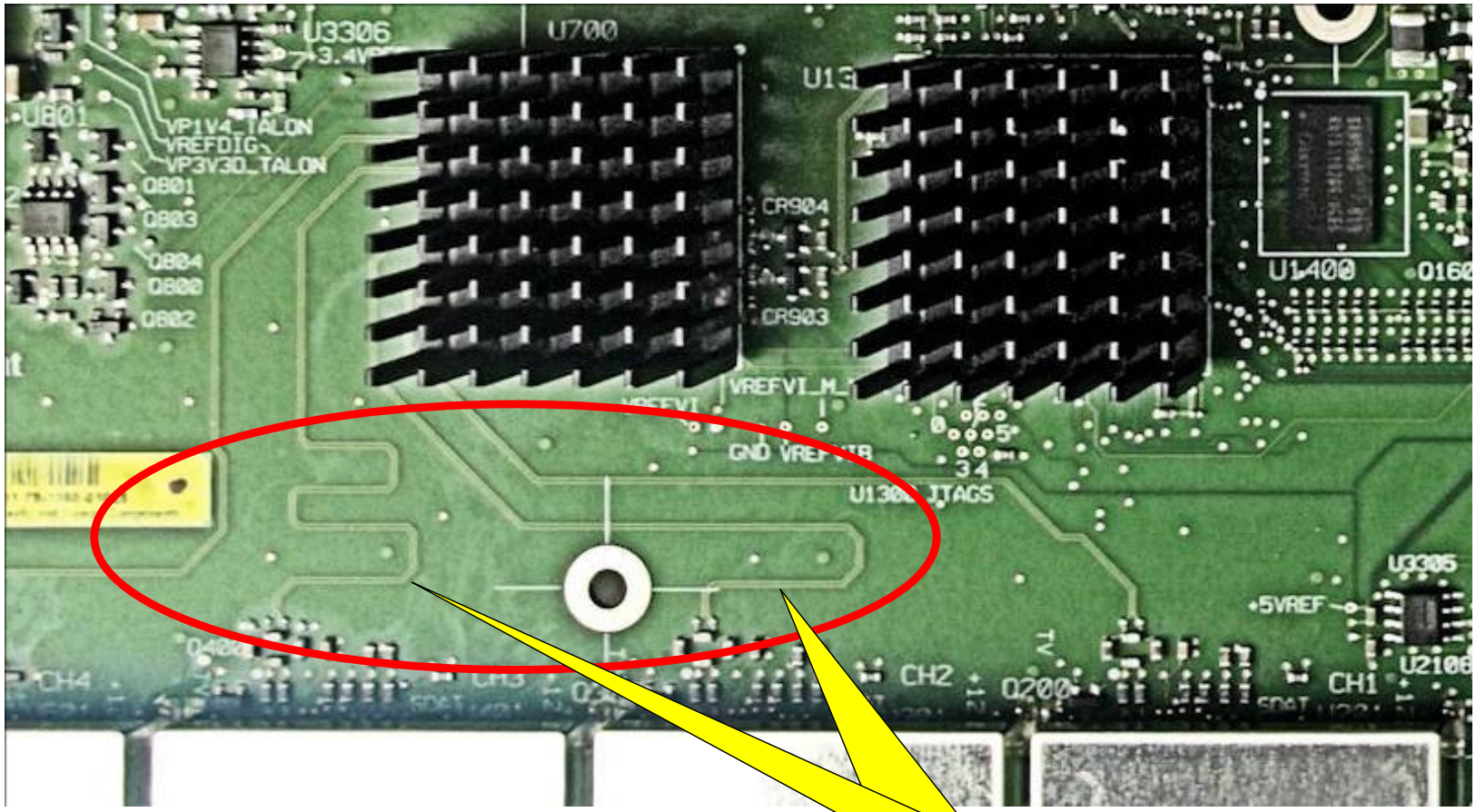

Image courtesy of David Jones, www.eevblog.com

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Agilent InfiniiVision 2000 X-Series DSO Circuit Board

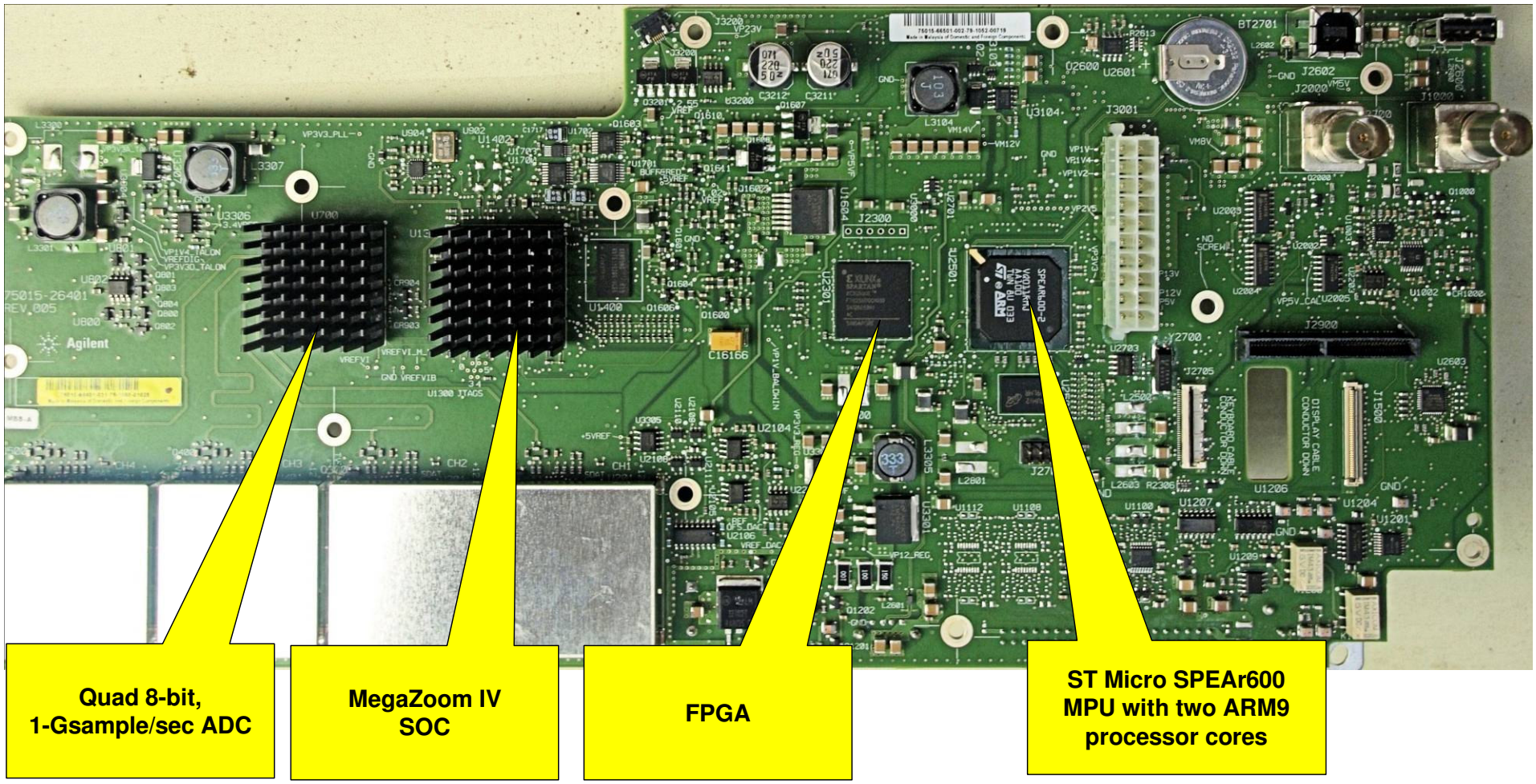
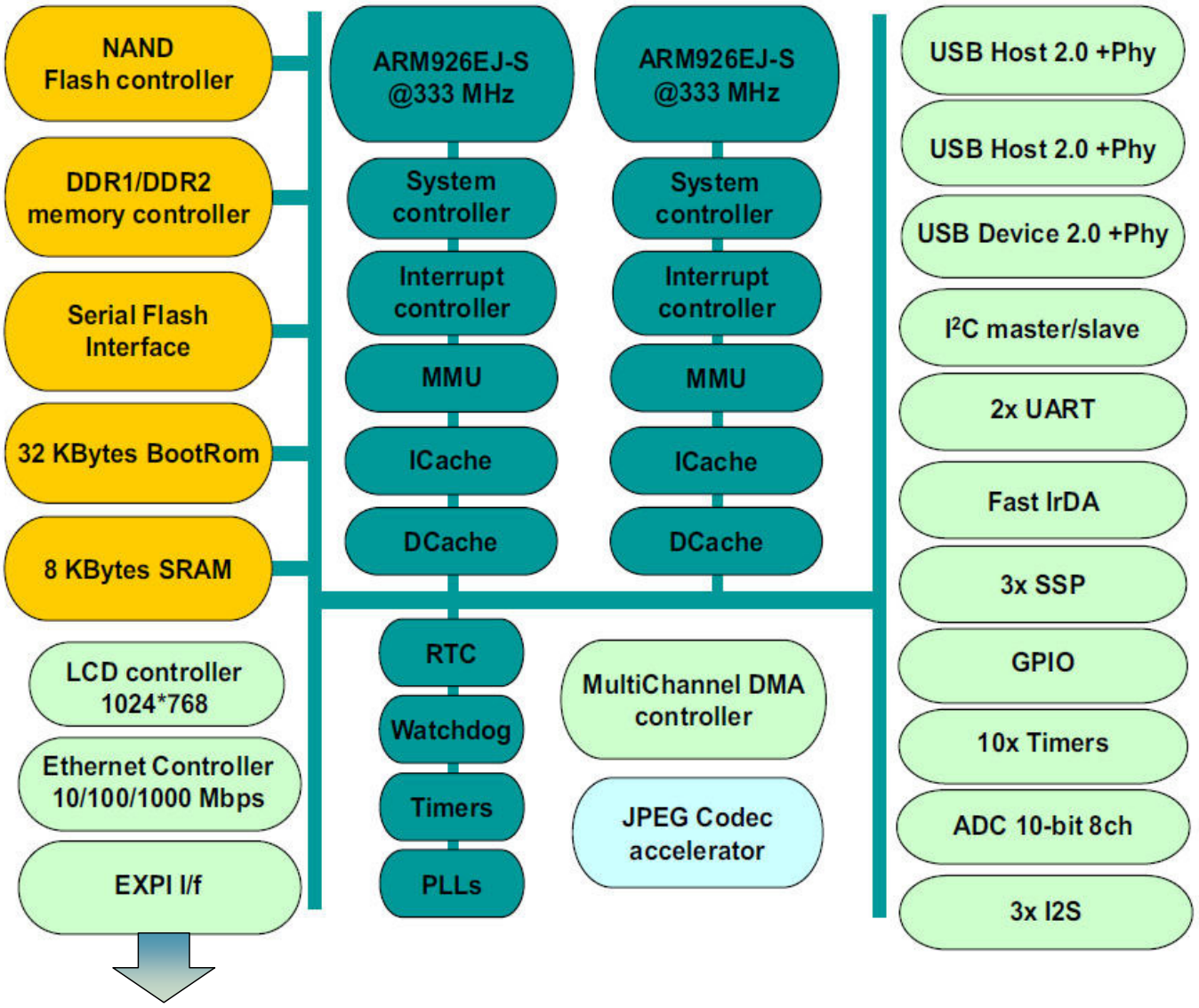
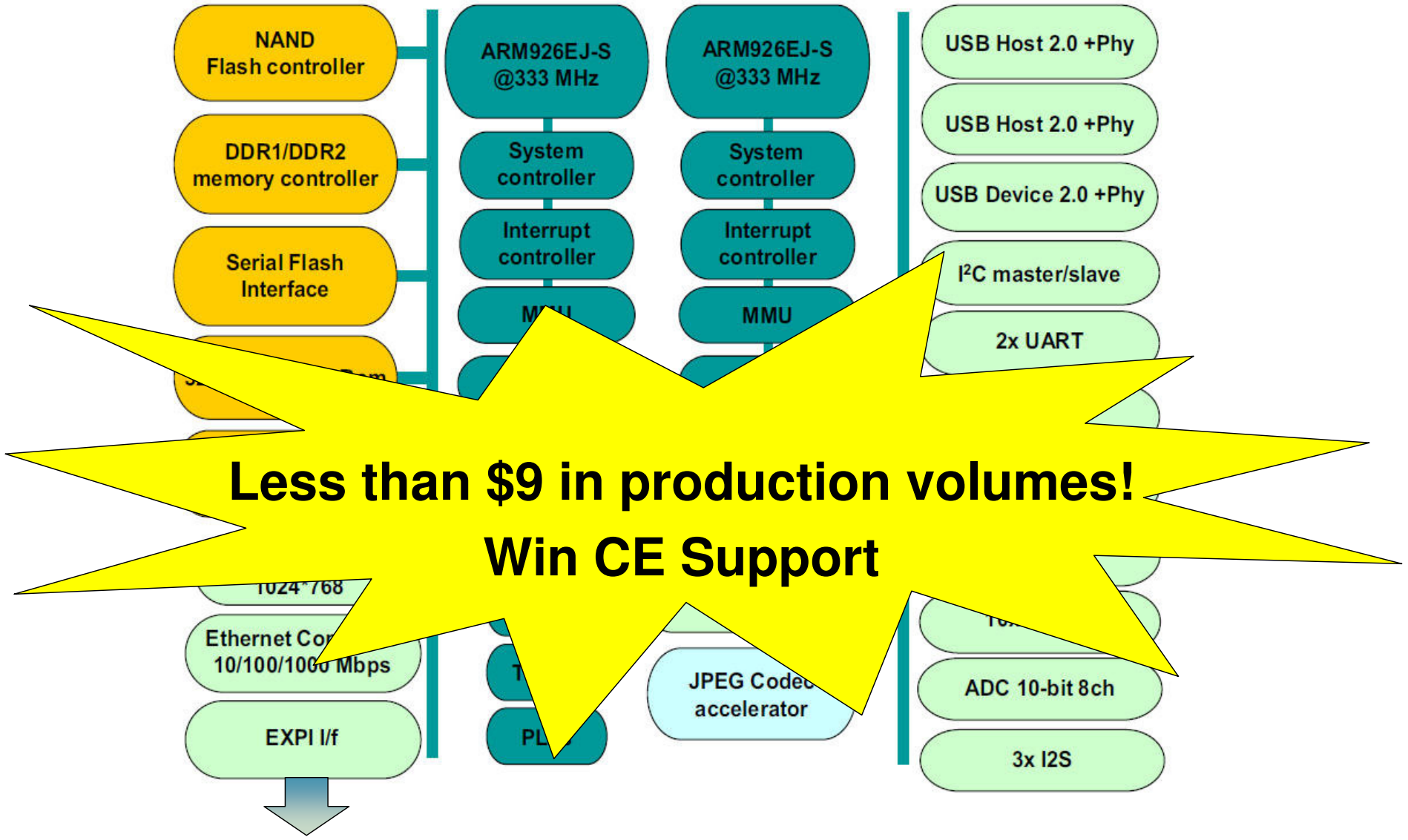


Image courtesy of David Jones, www.eevblog.com

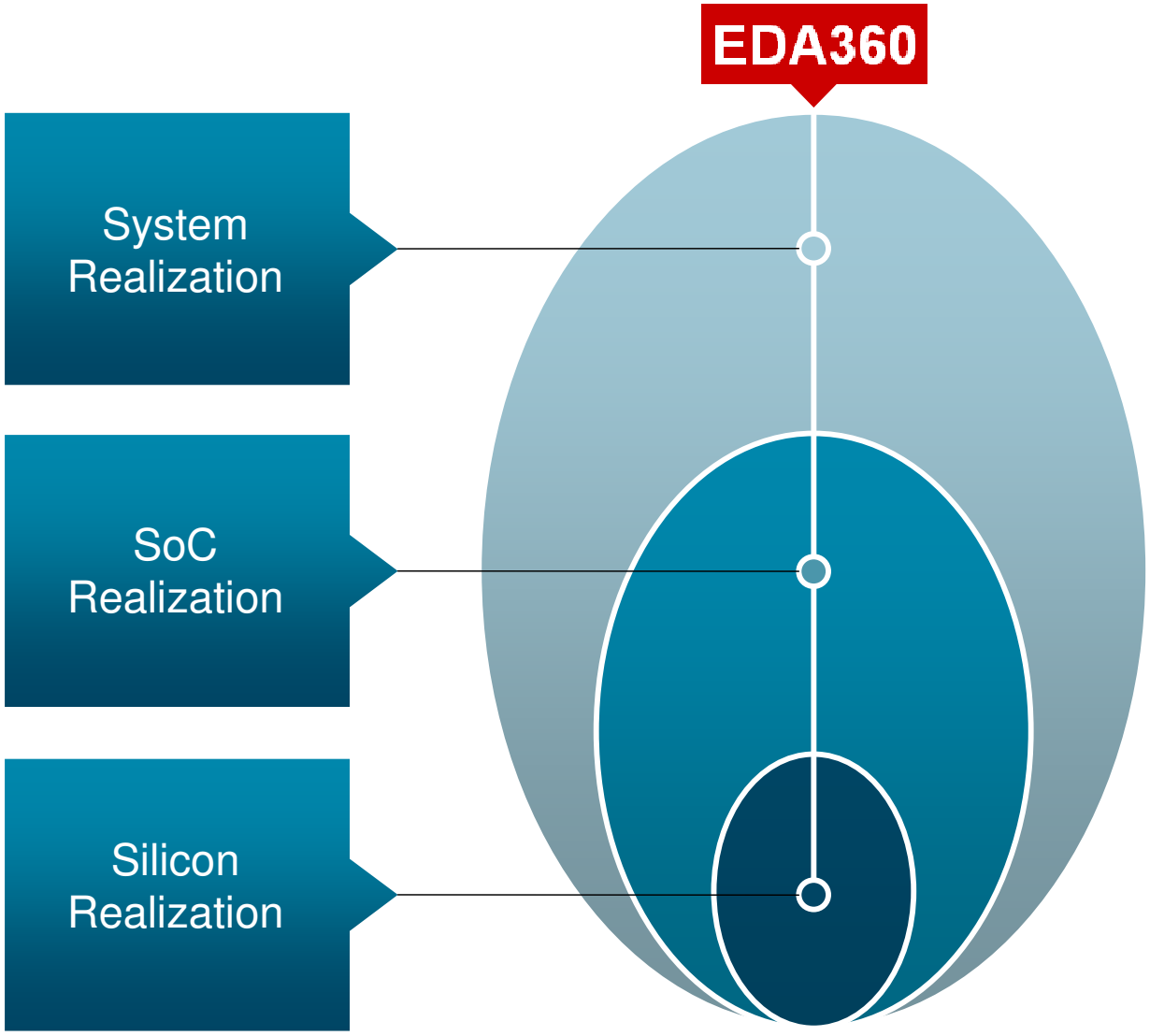
ST Microelectronics SPEAr600 Block Diagram

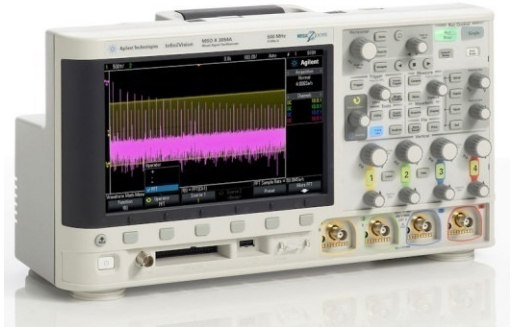


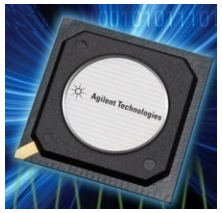
Why use an ST Micro SPEAr600?

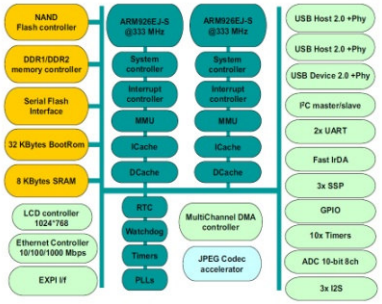


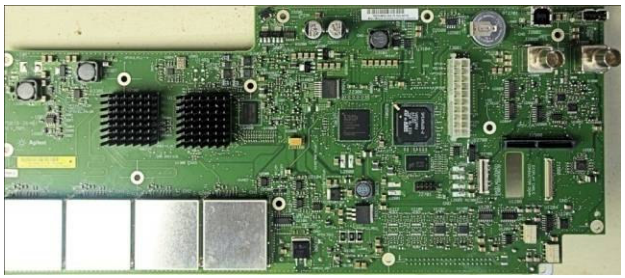
Three Key Pillars of EDA360











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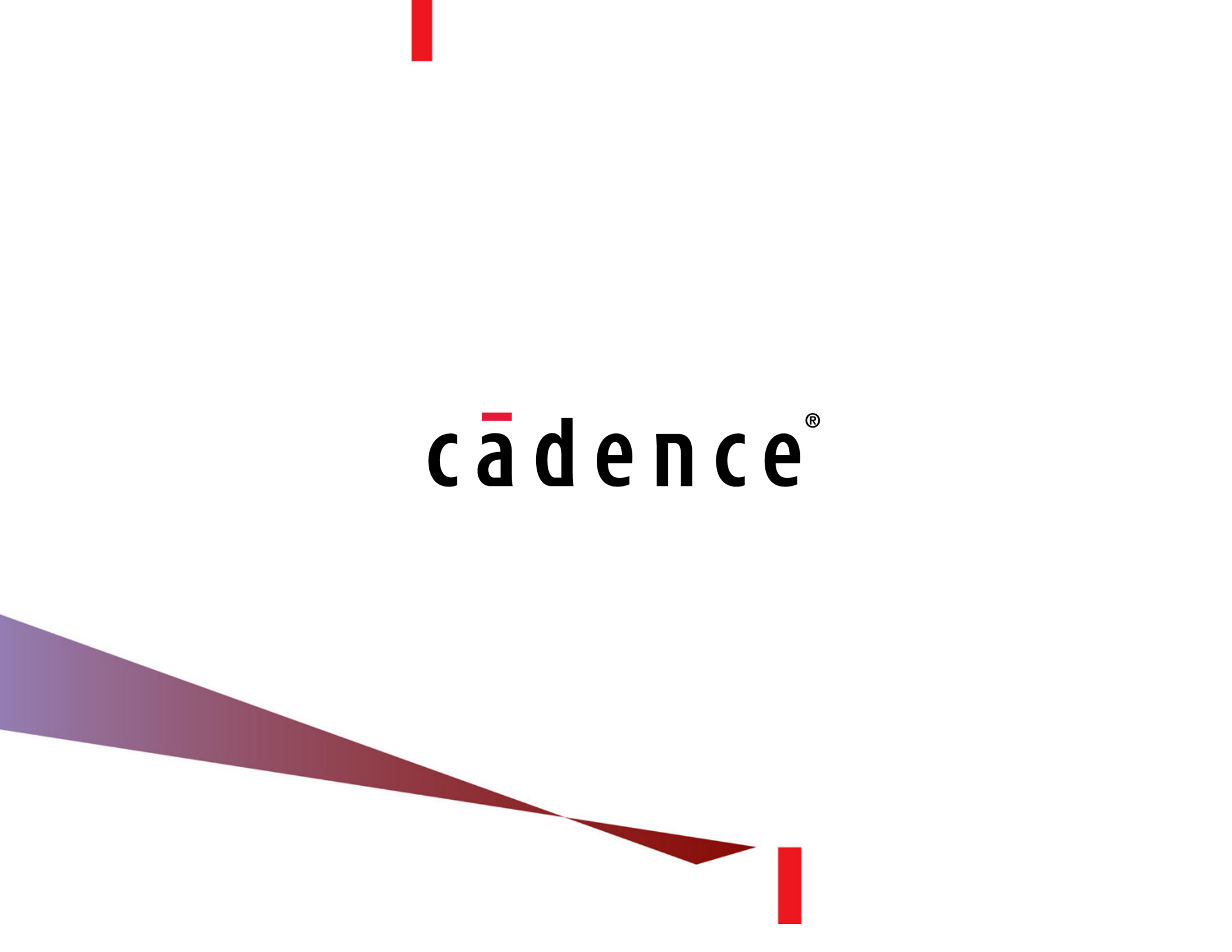
Questions and Answers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