MEMS and RF

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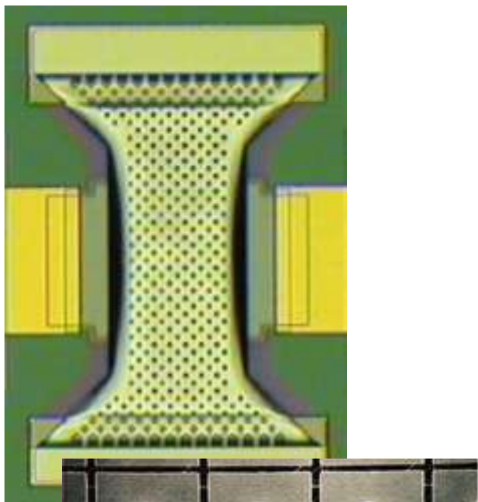
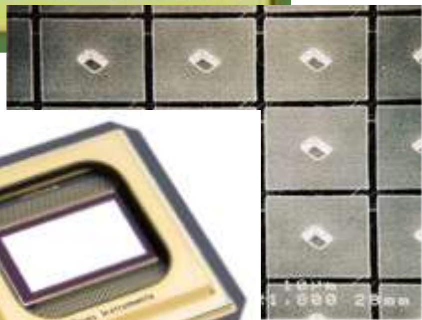
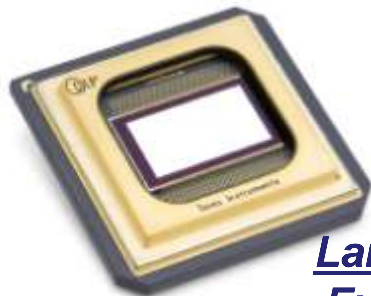
MEMS Technology Trend

Gen1: Build / Assemble

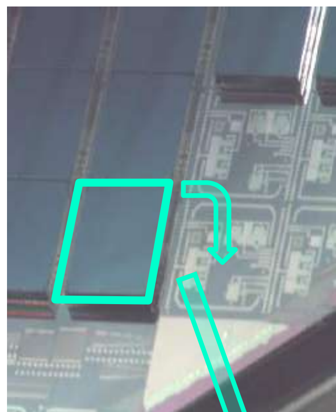






Large, Very Expensive

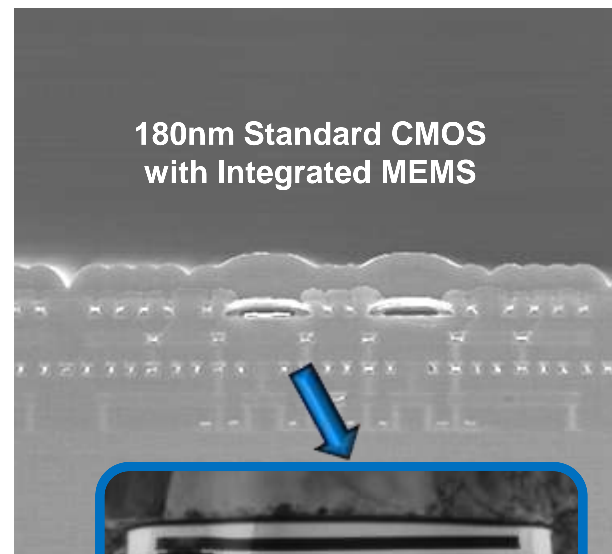
Gen2: Package in Package



Large, Expensive

Gen3: Fully Integrated

Cavendish 3rd Gen MEMS



Small, Integrated, Low Cost
No specialized tools/processes/materials

Cavendish MEMS encapsulation provides superior cost & reliability

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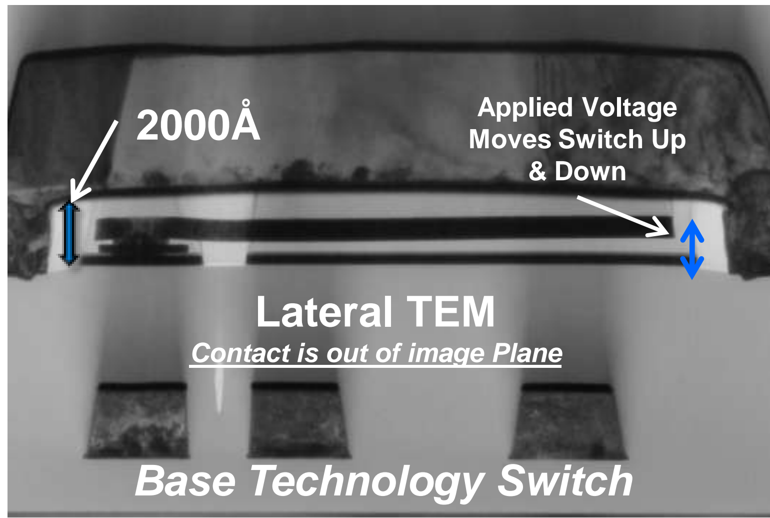
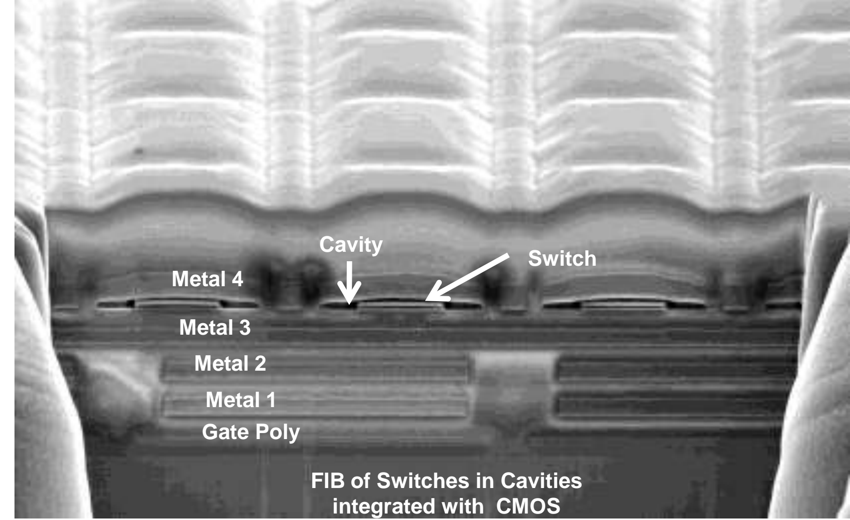
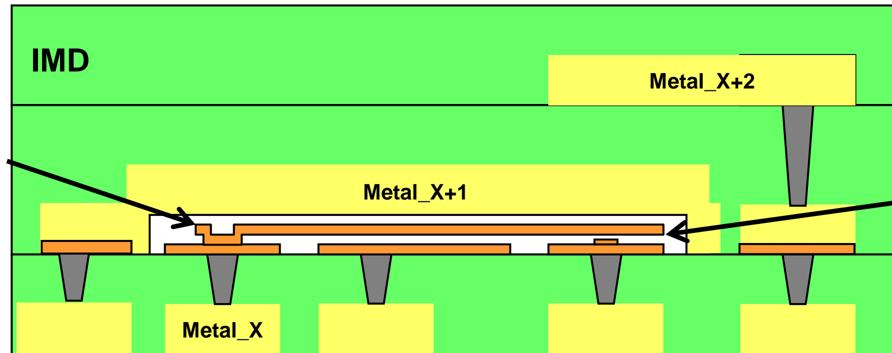
Core Technology: 3rd Gen MEMS





MEMS Technology

- Metal Based MEMS
- Cantilevers
  - Metal Logic
  - NV memory
  - Sensors
- Digital Variable Capacitor
  - Robust MEMS Design
  - Compact Routing
  - Small Die Size



Integrates into Standard Flow

Cavity

- Package Free MEMS
- Non Contaminating
- CMOS Processes
- Planarized Interconnect
- Controlled Release Design
- Electrically Active Roof
- Roof: Metal or Dielectric
- Via Electrical Connections

CMOS Compatible Package Free MEMS, Using Standard Interconnect Technology

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- **Mission: Enable our Customer to Deliver Breakthrough Products**
  - *How:* Enable integration of devices and sensors never before possible
  - *Results:* Lower cost, lower power and smaller size
  - *Means:* Standard semiconductor processing technology
- **NanoMech™ Technology Platform – 3rd Generation MEMS**
  - Fully integrated into the process flow
  - No unique equipment or materials or packaging
  - Capability of Delivering Multiple Applications on the same IC

Enable our Customers to Deliver Enhanced Value Products with MEMS Technology

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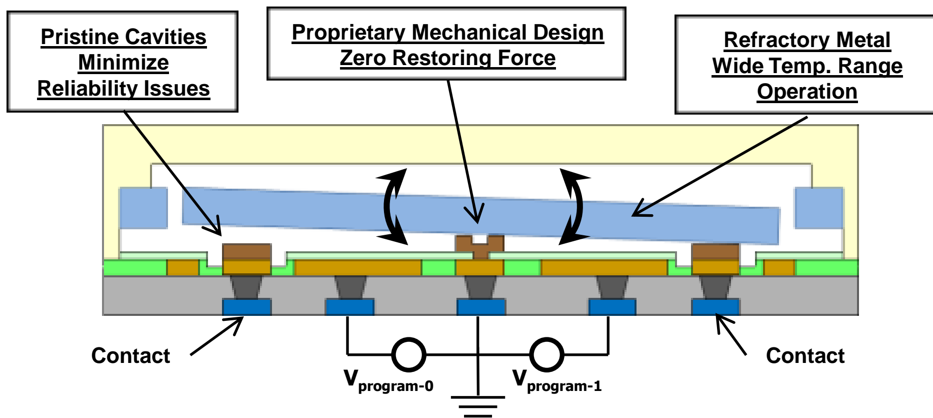
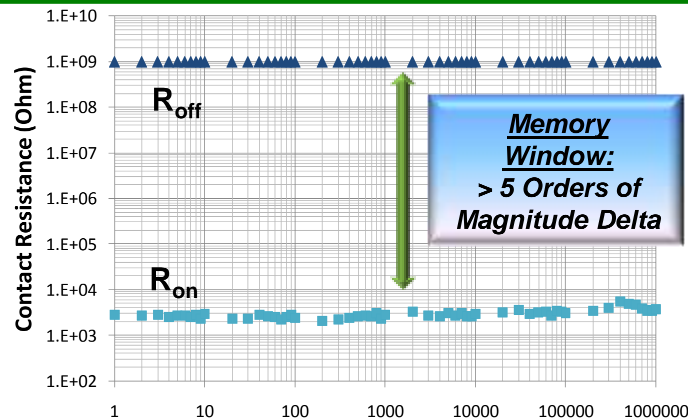
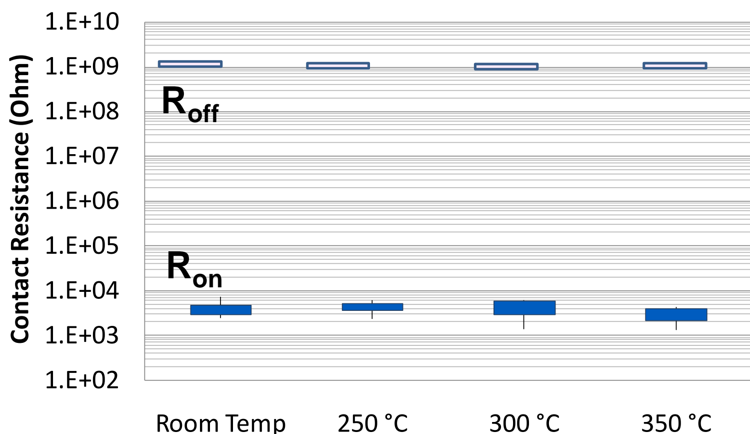
Cavendish Core Design Technology



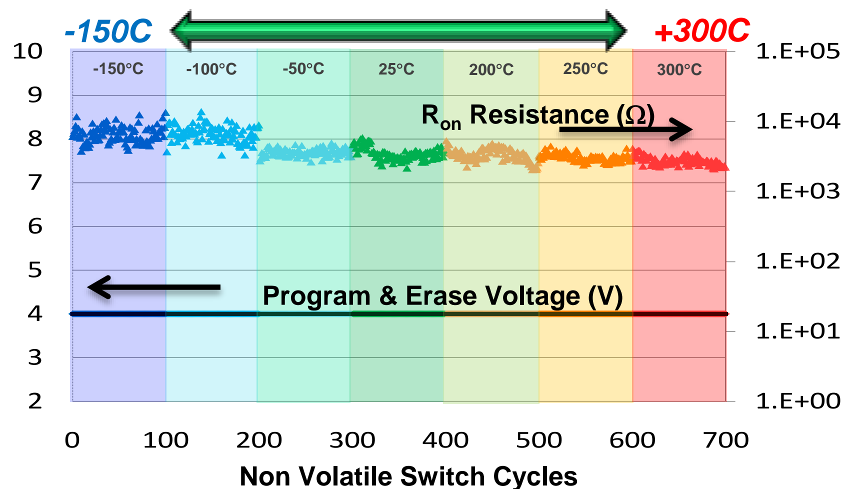
Design Schematic



Performance (No Change in Program / Un Program)



No Effect on Retention vs. Storage Temp up to 350°C



Wide Temperature of Operation -150°C to +300°C

NV Switch Performance Demonstrates Robustness of Technology

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Data Volume Forecast: Wireless Operators Have a Problem

Broadband Penetration and Traffic for Wireline and Mobile (US)

Source: Chetan Sharma Consulting

Wireless devices will need better performance = Opportunity

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Carrier Economics Dilemma…

Traffic Volume

Network Cost
Existing Technologies

Will Do What ever it takes
to Change Cost Curve

Revenue

Profit

Desired
Network
Costs

Carriers:
Pushing entire supply chain to enable more network capacity and reduce costs

Voice Dominated

Data Dominated

Source: Nokia-Siemens and AT&T

Adding Bands, Adding Complexity, Adding Requirements

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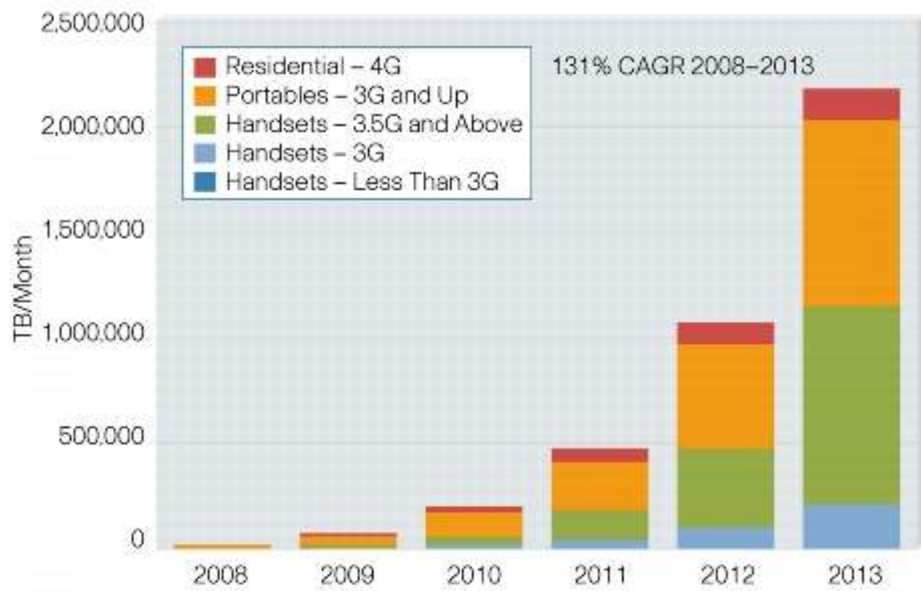
What is the Reason and Breakdown…

Uses = 30 Phones of Voice Bandwidth



Data Source: Cisco Systems White Paper Feb 2009

Data is swamping the networks as smart devices are adopted…

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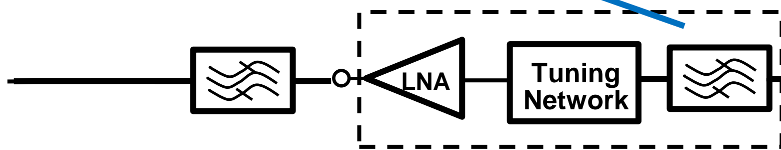
Areas for Applications in FEM

Impedance Matching & Capacitance Loading

Simplified FEM

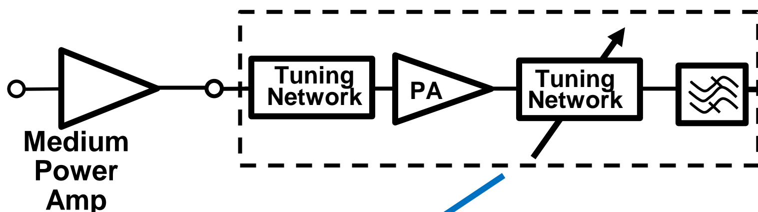
Future: Tunable Filters



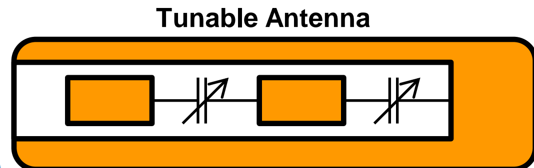
Future: RF Switches

Switch

Tuning Network



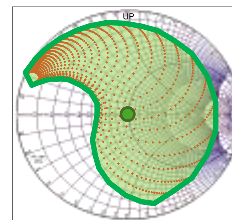
Tunable Antenna

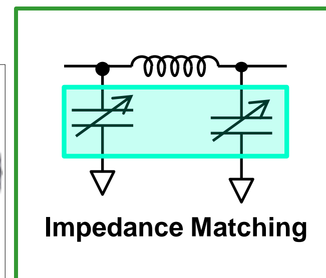


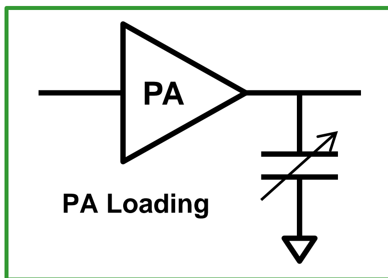
Enables:

Greater Bandwidth
Higher Gain

First Product







Enables:

Improved Efficiency at
Multiple frequencies and power levels

Enables:

Increased Bandwidth, Gain
Reduced Power
Lower System Loss

We have the opportunity to Win Multiple Sockets (3 to 5), reducing BOM costs by Multiple Dollars with Smaller Size and Superior Performance

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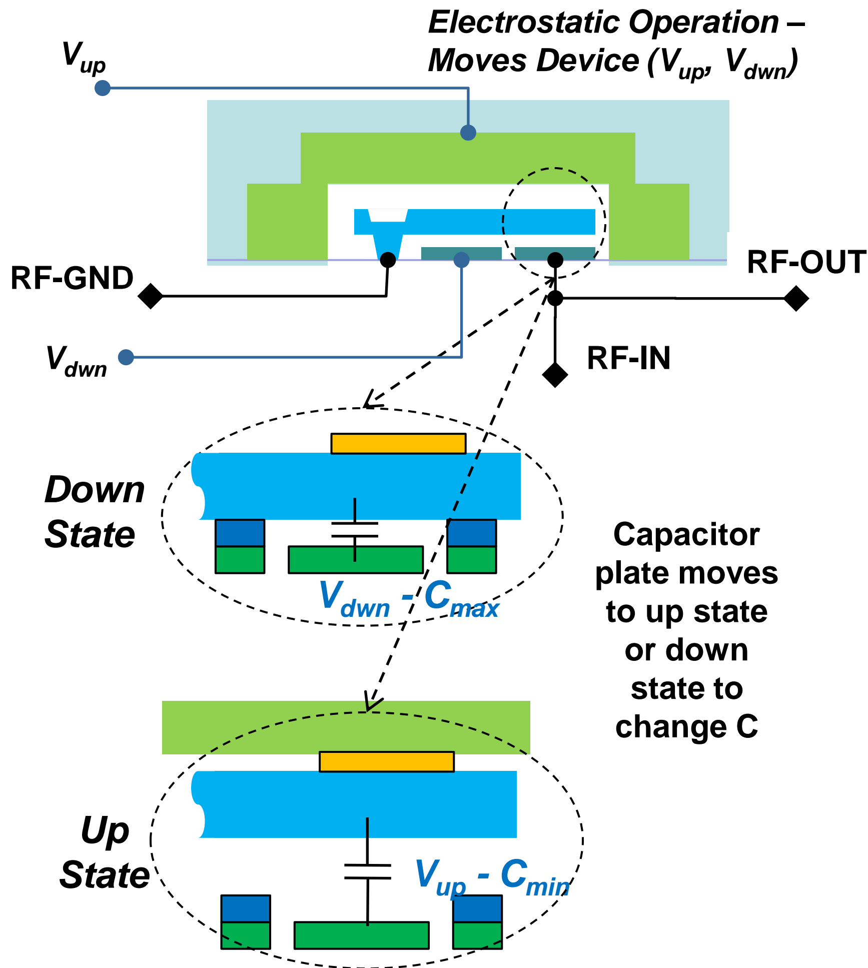
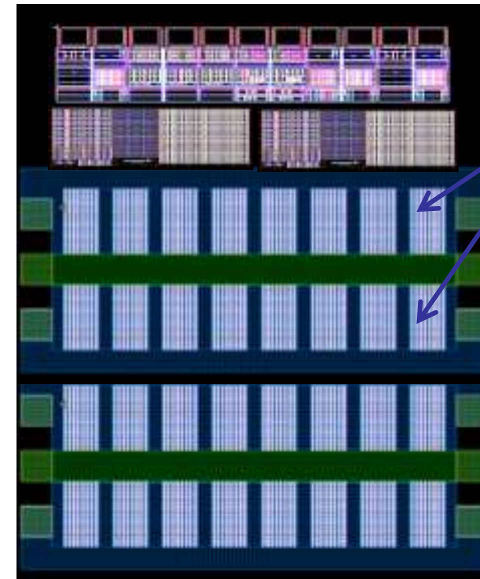
Nanomech™ Based Variable Capacitor Device

CROSS-SECTION VIEW – Unit Cell



Capacitor plate moves to up state or down state to change C

Array of Cells – Digital Variable Capacitor



Arrays of capacitors create digitally controlled variable capacitor

Bumped, Bare Die
No Package

Variable Capacitor:

- ✓ Total capacitance is the sum of all the caps
- ✓ Each Capacitor unit individually controlled to be either Up or Down
- ✓ **Result**: High resolution with linear response

Array of Capacitance Switches operated as one Variable Capacitor

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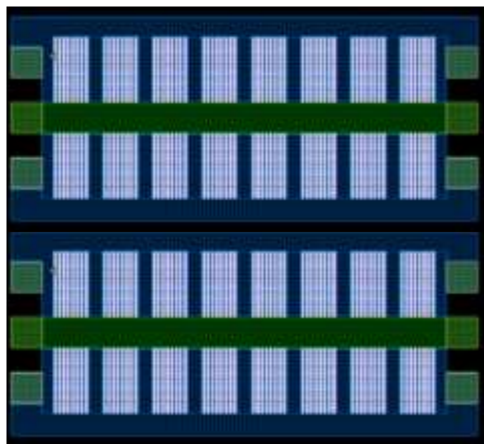
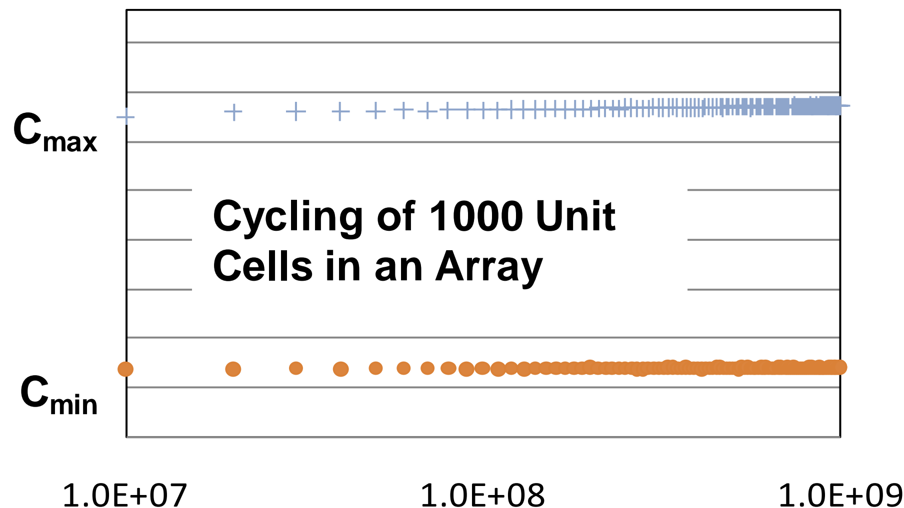
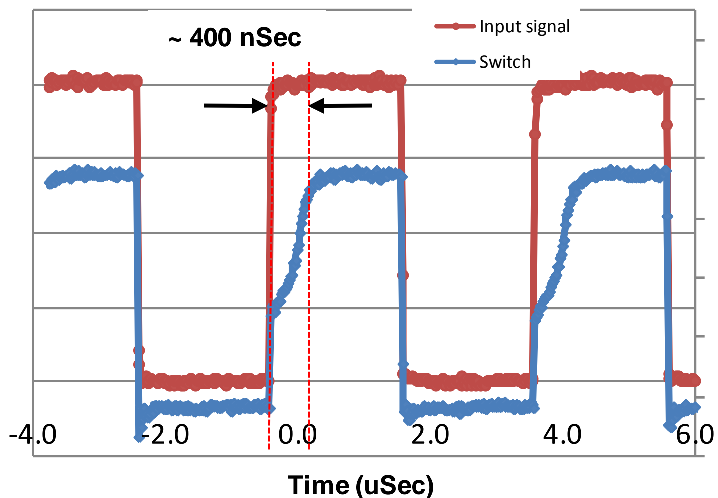
Measured Data

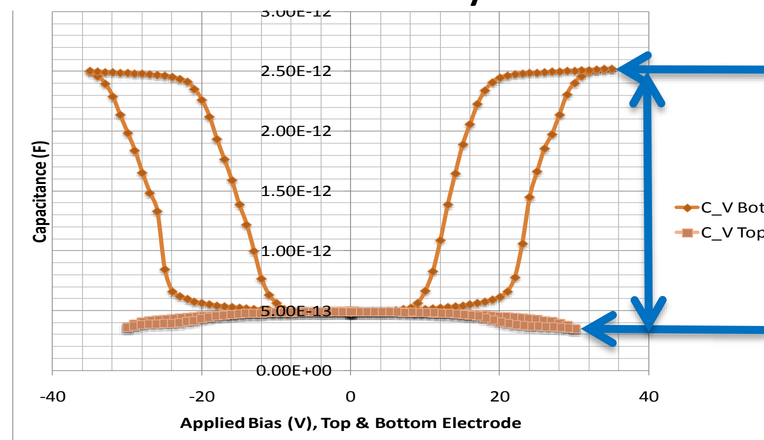


C_{MAX} & C_{MIN} Cycling to 1 Billion Cycles



Capacitor Array Switching Speed





Array of *"Small Switches"* Enables Reliable Fast Variable Capacitor Array

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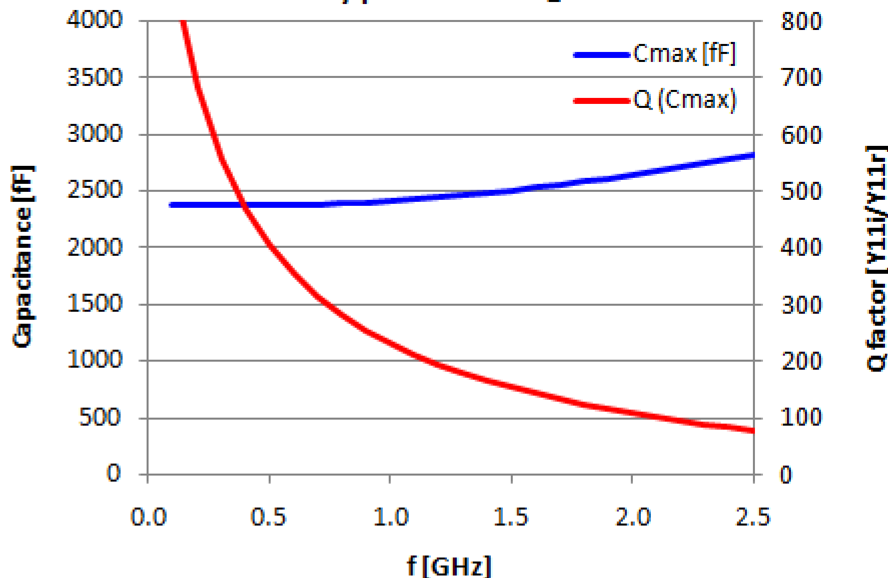
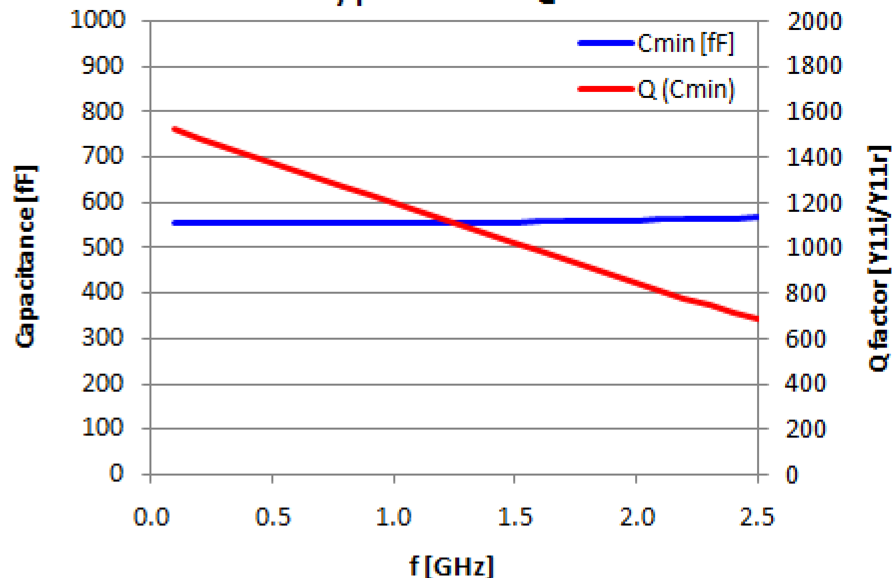
Sample simulation results
(5:1 design)

- **<u>Design example targets</u>:**
  - 5:1 high hot-switch MEMS design (45Vrms)
  - Q = 100 at 2GHz
- **Performance estimate includes effect of bumps and copper traces on RF board (total series inductance ~ 130pH including copper trace on RF board)**

> - ***Capacitance ≡ Y11i/(2*pi*f)***
> - ***Q factor ≡ Y11i/Y11r***





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DVC CAD DESIGN FLOW

MEMS CELL DESIGN — HFSS,COMSOL, CST

MEMS ARRAY DESIGN — SONET, ADS

PACKAGE DESIGN — SONET, ADS

MIXED MODE SIMULATOR

RF MEMS CTL DESIGN — Spice/RF simulator

RF Digital Controller DESIGN — NC Verilog, P&R

IO DESIGN — spice

Many different tools have to work together

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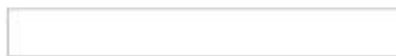
DVC CAD Tool at Cell Level

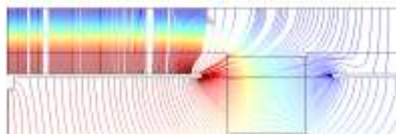
CELL DESIGN

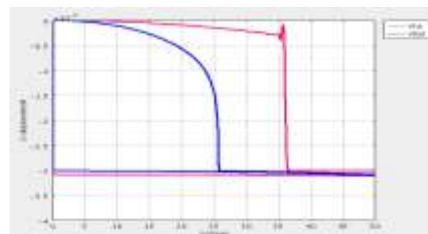
Electrostatic Simulation

CELL DESIGN

Electro-mechanic Simulation







Crf-gnd, Crf-pi, Cpi-gnd, Ccap-gnd, …Cratio

Vpi, Vhs, Vrel, Vpu

Cell design requires different simulators

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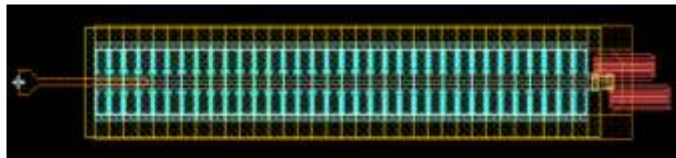
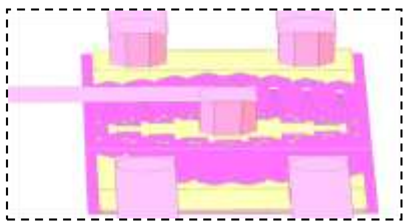
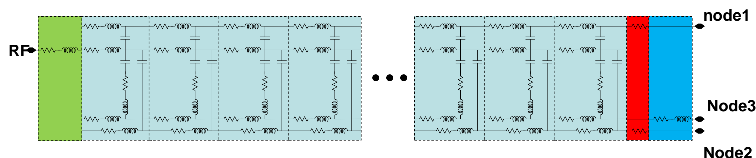
DVC CAD Tool at Array/Chip/Package levels

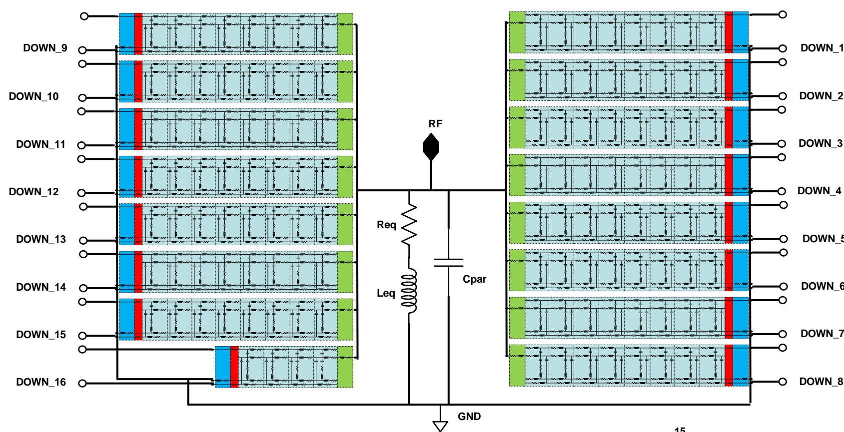


Package R,L,C





Interconnect R,L,C



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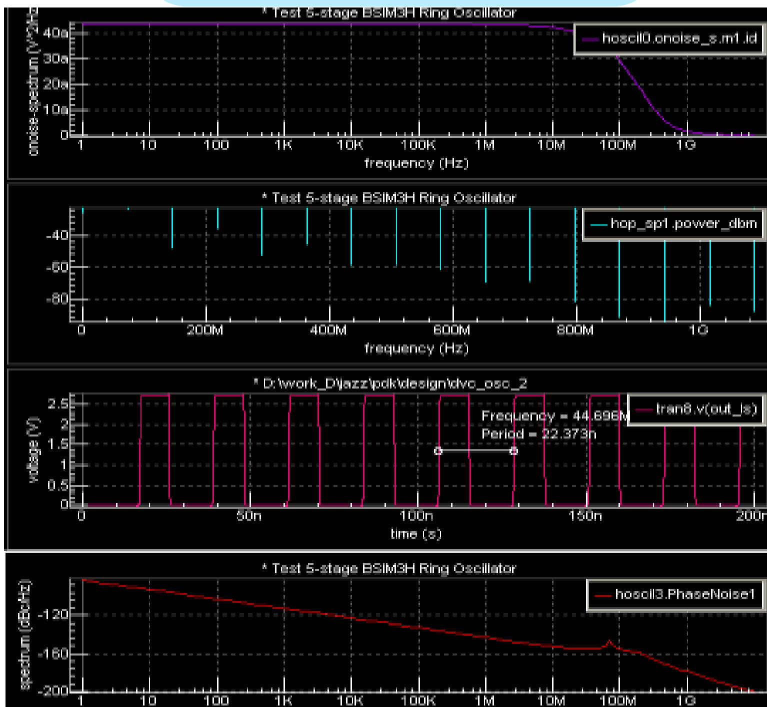
DVC Circuit/RF simulators

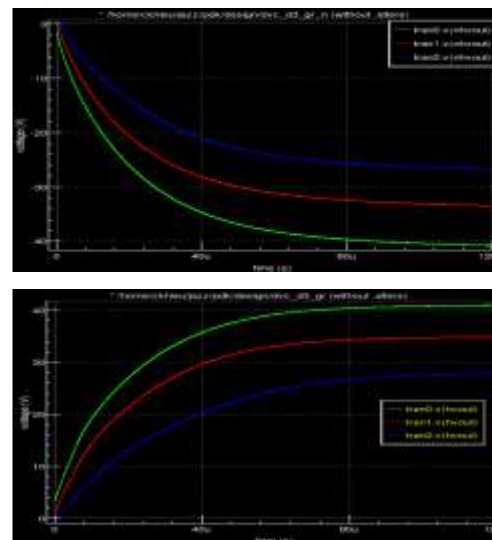
Charge Pump DESIGN

RF Simulator

Charge Pump DESIGN

Circuit Simulator





Pnoise, onoise, harmonics

posHV, negHV

Power, timing, S-paramaters

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Summary

- **RF front end limits the cell phone scalability to many bands**
- **MEMS provide solutions for:**
  - Antenna tunable matching network, or band select
  - High power handling, Very linear, no harmonics, low cost
- **MEMS + CMOS CAD Flow requires:**
  - Many different CAD tools and sometimes manual edits are required
  - There are room for CAD Design Flow Improvement

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