Mechanical Computing Redux: Relays for IC Applications

Tsu-Jae King Liu

Electrical Engineering and Computer Sciences Department
University of California at Berkeley

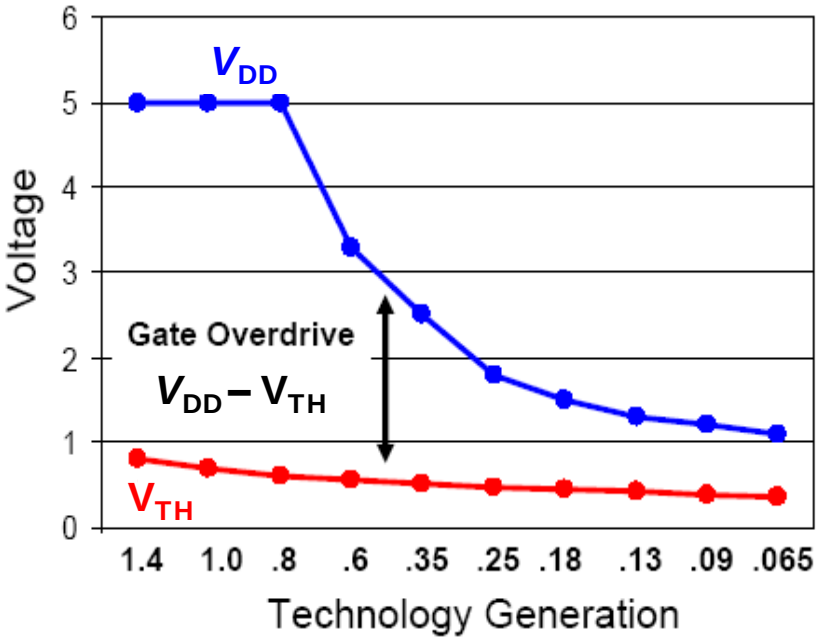
Collaborators: Elad Alon (UC Berkeley)
Vladimir Stojanovic (MIT), Dejan Markovic (UCLA)

Power Density Scaling – NOT!

- Due to off-state leakage, V_{TH} cannot be scaled down aggressively. Thus, the supply voltage (V_{DD}) has not been scaled down in proportion to the MOSFET channel length.

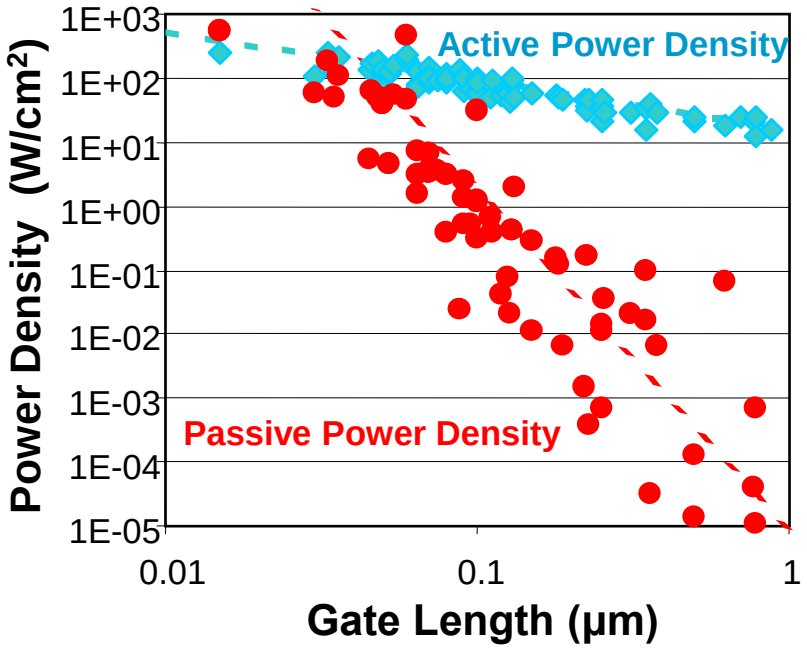
→ CMOS power density has increased with transistor scaling!

CMOS Voltage Scaling



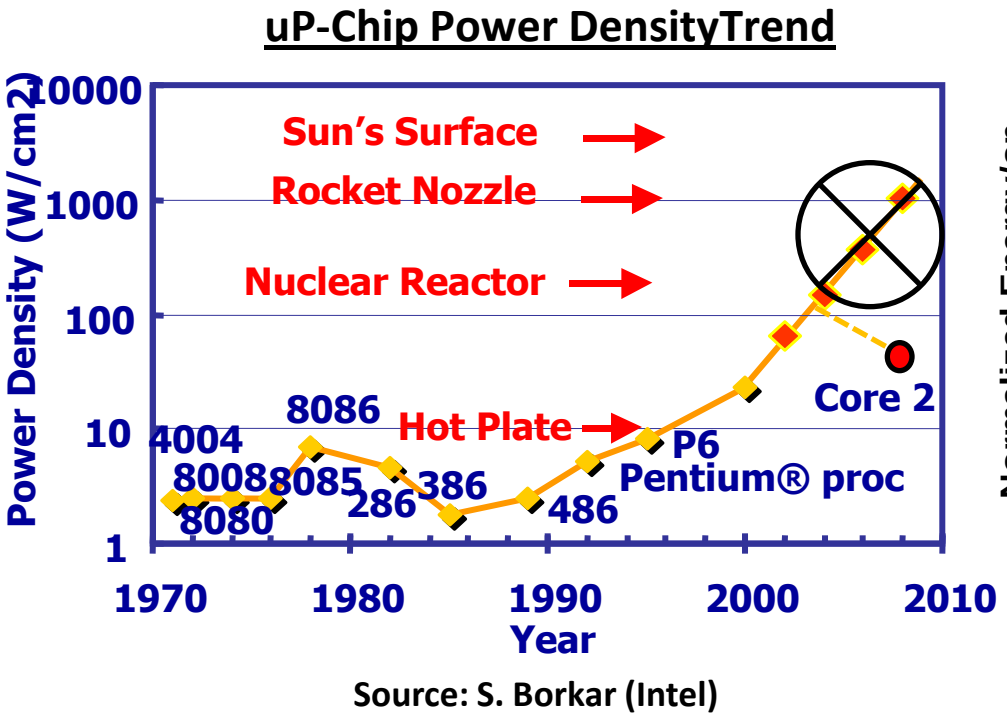
Source: P. Packan (Intel), 2007 IEDM Short Course

Power Density with CMOS Scaling

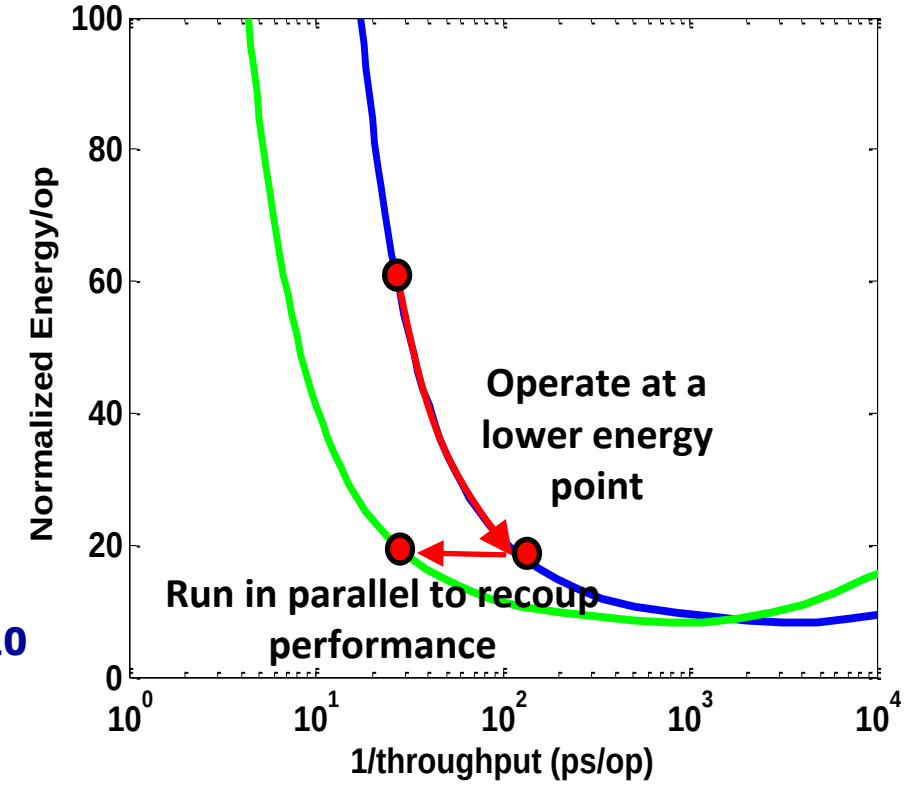


Source: B. Meyerson (IBM) Semico Conf., January 2004

Parallelism

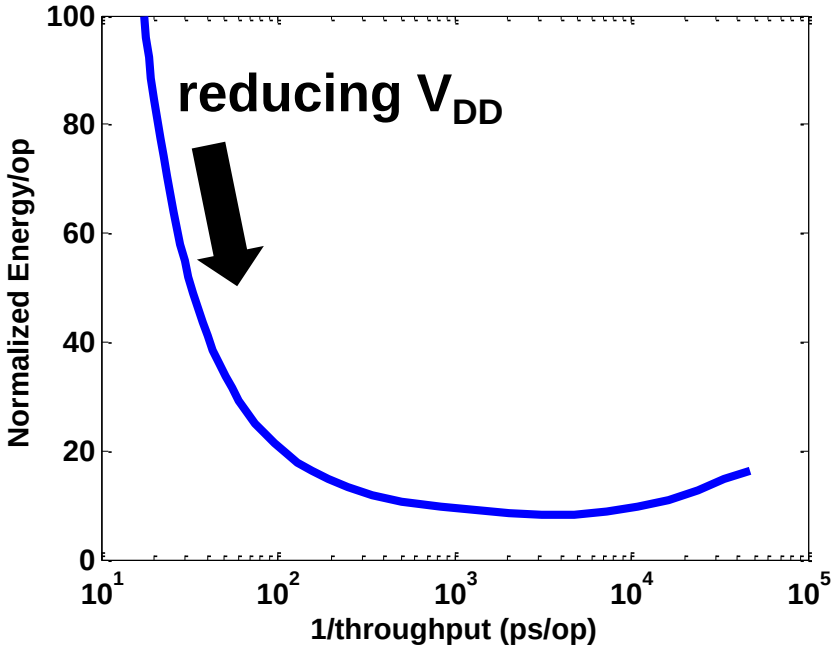


Source: S. Borkar (Intel)



- **Parallelism is the main technique to improve system performance under a power density constraint.**

CMOS Energy *vs.* Delay



- **CMOS (and CMOS-like) technologies fundamentally have a lower limit in energy per operation, due to off-state leakage (I_{OFF}).**

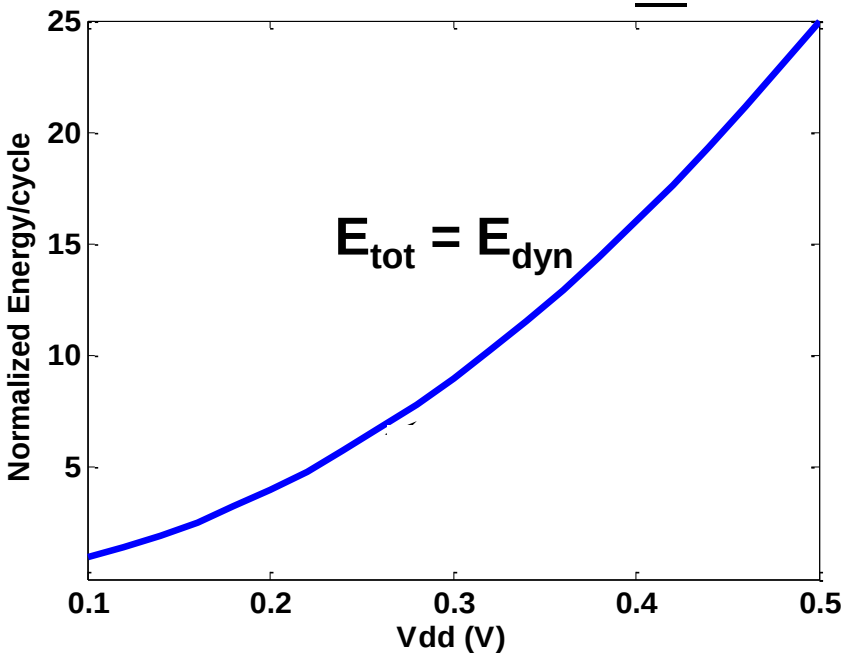
$$E_{total} = E_{active} + E_{leak} = \alpha L_d C V_{DD}^2 + L_d I_{OFF} V_{DD} t_{delay}$$

$$t_{delay} = L_d C V_{DD} / (2 I_{ON})$$

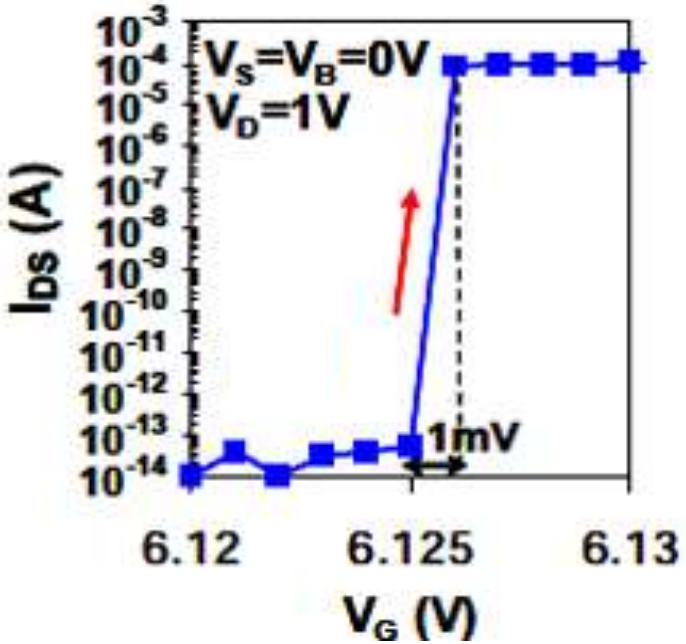
α = activity factor; L_d = logic depth; C = capacitance per stage

What if There Were No Leakage?

Energy/op vs. V_{DD}



Measured MEM Relay I-V*

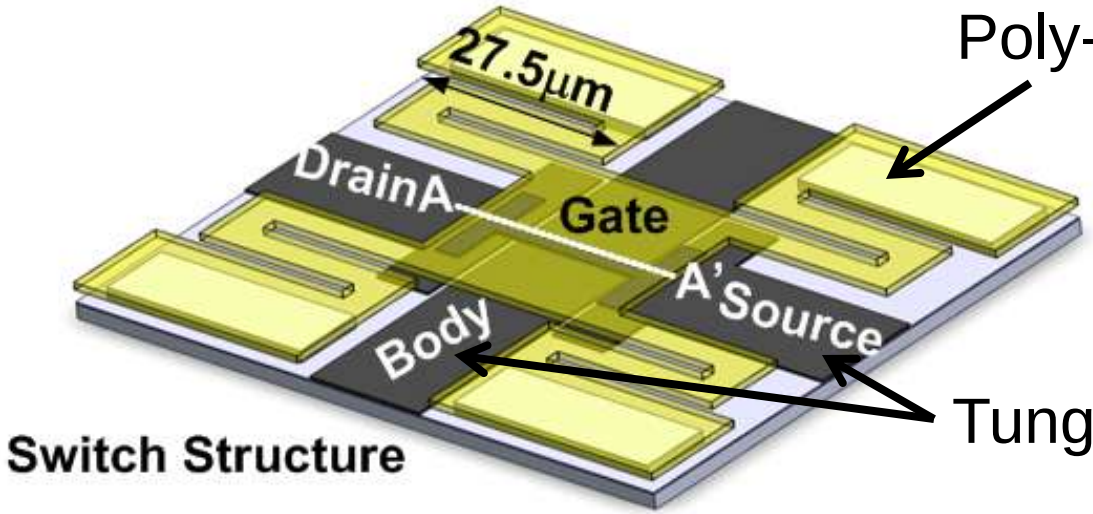


- V_{DD} decreases → energy decreases
- Mechanical switch offers zero leakage current and steep switching behavior

*R. Nathanael *et al*., "4-Terminal Relay Technology for Complementary Logic," *IEDM 2009*

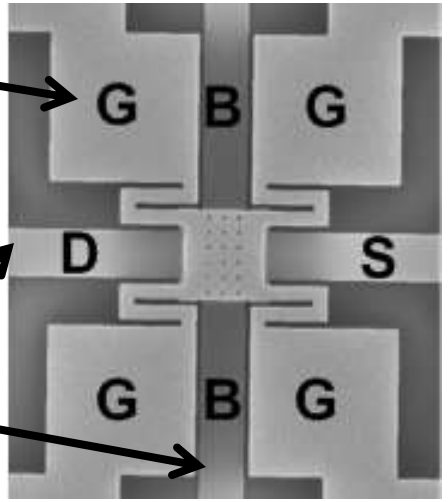
Relay Technology

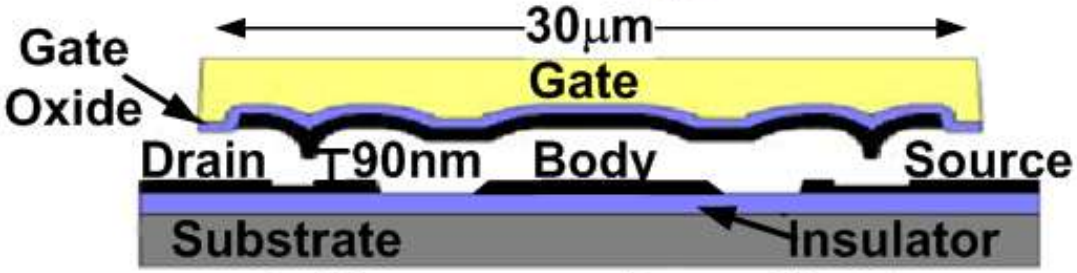
4-Terminal Relay Structure & Operation



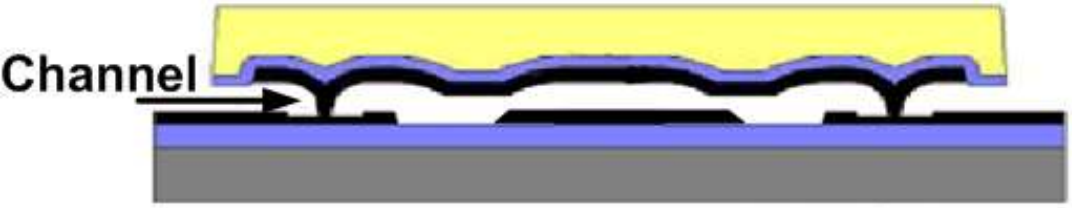
Poly-SiGe

Tungsten





A-A' cross-section: *off*-state



A-A' cross-section: *on*-state

OFF State:

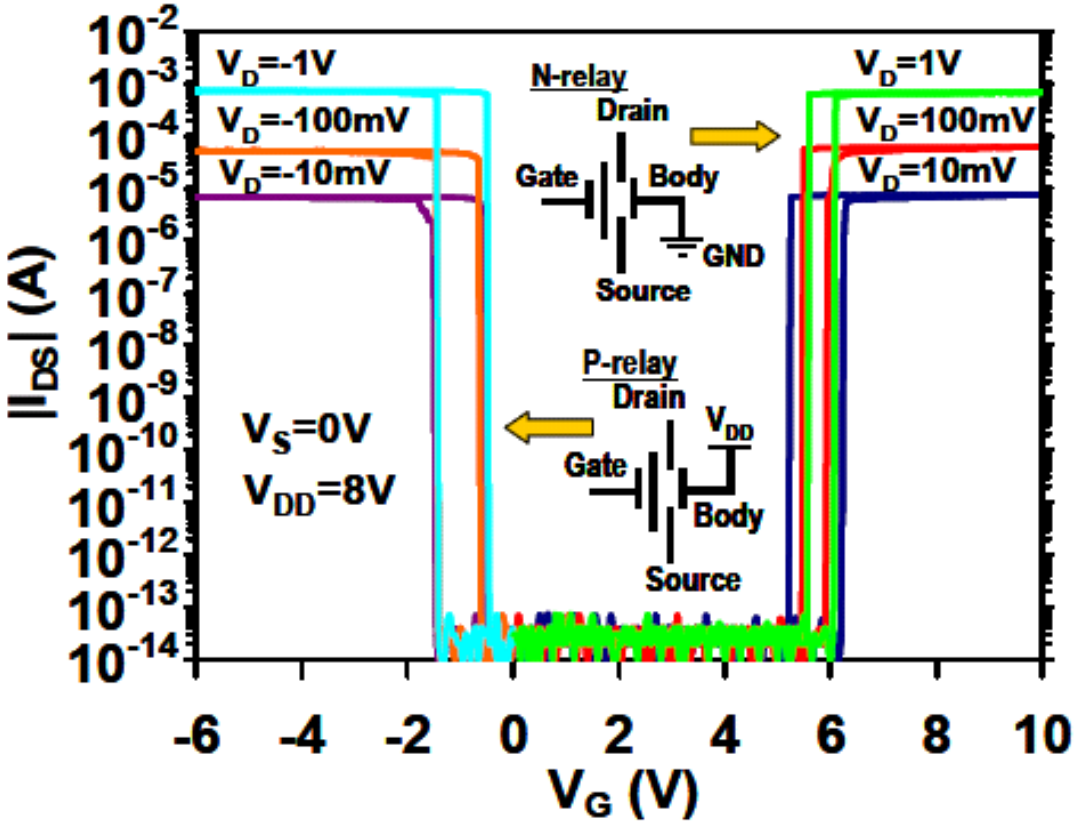
$|V_{gb}| < V_{po}$ (pull-out voltage)

ON State:

$|V_{gb}| > V_{pi}$ (pull-in voltage)

Measured I_D-V_G Characteristics

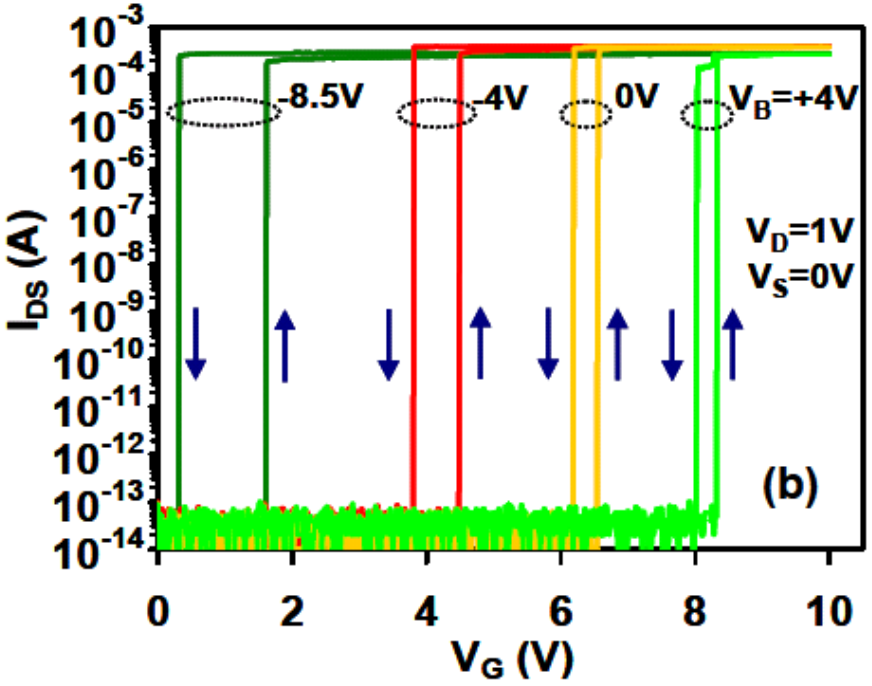
- NMOS or PMOS operation is achieved with appropriate body bias:



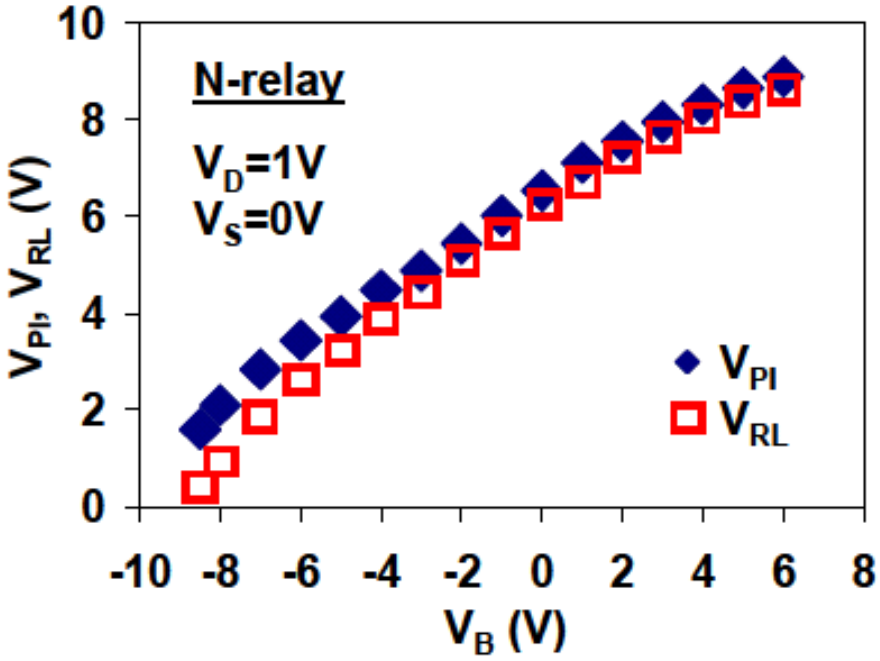
- Zero off-state leakage; S < 0.1mV/dec
- Hysteresis due to pull-in mode operation & surface adhesion force

Impact of Body Biasing

I_D-V_G Characteristics



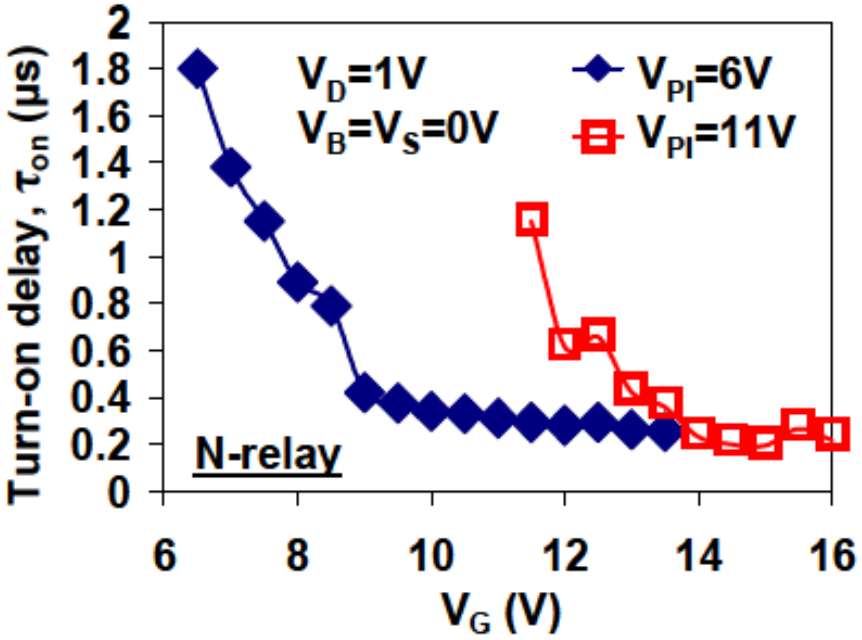
Switching Voltages *vs*. Body Bias



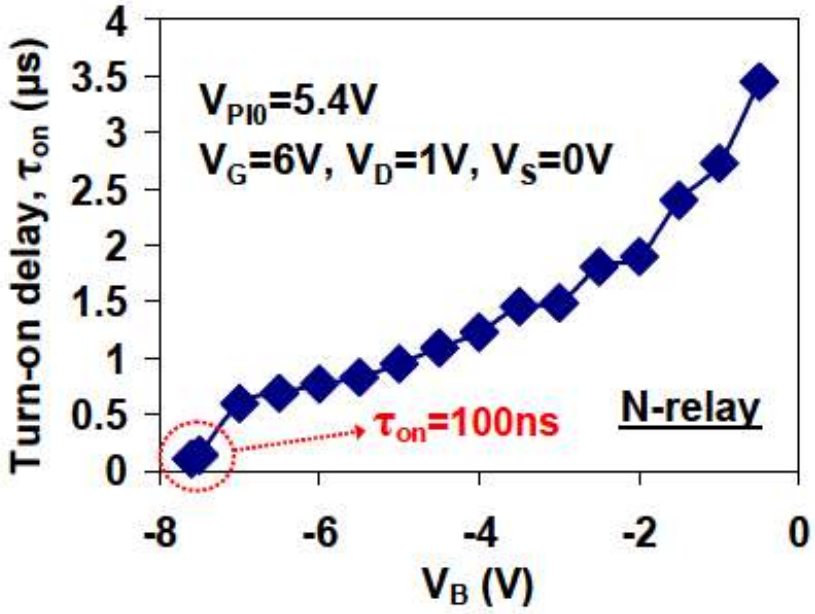
- **Body biasing can be used to reduce the gate voltages for switching.**
- **Increased hysteresis seen for $V_B < 0$ is due to gate-oxide charging (DC voltage stress during measurement).**

Switching Delay

Turn-ON Time *vs.* Gate Voltage



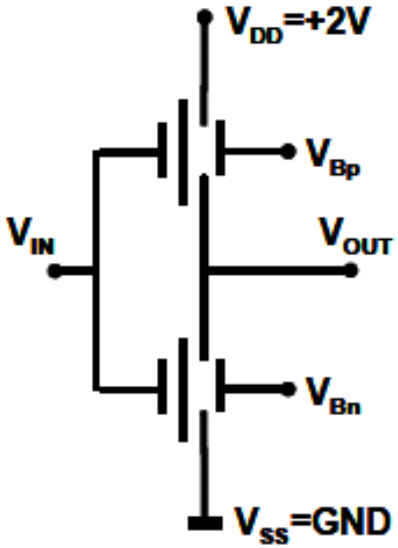
Turn-ON Time *vs.* Body Bias



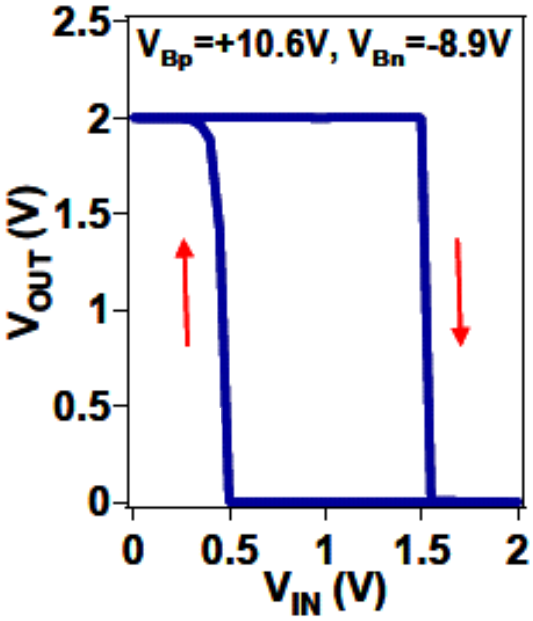
- **Turn-on delay improves with gate overdrive, and saturates at ~200ns for V_B = 0V.**
- **Turn-on delay improves w/ body biasing to reduce V_{PI} → 100ns turn-on delay**

Complementary Relay Inverter

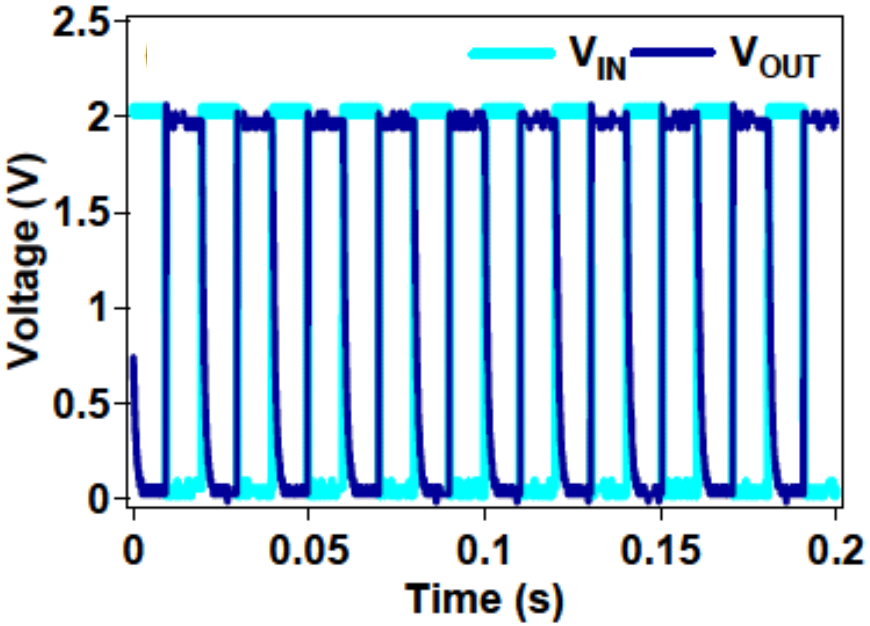
Circuit Diagram



Voltage Transfer Char.



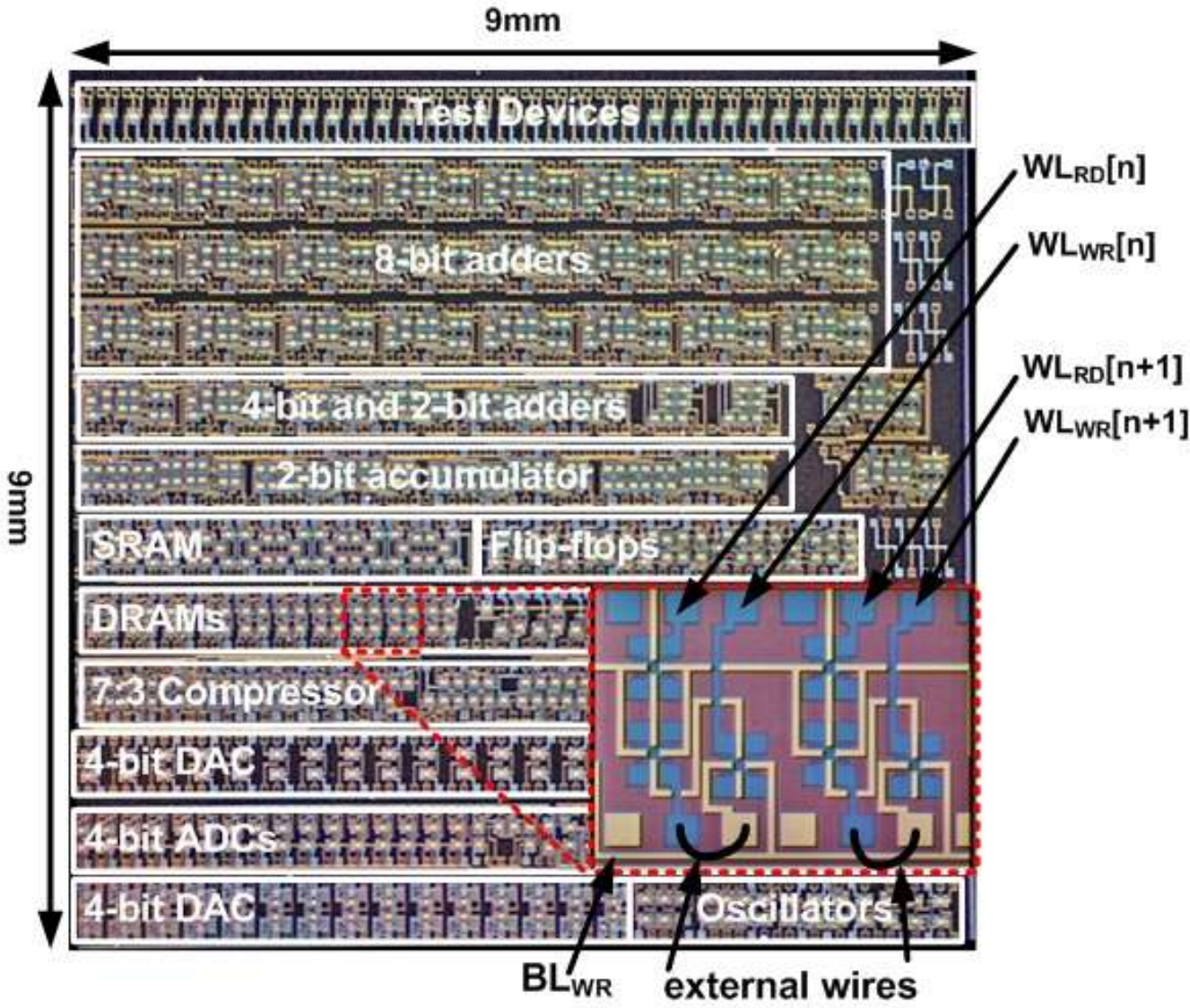
Voltage Waveforms



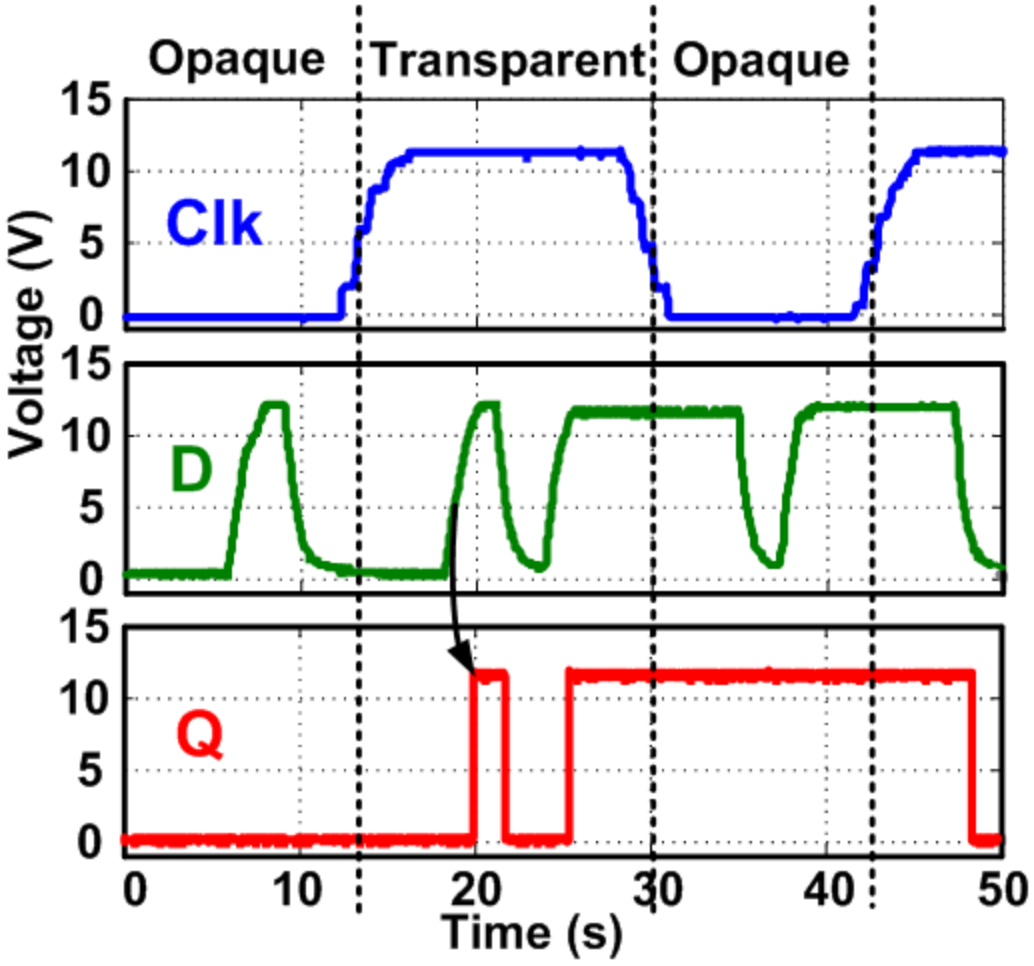
- **Complementary operation is achieved via body biasing**
  - **$V_{PI,n} \geq V_{RL,p}$ & $V_{PI,p} \leq V_{RL,n}$ for abrupt VTC and zero crowbar current.**
- **For maximum noise margin, switching should be symmetric about $V_{DD}/2$ with minimum hysteresis.**

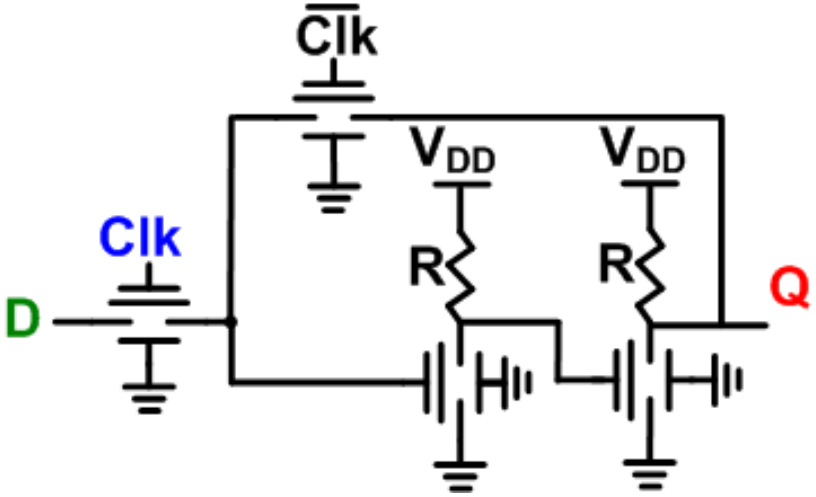
Demonstration Test Chip

- Test devices
- Adders
- Flip-flops/Latches
- 7:3 Compressor
- SRAM, DRAM
- DAC
- ADC
- Oscillators



Relay Latch Circuit

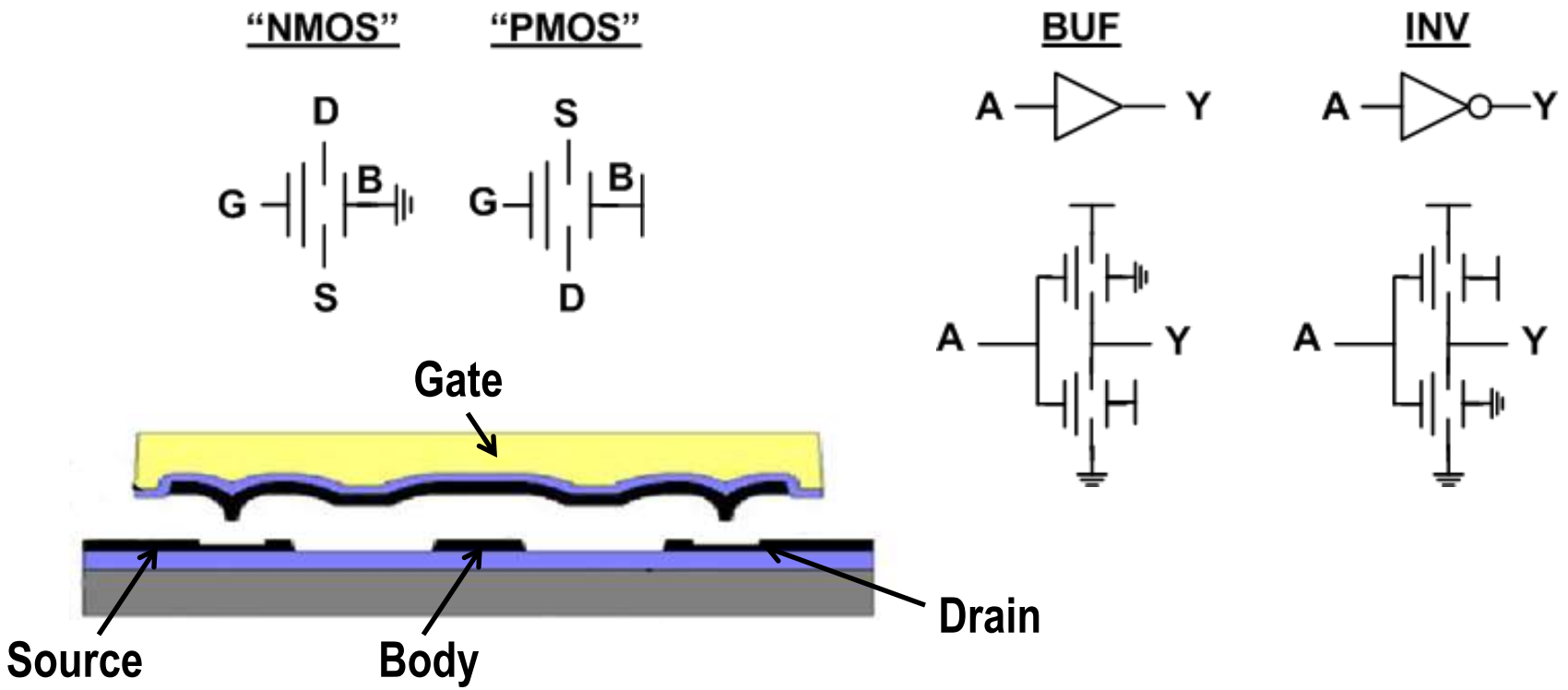




- **Designed as for MOSFETS, but this not always optimal…**

Relay-Based IC Design

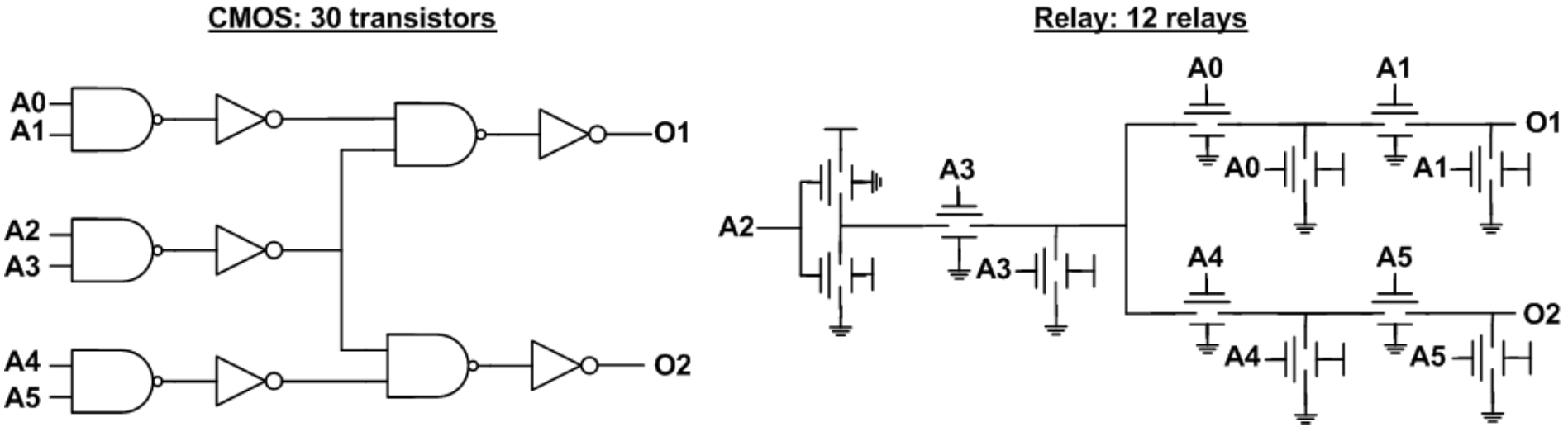
The 4-T Relay as a Logic Element



- **4-terminal design mimics MOSFET operation**
  - **Actuation is independent of source/drain voltages**
- **Electrostatic actuation is ambipolar**

  → **Non-inverting logic is possible**

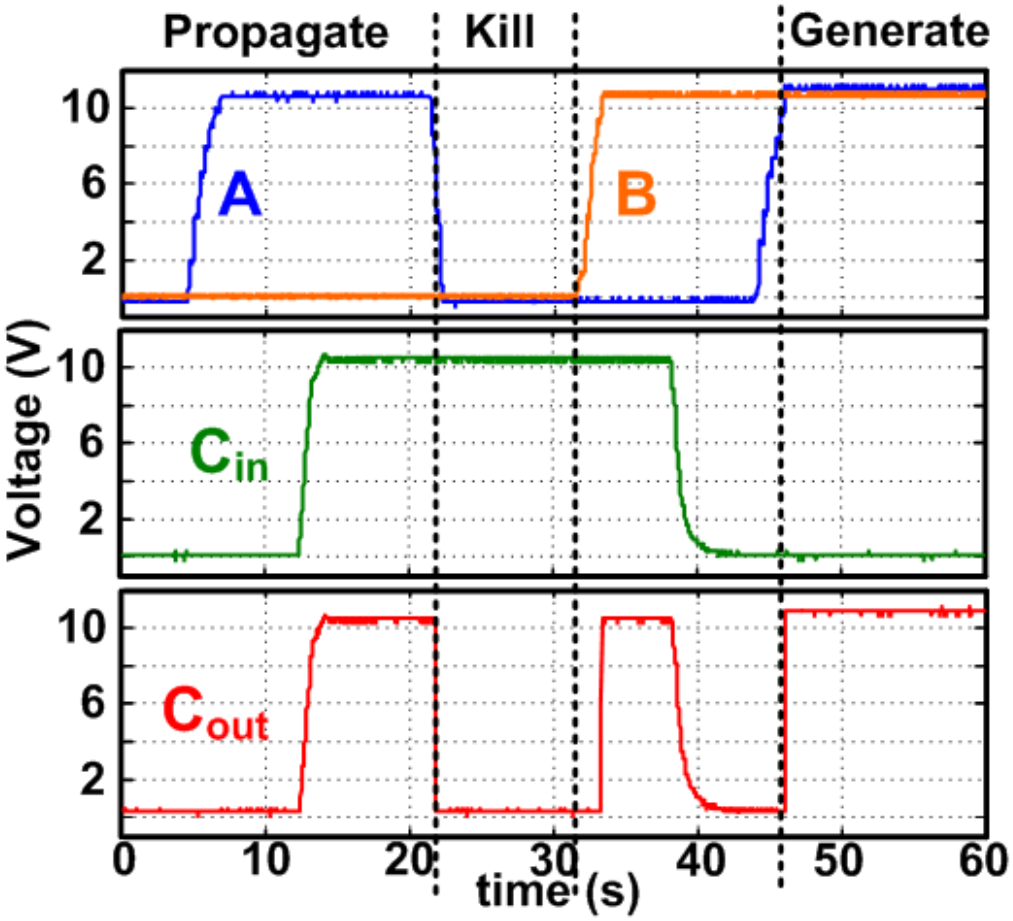
Digital Circuit Design with Relays

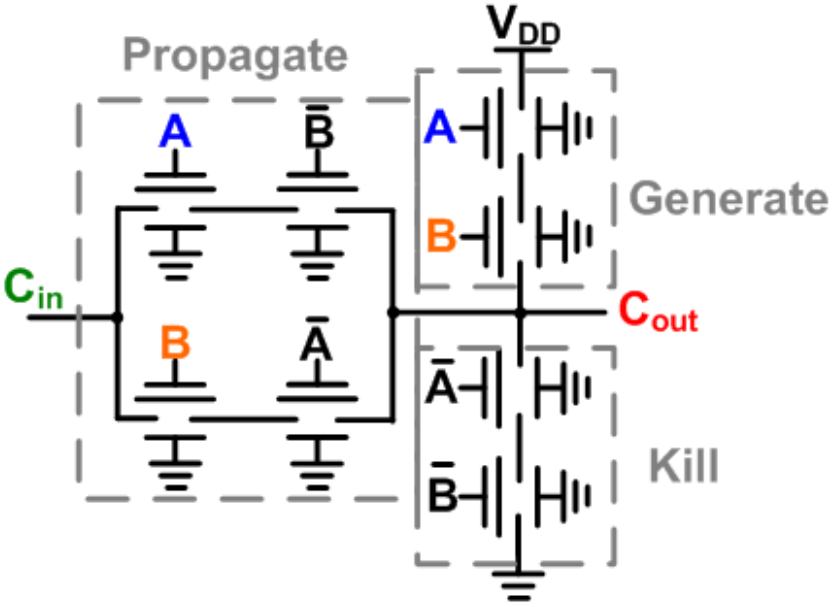


- **CMOS: delay set by electrical time constant**
  - **Quadratic delay penalty for stacking devices**
  - **Buffer & distribute logical/electrical effort over many stages**
- **Relays: delay dominated by mechanical movement**
  - **Can stack ~100-200 devices before $t_{d,elec} \approx t_{d,mech}$**
  - **So, want all relays to switch simultaneously**

→ Implement relay logic as a single complex gate

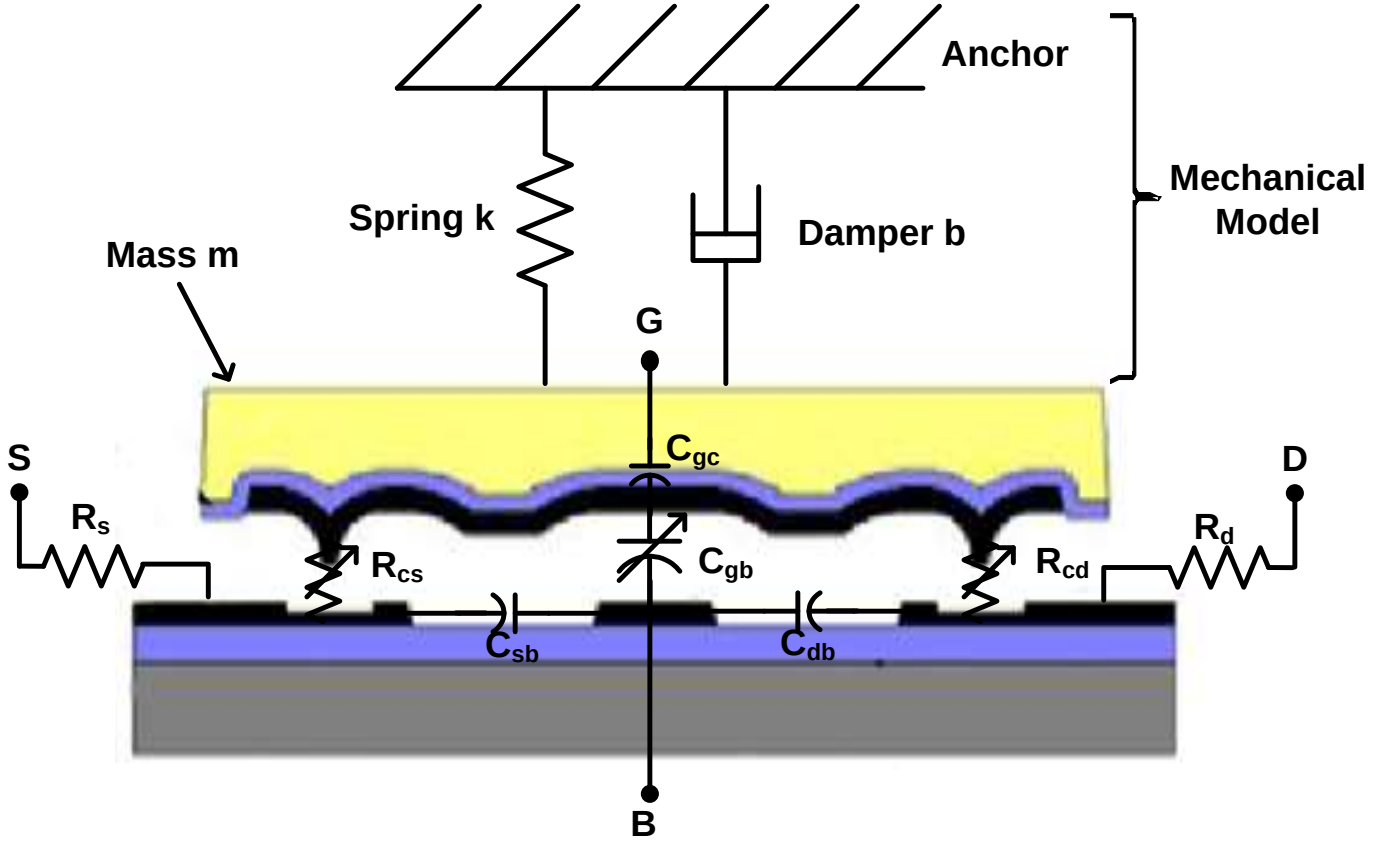
Relay Carry Generation Circuit





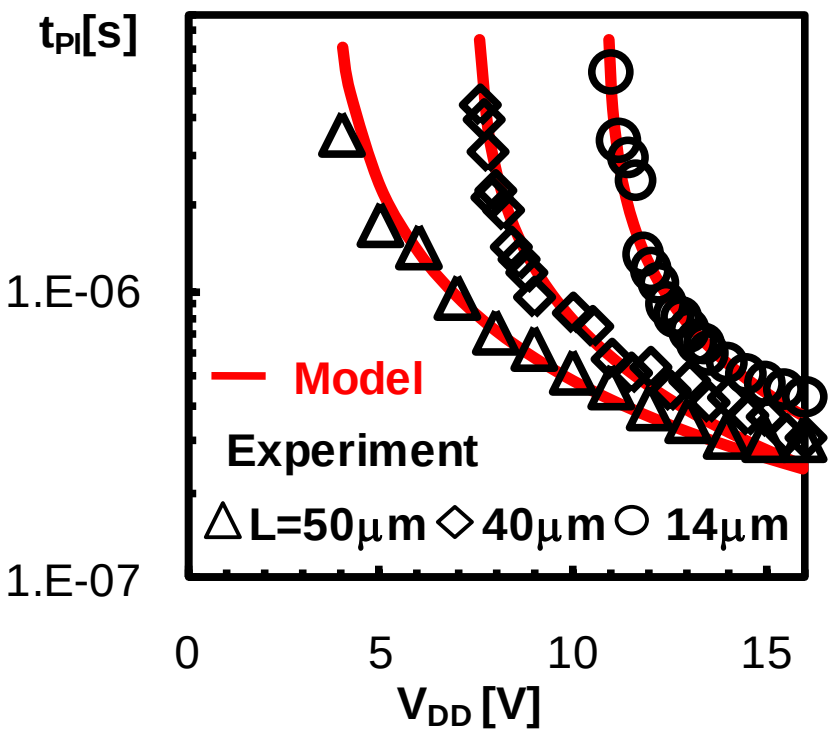
- **Demonstrates propagate-generate-kill logic as a single complex gate**

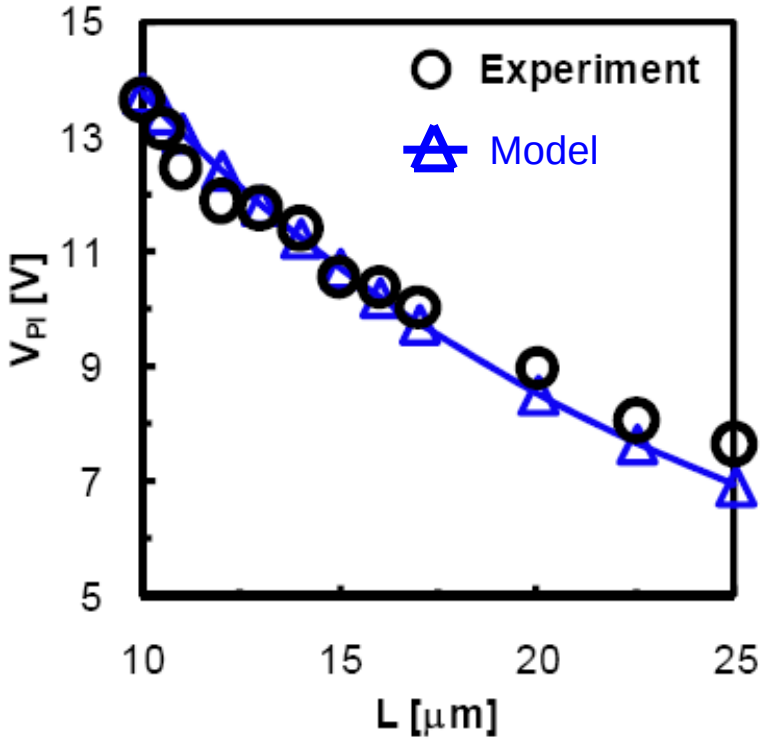
4-T Relay Compact Model



- **Lumped Verilog-A model for circuit sims:**
  - **Mechanical dynamics: spring (k), damper (b), mass (m)**
  - **Electrical parasitics: non-linear gate-body (C_{gb}), gate-channel (C_{gc}), and source/drain-body cap ($C_{s,db}$), contact resistance ($R_{cs,d}$)**

Model Calibration

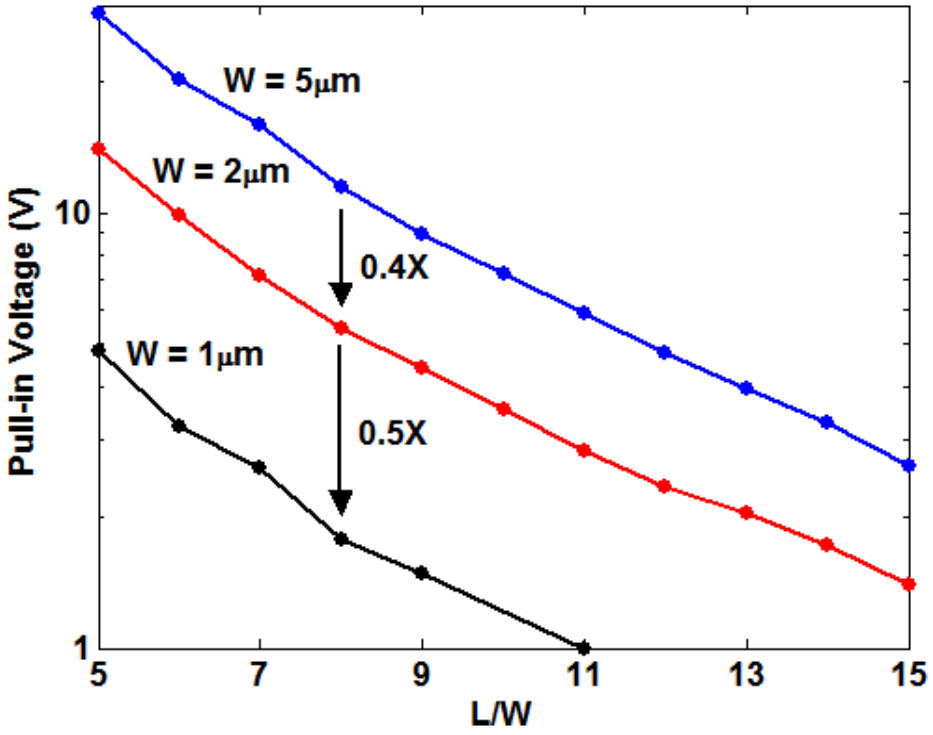




- **Lumped model matches measurements**
- **Use calibrated models for circuit design**

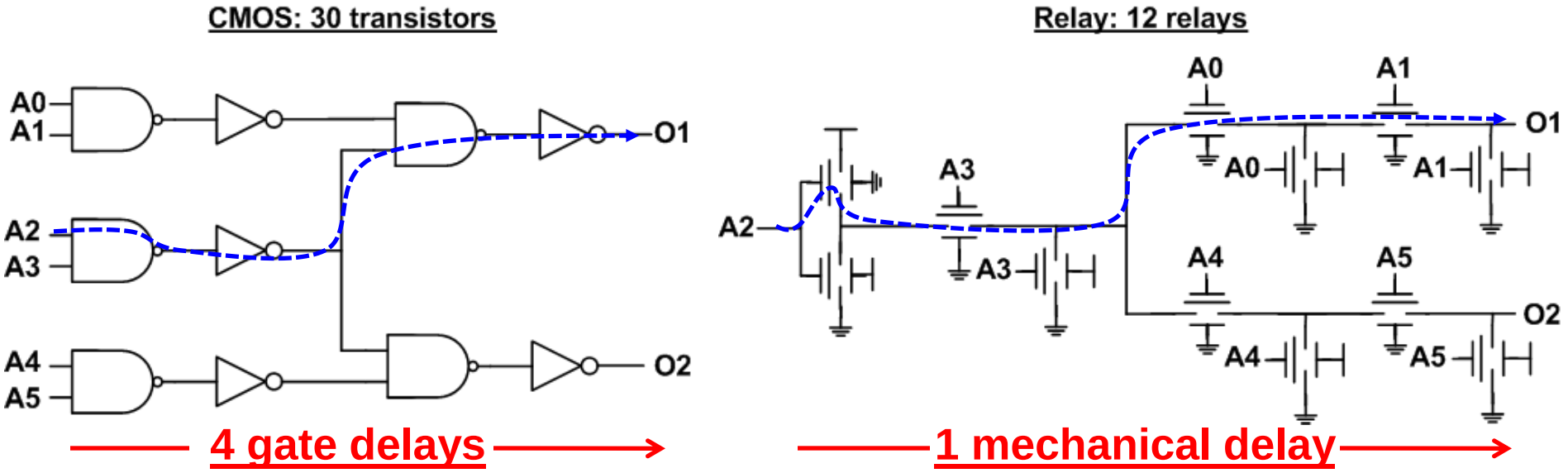
Relay Scaling

- **Constant E-field: mechanical delay and V_{PI} scale linearly**
  - **Assuming surface forces scale**



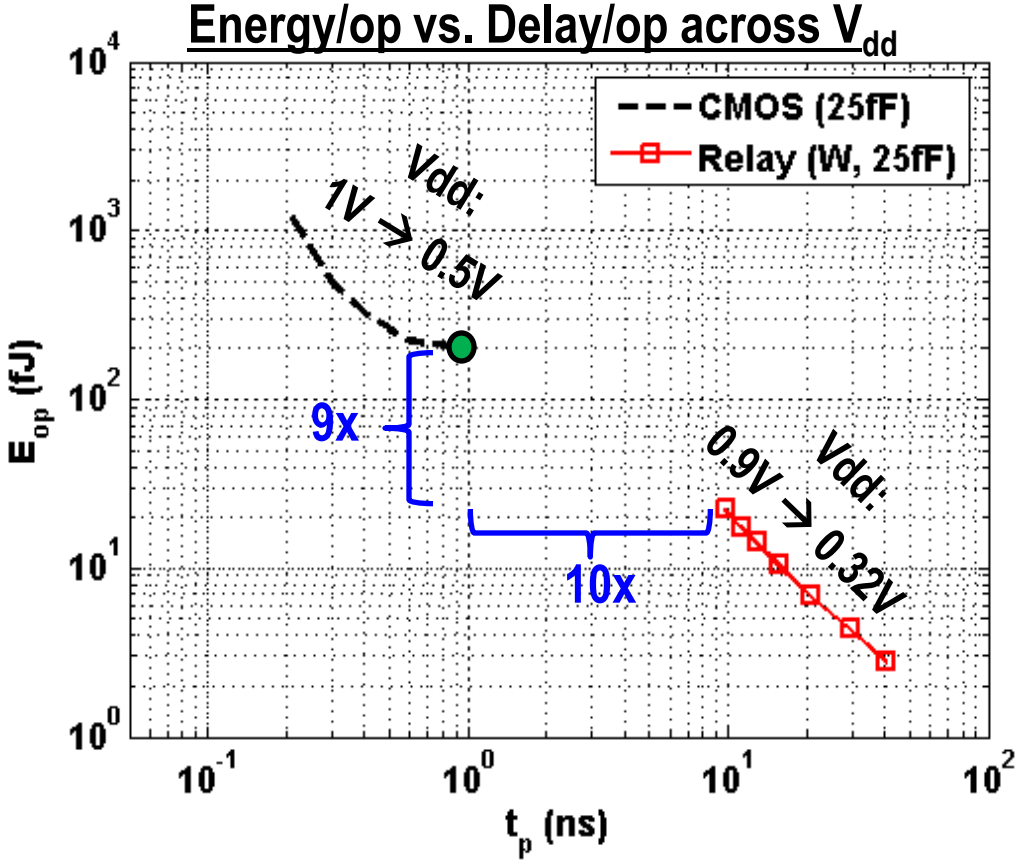
- **For a 90nm device: V_{PI} ~200mV, t_{PI} ~10ns @ V_{dd} = 1V**
  (cantilever beam with W = 90nm, H = 90nm, t_{gap} = 10nm, L = 2.3um)

Benchmarking Relays *vs.* CMOS



- **Delay Comparison *vs*. CMOS**
  - Single mechanical delay *vs*. several electrical gate delays
  - For reasonable load, relay delay unaffected by fan-out/fan-in
- **Area Comparison *vs*. CMOS**
  - Larger individual devices
  - Fewer devices needed to implement the same logic function

Energy-Delay Comparison

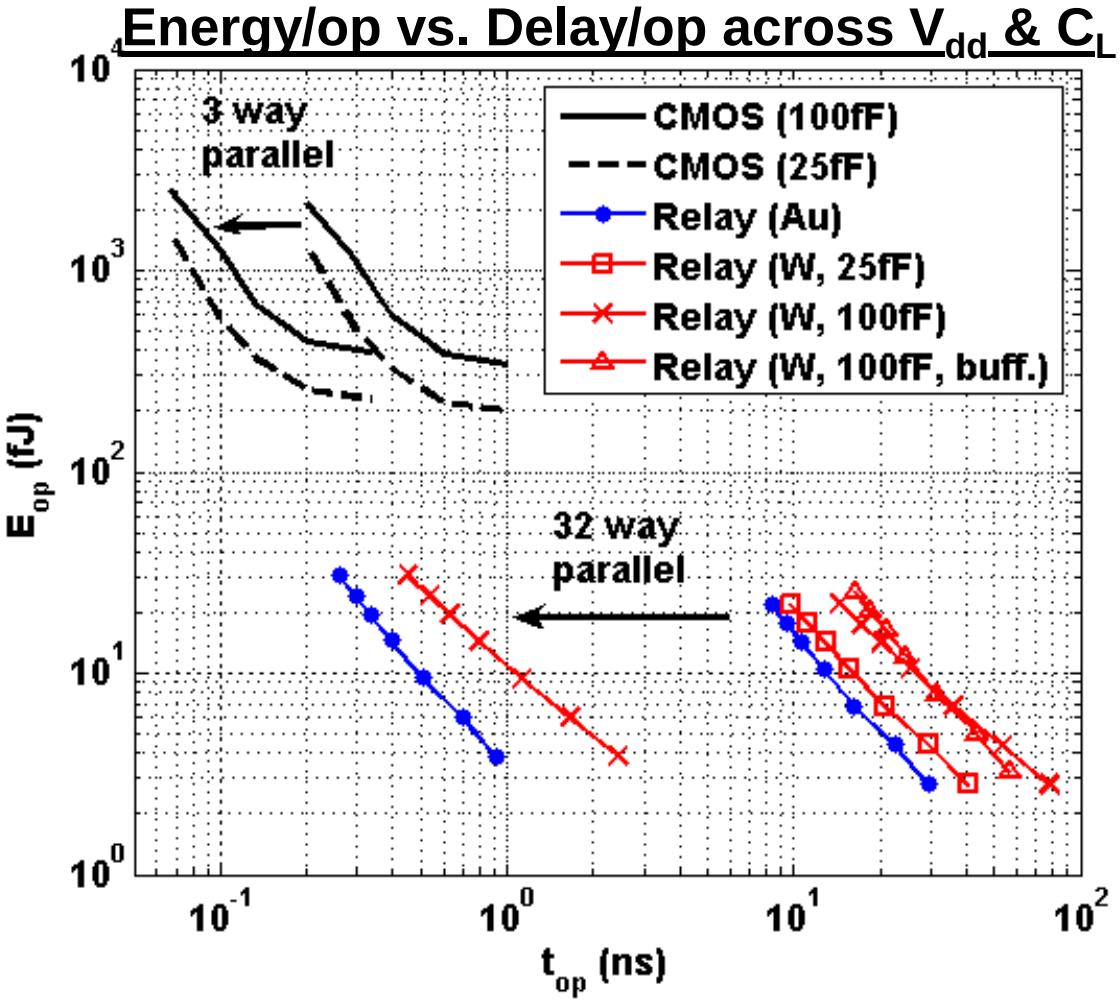


- Compare *vs.* Sklansky CMOS adder[1]
- 30x less capacitance
  - Lower device C_g, C_d
  - Fewer devices
- 2.4x lower V_{dd}
  - No leakage energy

- For similar area: >9x lower E/op, >10x greater delay

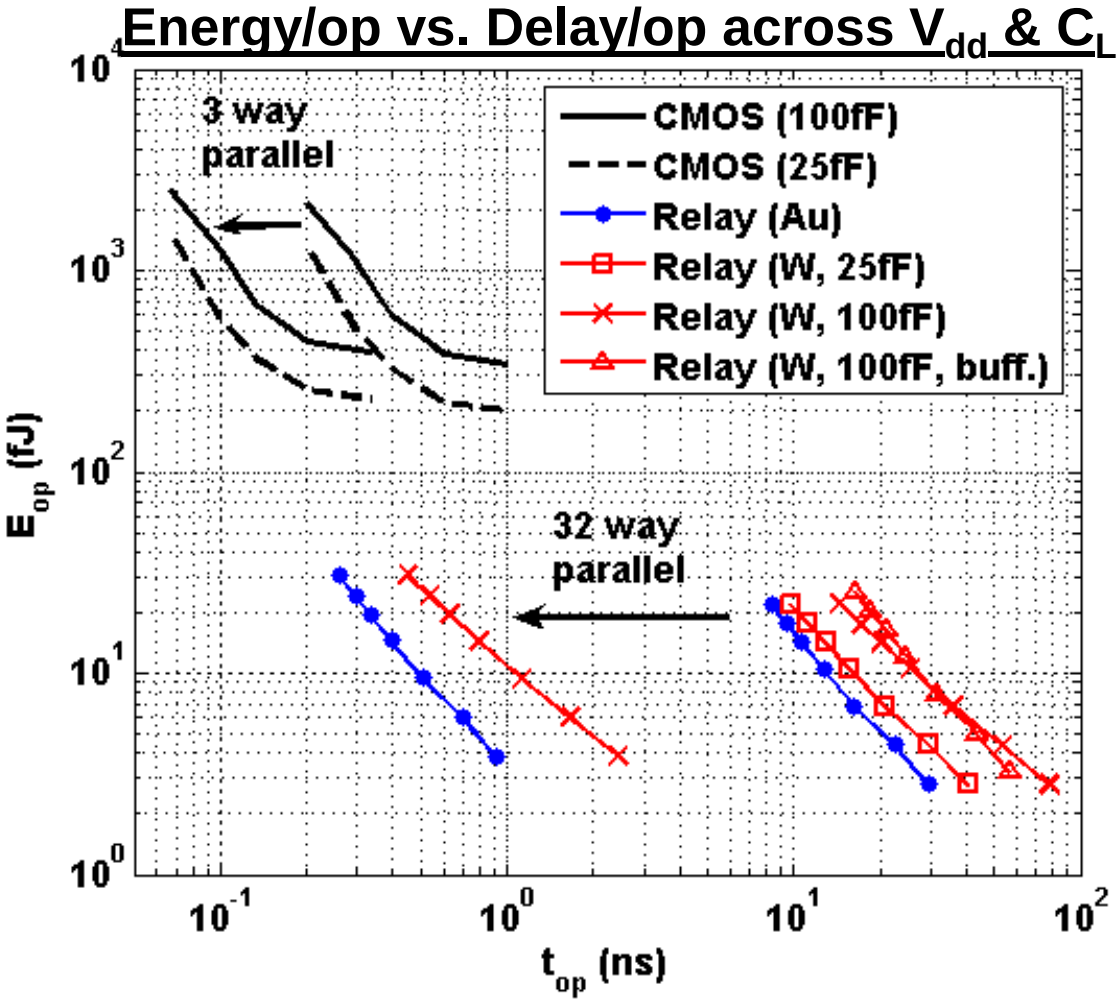
[1]D. Patil et. al., "Robust Energy-Efficient Adder Topologies," in Proc. 18th IEEE Symp. on Computer Arithmetic (ARITH'07).

Benefit of Parallelism



- **Can extend energy benefit up to GOP/s throughput**
  - **As long as parallelism is available**

Effect of Contact Resistance

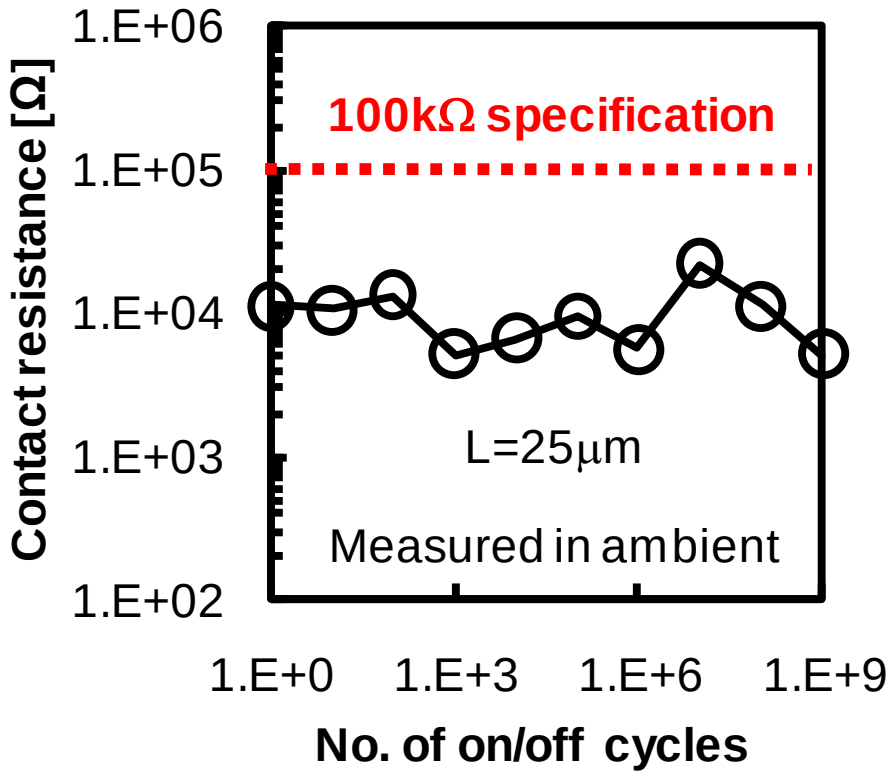


- **Low contact R not critical**
  - **Enables low force, hard contact material**

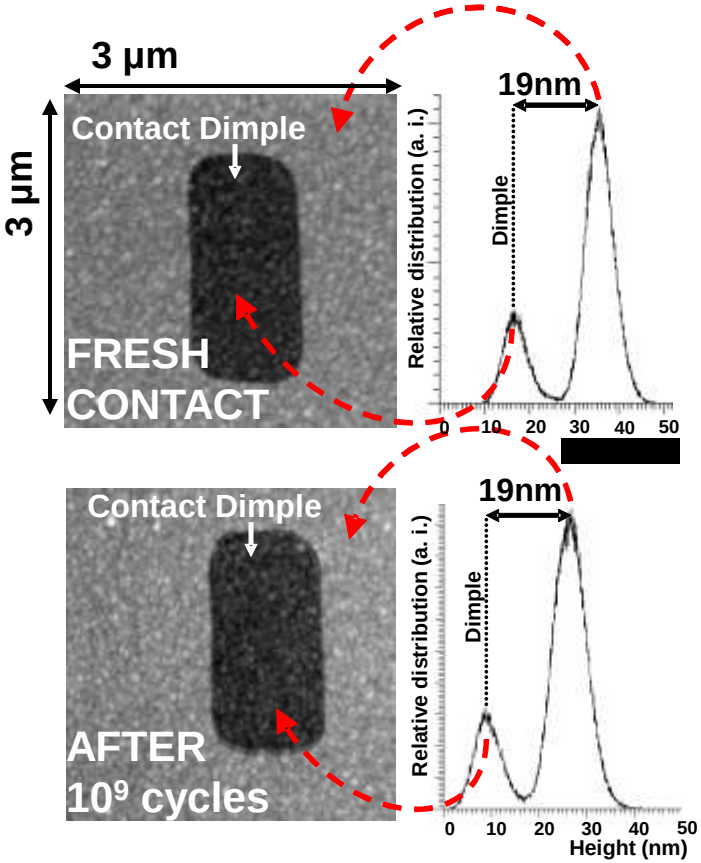
→ Good news for reliability

Contact Endurance

ON-state Resistance *vs*. # ON/OFF Cycles



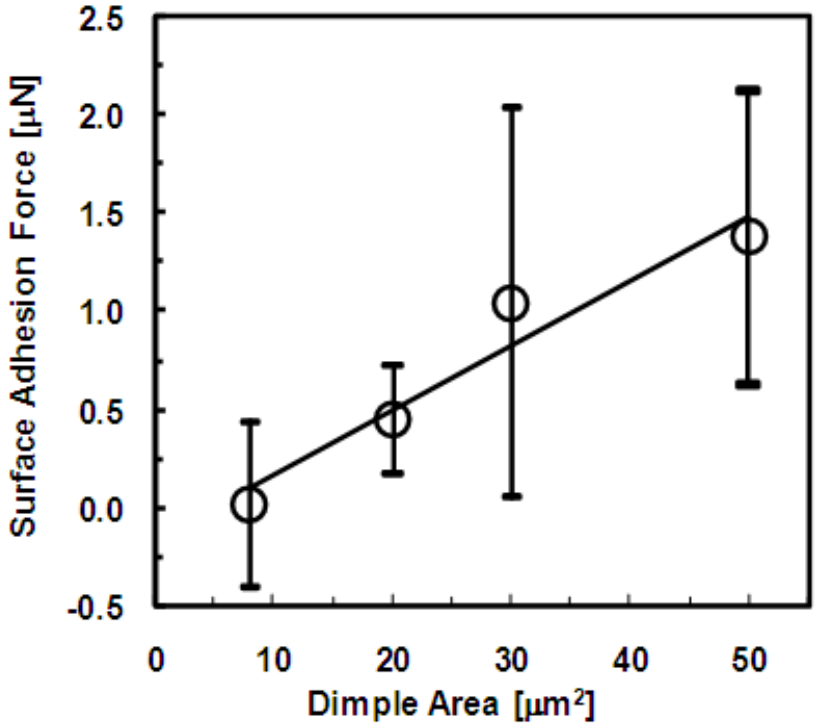
AFM Measurements



- **Variations are likely due to *W* oxidation**
- **No surface wear is seen after 1 billion ON/OFF cycles**

Relay Energy Limit

- Spring restoring force must be able to overcome surface adhesion force F_A.
- For large contacts, F_A scales with area:



- Extracted surface adhesion energy ≈ 5 μJ/m²
- Ultimate relay energy limit set by required R_{on}

Summary

Summary

- **Due to transistor off-state leakage, CMOS technology has a fundamental limit in energy efficiency.**
- **Mechanical switches have zero leakage and thus may achieve substantially lower energy/operation.**
  - **Much progress has been made toward a high-yield, reliable micro-relay technology suitable for IC applications.**
- **New circuit and system architectures are needed to fully realize the benefits of relay technology.**
  - **Potential CMOS replacement for low-throughput/parallel applications**

Acknowledgements

Collaborators:

- **Vincent Pott, Hei Kam, Rhesa Nathanael, Jaeseok Jeon**
- **Fred Chen (MIT), Matthew Spencer, Hossein Fariborzi (MIT), Chengcheng Wang (UCLA)**

Funding:

- **DARPA/MTO NEMS Program**
- **DARPA/MARCO Focus Center Research Program**
  - **Center for Materials, Structures, and Devices (MSD)**
  - **Center for Circuits and Systems Solutions (C2S2)**

- **UC Berkeley Microfabrication Laboratory**
- **Berkeley Wireless Research Center**