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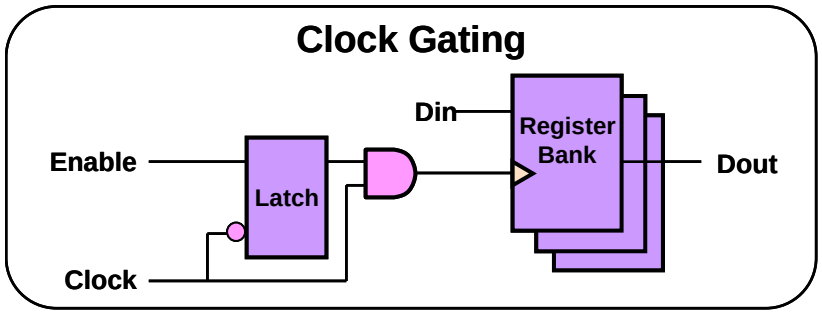
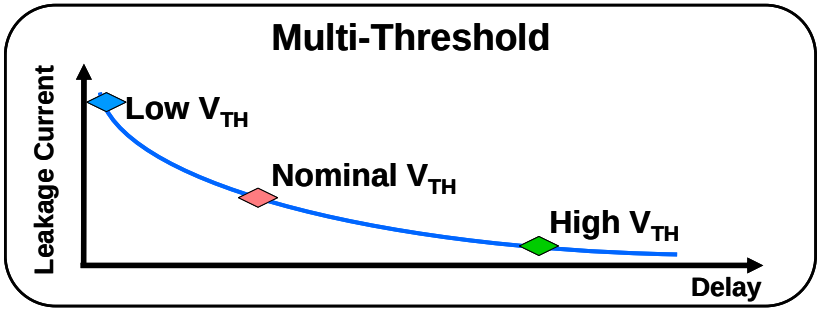
Low Power
&
Impact On Verification

Prapanna Tiwari

Low Power Techniques

- **Traditional Techniques**





- **Advanced Techniques**

Voltage Control Is Key

Design Techniques Impact Verification

MTCMOS power gating (shut down)

Power gating with State Retention

Low-VDD Standby

Dynamic or Adaptive Voltage Frequency Scaling (DVS, DVFS, AVS, AVFS)

Multi-Voltage (MV)

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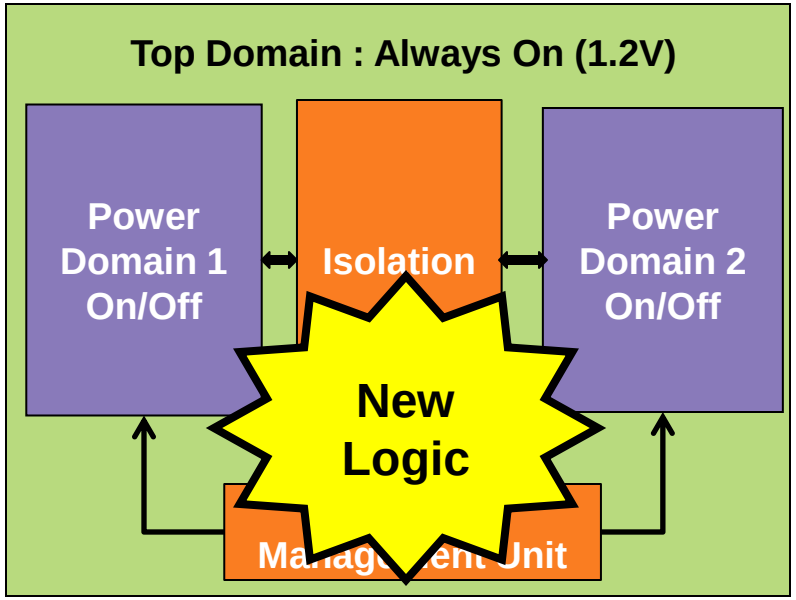
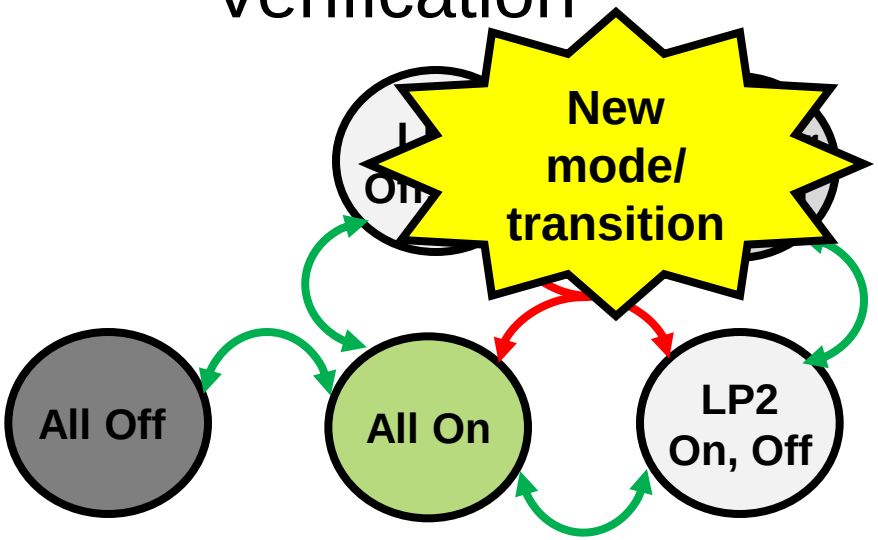
Verification Impact

Design



Verification



Allowed transitions

Disallowed transitions

New logic and semantic to be checked and simulated without being present in RTL!!!

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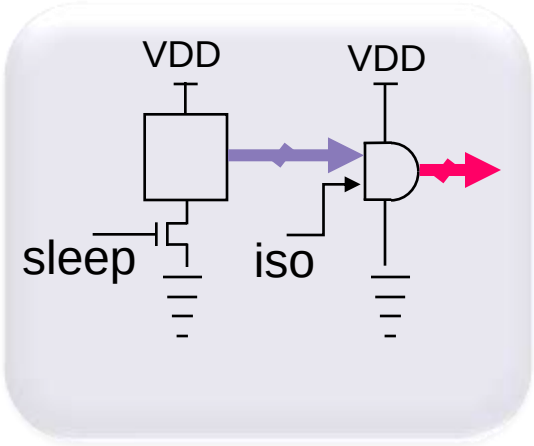
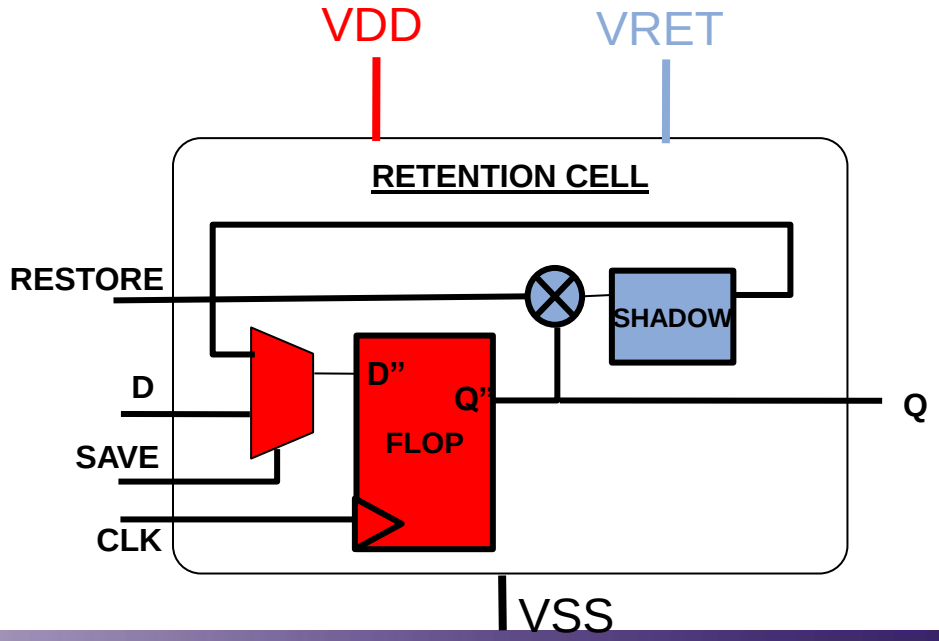
Low Power Introduces New Logic

- Power management introduces logic for **Isolation, Retention and Level-shifter** (defined in UPF)
  - This is behavioral code that doesn't exist in RTL
  - It must account for secondary effects in addition to the primary role.
  - E.g. Isolation is dependent on iso-enable and it's driving rail
  - E.g. Retention is dependent on save/restore/ret-rail/assert-values/voltage-ramp time



ISOLATION



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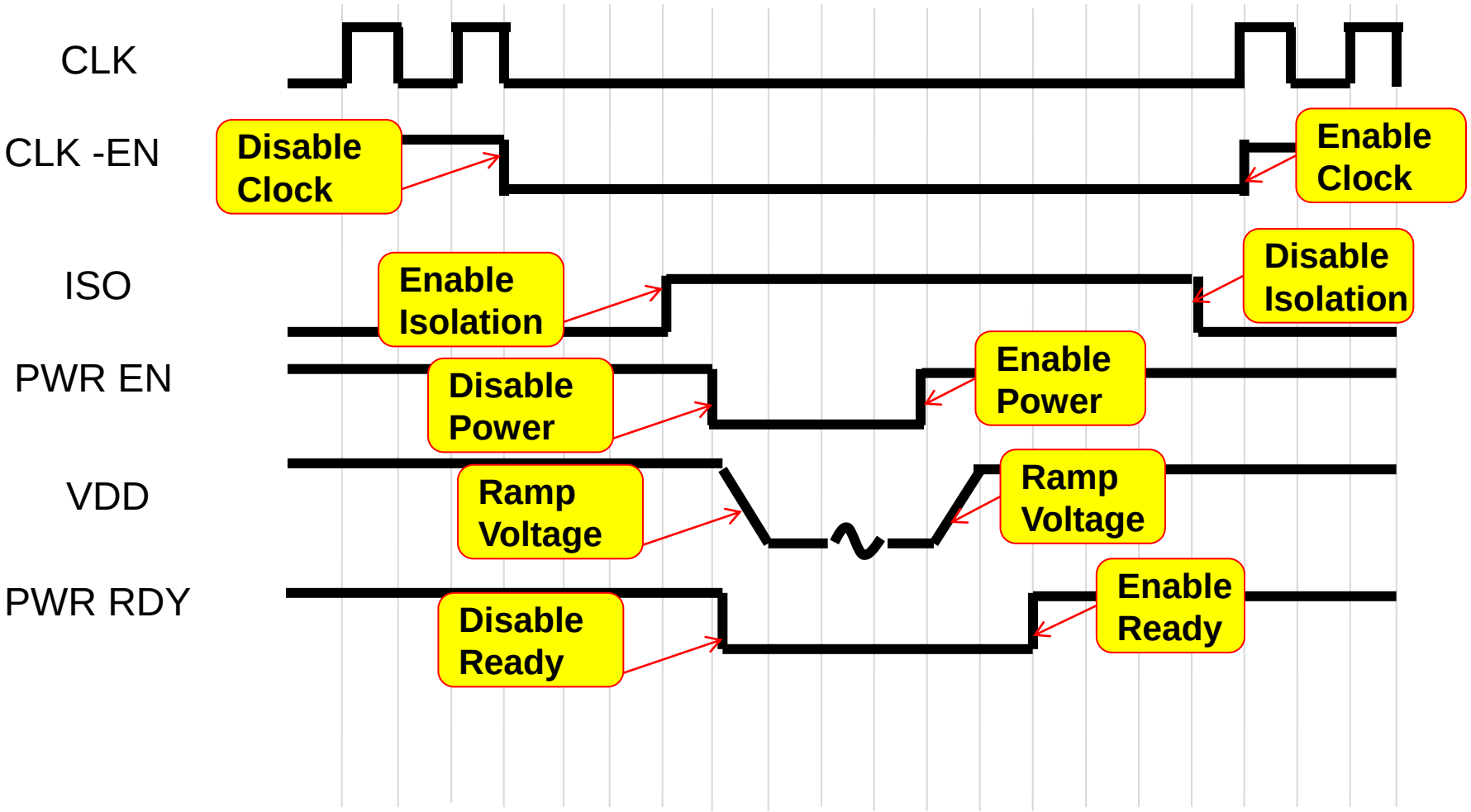
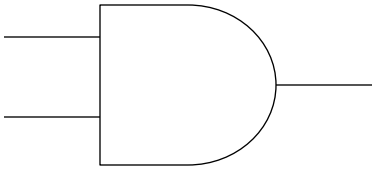
Low Power Introduces New Events/Protocol

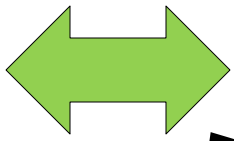


Accuracy Of Simulation

A key concern for LP verification

- Non-LP behavior of logic is defined in HDL (verilog, VHDL, SV) manuals
  - You do not loose sleep over whether simulator is simulating the AND gate accurately!!
- HDL LRM only defines association between logic pins
  - Does NOT consider voltage effects





and	0	1	x	z
0	0	0	0	0
1	0	1	x	x
x	x	x	x	x
z	x	x	x	x

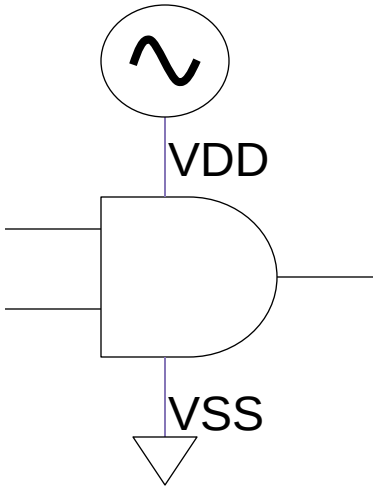
No Voltage Field

Snippet from IEEE Std 1364-1995 (Verilog-1995)

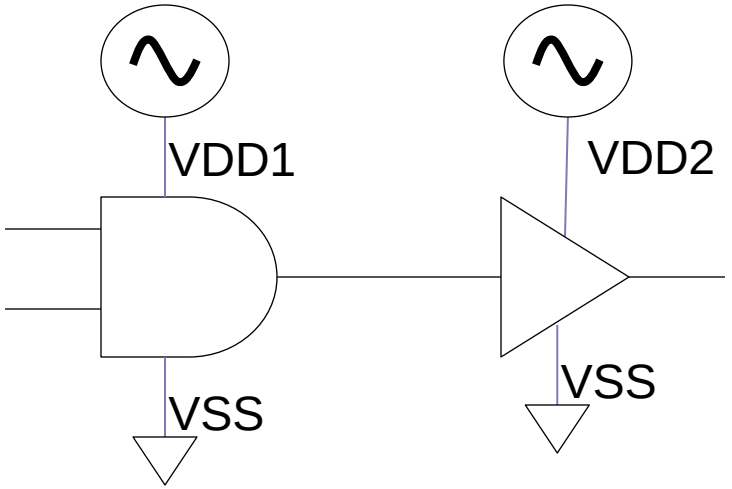
Accuracy Of Simulation

A key concern for LP verification

- Voltage variation NOT part of LRM
- Accuracy of LP simulations is now a concern



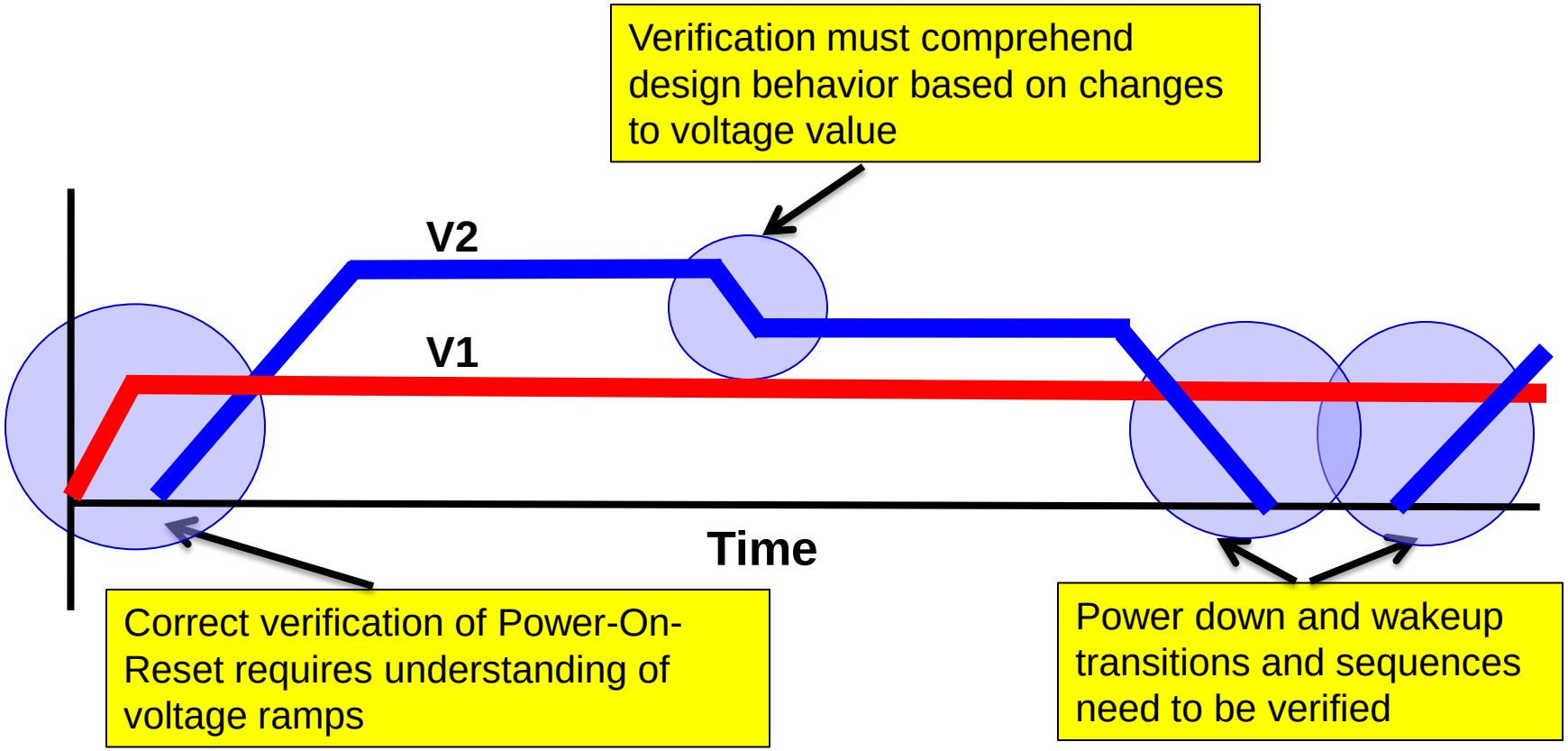
Voltage variation effects output of logic



Voltage comparison across two logic elements effects logic transfer

Power Management Verification –

Accurate Interpretation of Voltages



Verification must be aware of the waveform nature of voltage

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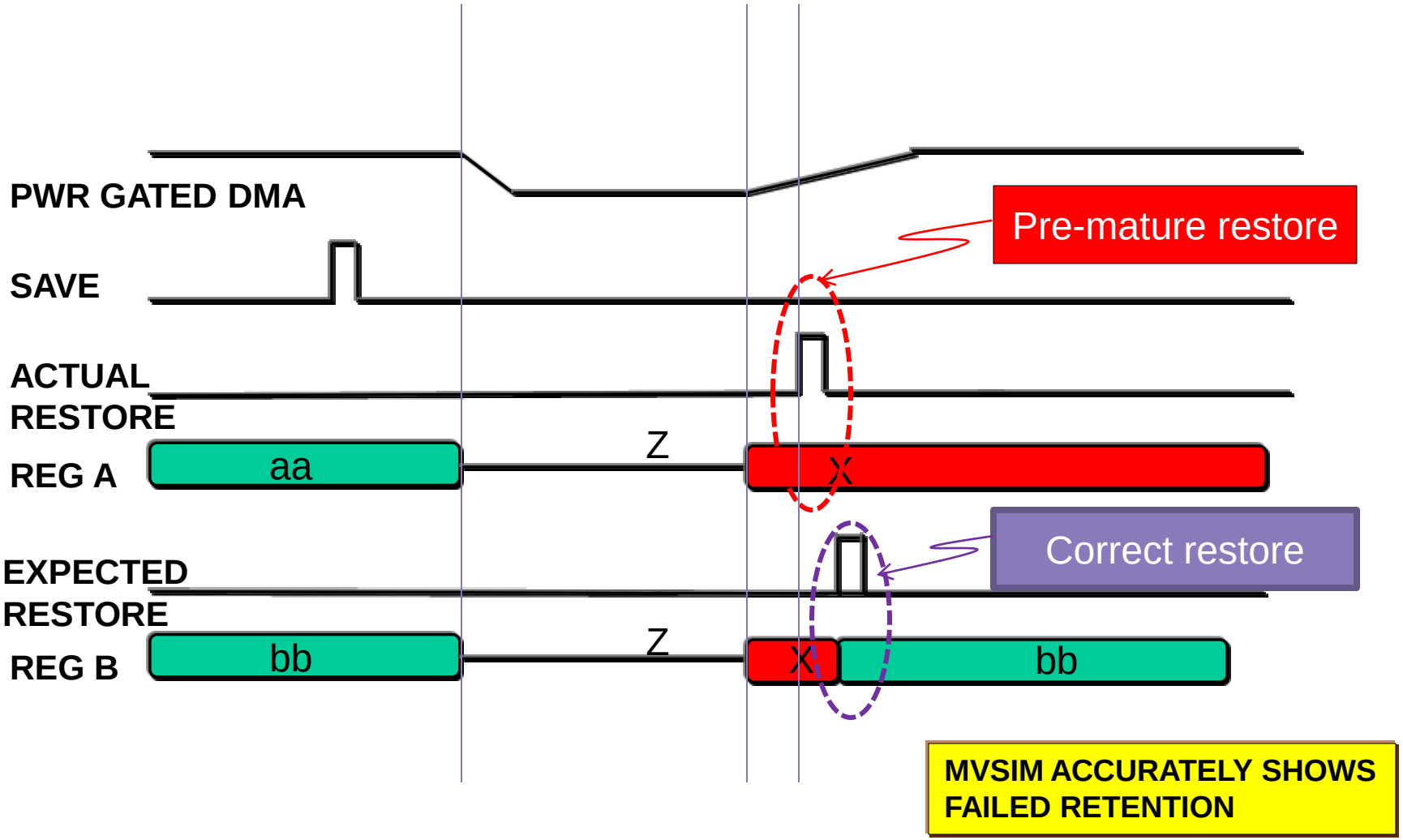
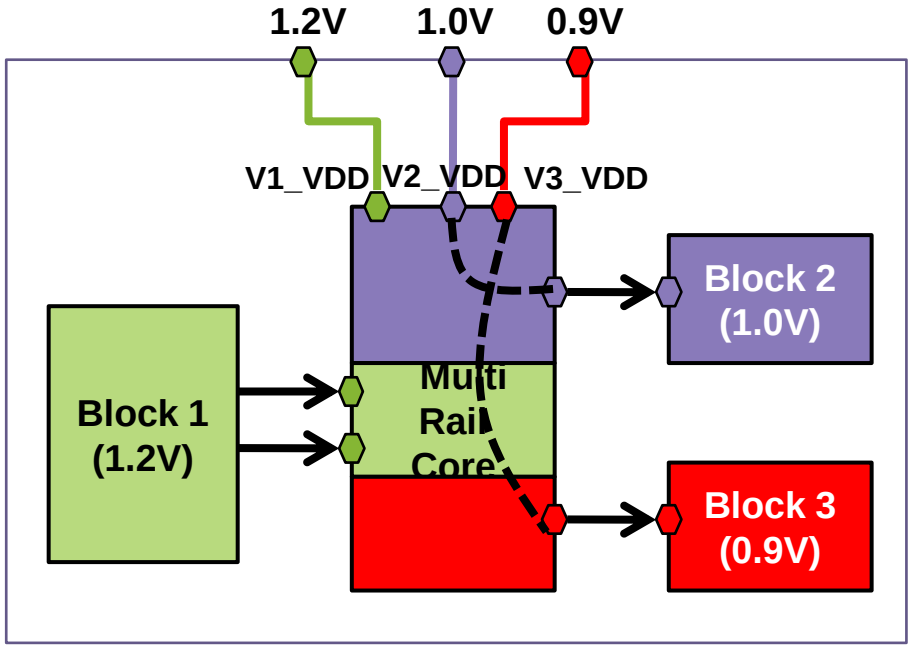
Voltage Ramps Catch Corner Cases



To Make Matters Worse
Multi-Rail Cores

Design

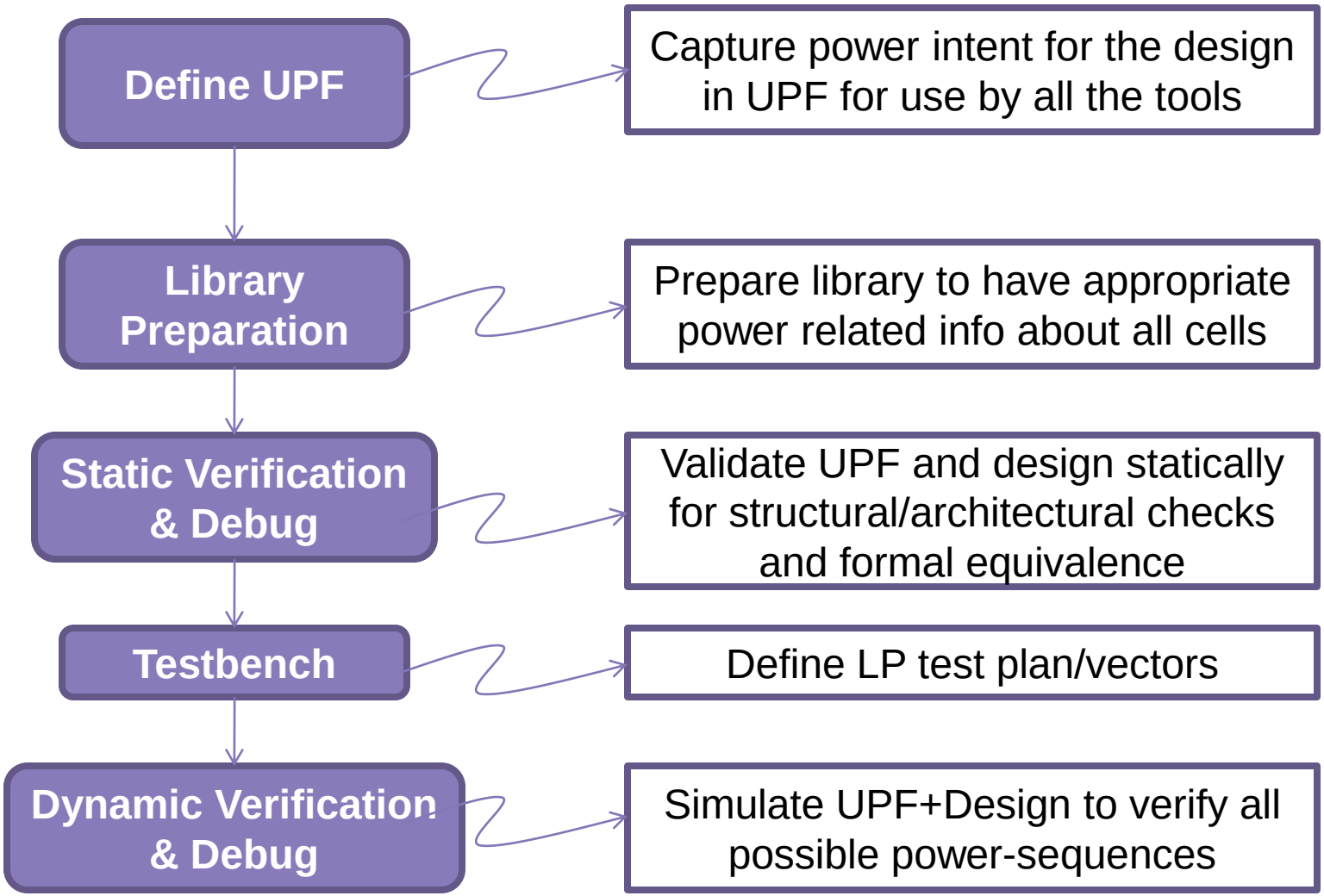


Verification

- Multi-rail cores are connected to different supply voltages
- Logic pins connect to other domains at different voltages

Verification must associate logic pins and internal power partitions to with supply rails

Stages In Verification



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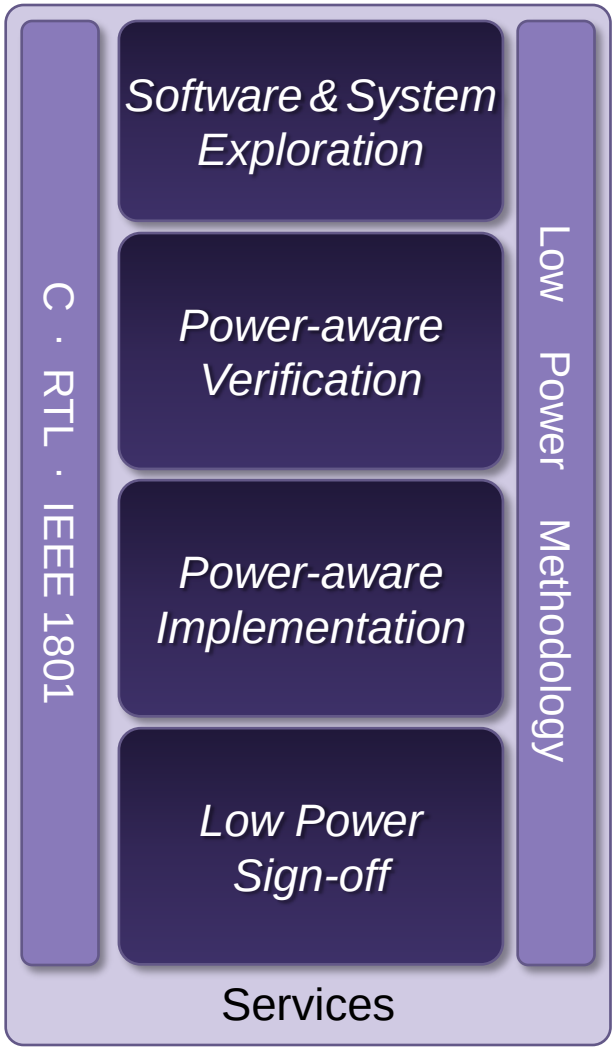
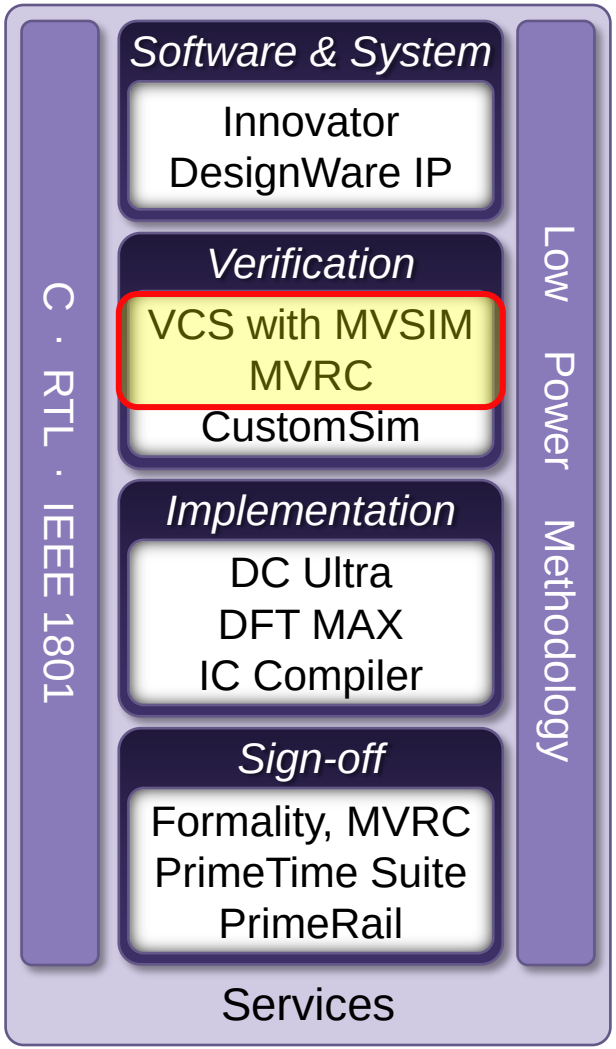
Eclypse Low Power Solution





Summary

- A combination of static and dynamic checks is required for complete low-power verification
- Accuracy is a key concern for low-power verification
  - Verification engineers MUST focus on accuracy when defining a solution
- A complete & scalable low-power verification methodology is necessary to ensure success

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