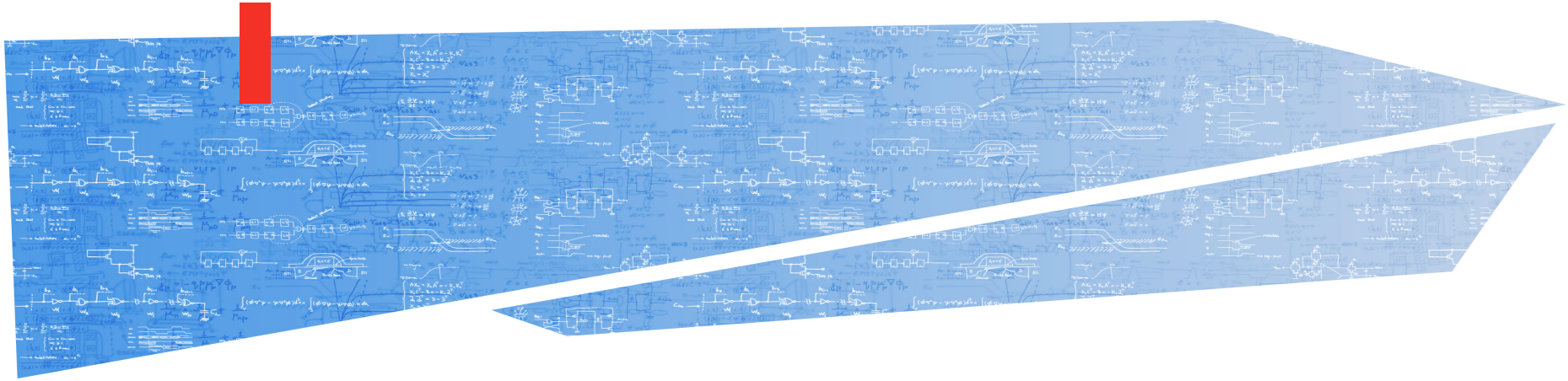

EDA = Electronic Design Automation
Are you kidding?

EDP 2010

Andreas Kuehlmann

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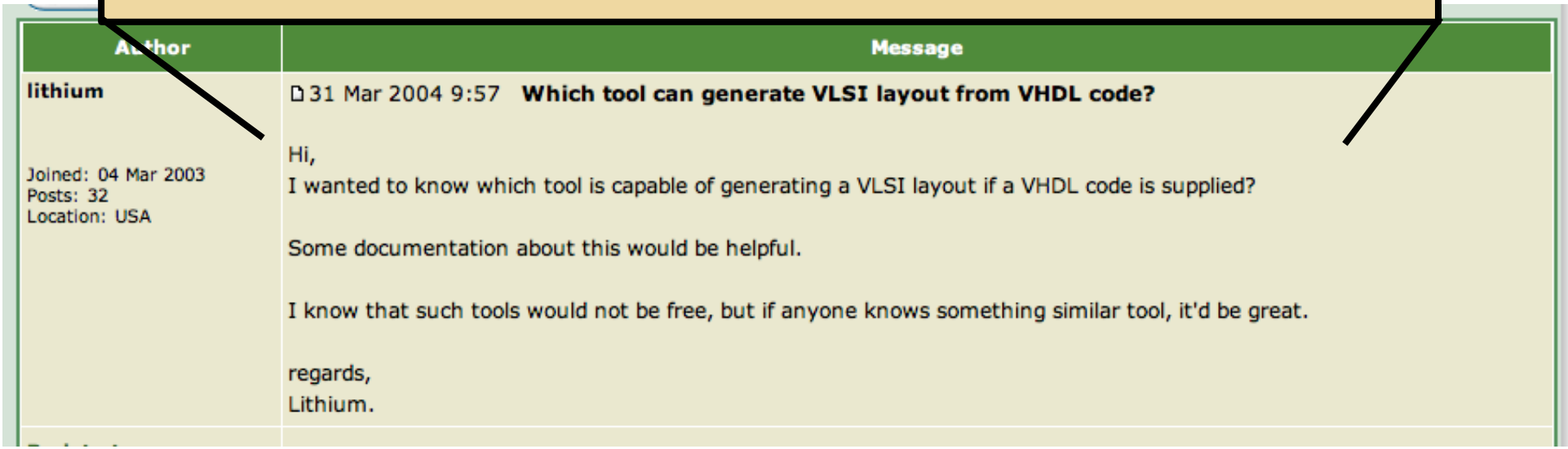
EDA is now more than 30 years old….

Hi, I wanted to know which tool is capable of generating a VLSI layout if a VHDL code is supplied?

…
Some documentation about this would be helpful.
…



Author	Message
lithium Joined: 04 Mar 2003 Posts: 32 Location: USA	31 Mar 2004 9:57 **Which tool can generate VLSI layout from VHDL code?** Hi, I wanted to know which tool is capable of generating a VLSI layout if a VHDL code is supplied? Some documentation about this would be helpful. I know that such tools would not be free, but if anyone knows something similar tool, it'd be great. regards, Lithium.

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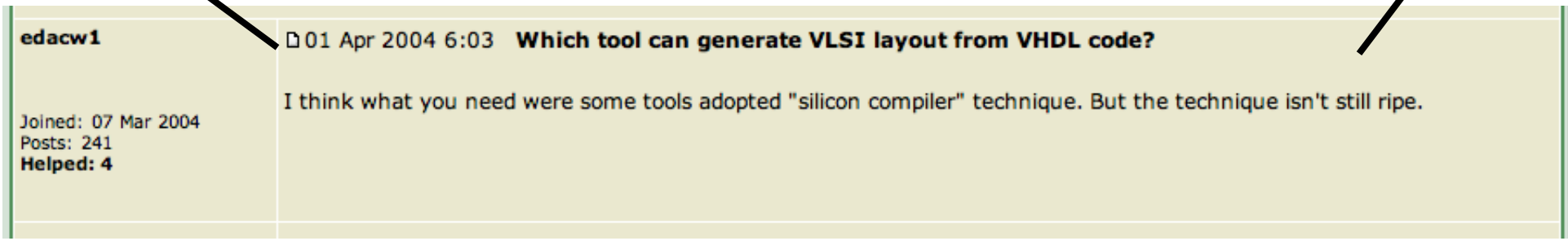
… a response came within a few hours

I think what you need [is] some tool adopted “silicon compiler”. But the technique isn’t still ripe.



edacw1 Joined: 07 Mar 2004 Posts: 241 **Helped: 4**	01 Apr 2004 6:03 **Which tool can generate VLSI layout from VHDL code?** I think what you need were some tools adopted "silicon compiler" technique. But the technique isn't still ripe.

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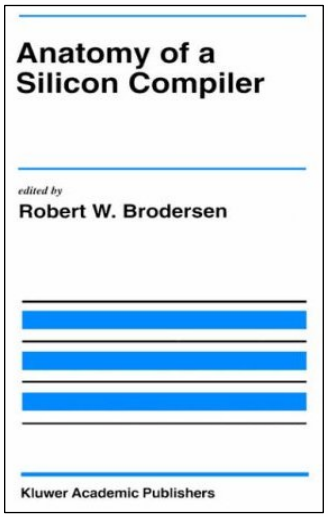
… so, what happened to the “Silicon Compiler”?

Carver A. Mead and George Lewicki, "Electronics" magazine 1982:

"Silicon compilers and foundries will usher in user-designed VLSI”




```
MODULE P801
 ... declarations ...
BODY P801;

 MODULE P8RI                    /* Read instruction     */
  ... declarations ...
  BODY P8RI;
  ...
 END P8RI;

 MODULE P8EXE                   /* Execute instruction */
  ... declarations ...
  BODY P8EXE;
   IF ¬((IR::0,6)=63)           /* String at bit 0,     */
    THEN                        /*        length 6 bit */
     WHEN  (IR::0,6)            /* Simple opcodes       */
      CASE 17;                  /* L   RT,D(RA)         */
       ...
      CASE 16;
       ...
     ENDCASE;
    ELSE
     IF ¬((IRT::21,4)=0)
      THEN
       PGM_FAULT:=1;            /* Undefined opcodes    */
      ELSE
       WHEN (IRT::25,7)         /* Extended opcodes     */
        CASE 17;                /* LX RT,RA,RB          */
         ...
        CASE 16;
         ...
       ENDCASE;
     ENDIF;
    ENDIF;
 END P8EXE;
```

References

1. R.K. Brayton, N.L. Brenner, C.L. Chen, G. DeMicheli, C.T. McMullen and R.H.J.M. Otten. The YORKTOWN Silicon Compiler. *1985 ISCAS Proceedings*, pages 391-394, Kyoto, June 1985.

2. R.K. Brayton, R. Camposano, G. DeMicheli, R.H.J.M. Otten and J.T.J. van Eijndhoven. The Yorktown Silicon Compiler System. in D. Gajski (Editor), editor, *Silicon Compilation*, Addison-Wesley, 1988. (also IBM Research Report RC 12500, Mathematics, Yorktown Heights, December 1986).

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… another prediction of the “Silicon Compiler”?

John Gray, Irene Buchanan, Peter Robertson, DAC 1982:

”…It allows the engineer to design for performance, wirability and testability by manipulating a textual description of a design. The principle features of this are a high-level language for design description, completely automatic layout, and an integrated simulator. The total package can be referred to as a silicon compiler…”

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They got it almost right…

… except that

"a high-level language"

should have meant

"a pile of files with many languages"

VHDL, Verilog, Spice, Systemverilog, C, C++, SystemC, BlueSpec, UML, …

and then the other "beauties" such as

tcl, grep, awk, sed, perl, sh, csh, ksh, bash, …

What do I want, as a designer?

Tools that…

- … produce “optimal” results for me.
  - … results that are predictable and repeatable.
  - … results that are incremental.
- … know what results I will like and takes it into account.
- … I can micromanage when needed because I am an Engineer!

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What do we give them?

Many Tools that…

- … utilize instable algorithms
- … have many variations and thousands of options
- … and are buggy

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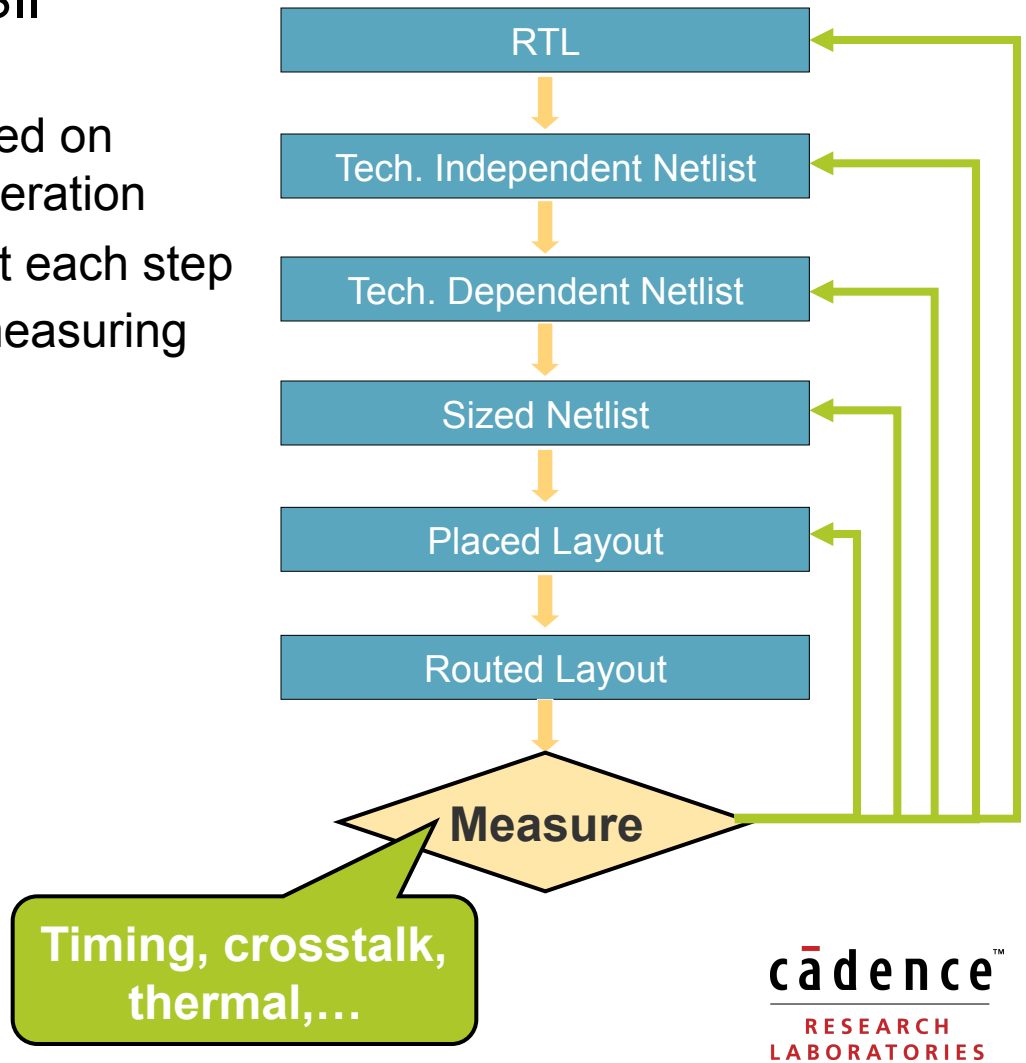
Today's Design Flows are Split into many Steps

- There is **no** monolithic optimization approach to the RTL-to-GDSII synthesis problem
  - Traditional approaches based on horizontal flow slicing and iteration
  - Simplified models applied at each step
  - Optimization achieved by measuring and readjusting weights
- There is **no** guarantee of convergence!
- There is **no** guarantee of incrementality
- Result:
  - Extremely instable flows



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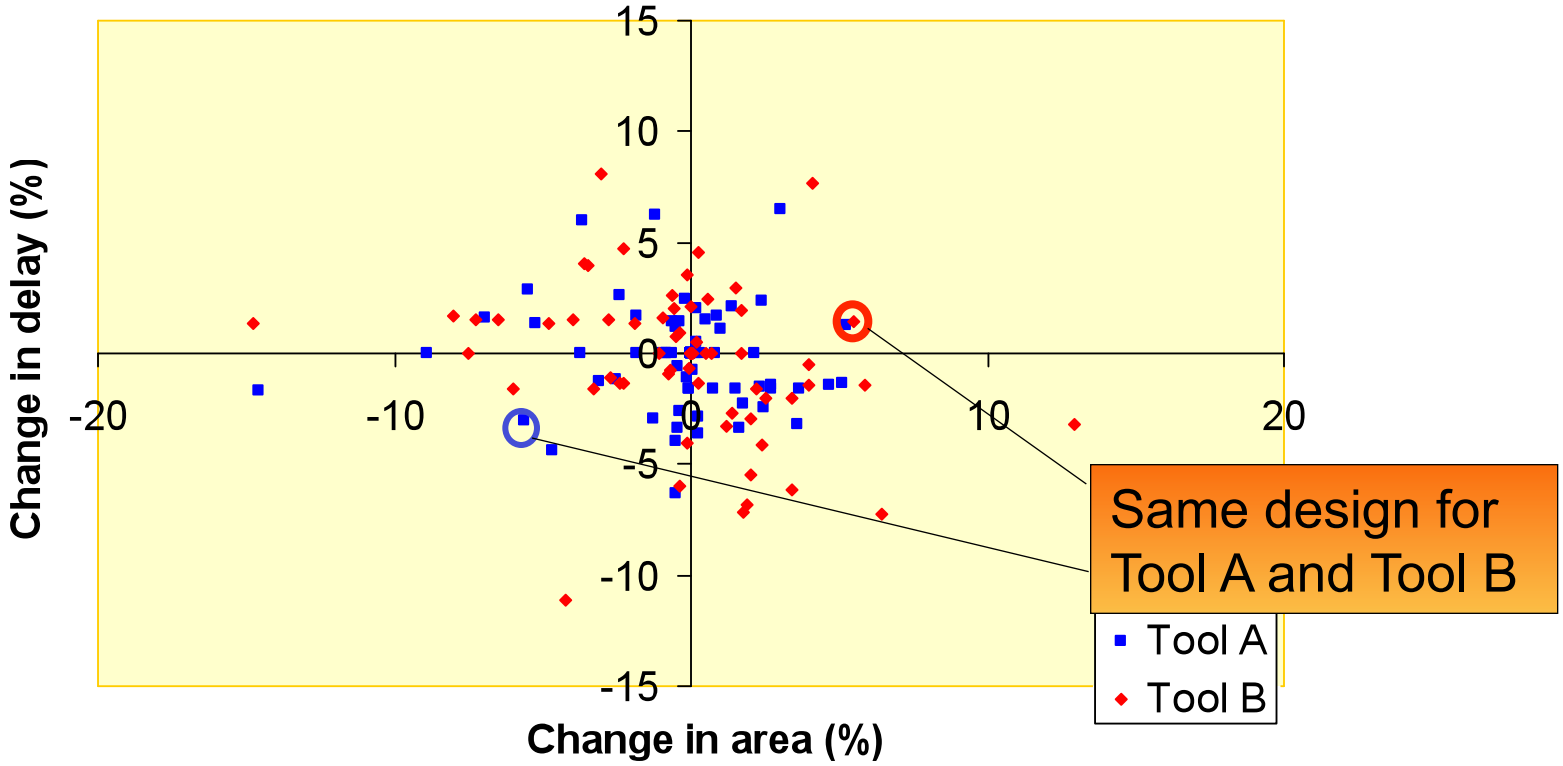
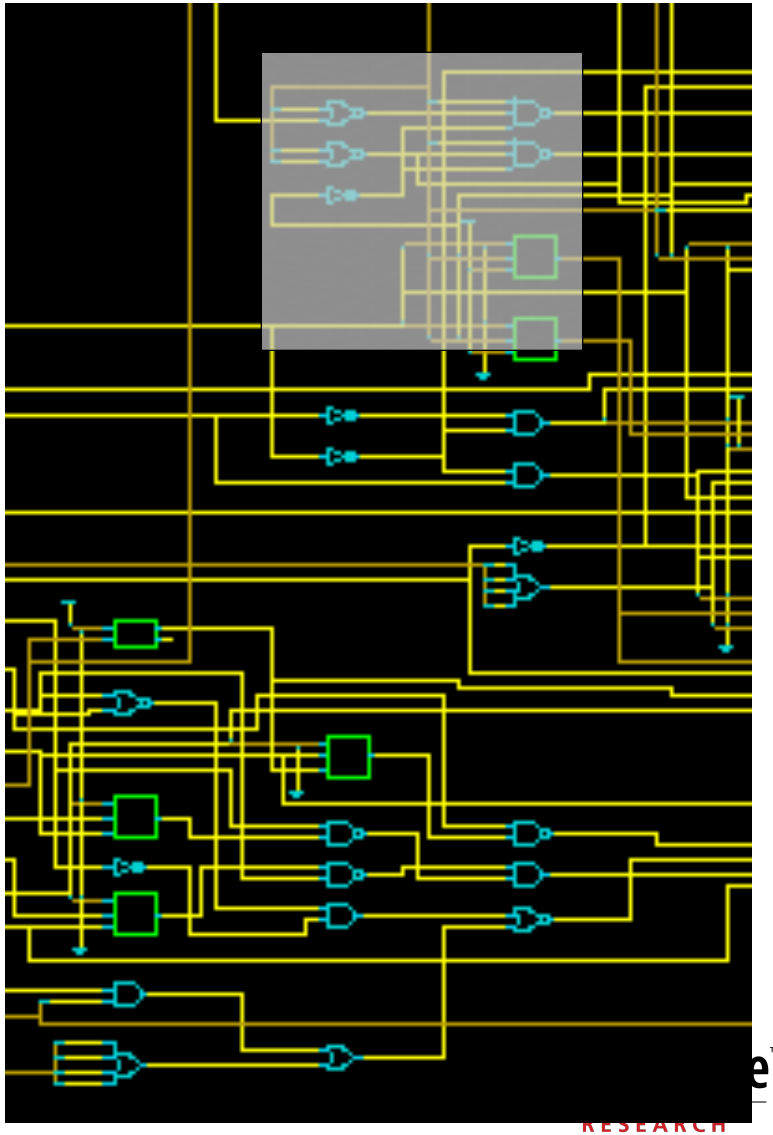
Example: Instability of Logic Synthesis

- Logic synthesis experiment with public benchmarks (IWLS 2005)
  - Original RTL synthesized versus identical RTL with names mangled



Why is it like this – three reasons?

- Reason # 1: Windowing
  - Many synthesis algorithms don't scale and need to be applied to a small window. The window is being shifted over the design which make the results order dependent which can dramatically change with a small change of the design.



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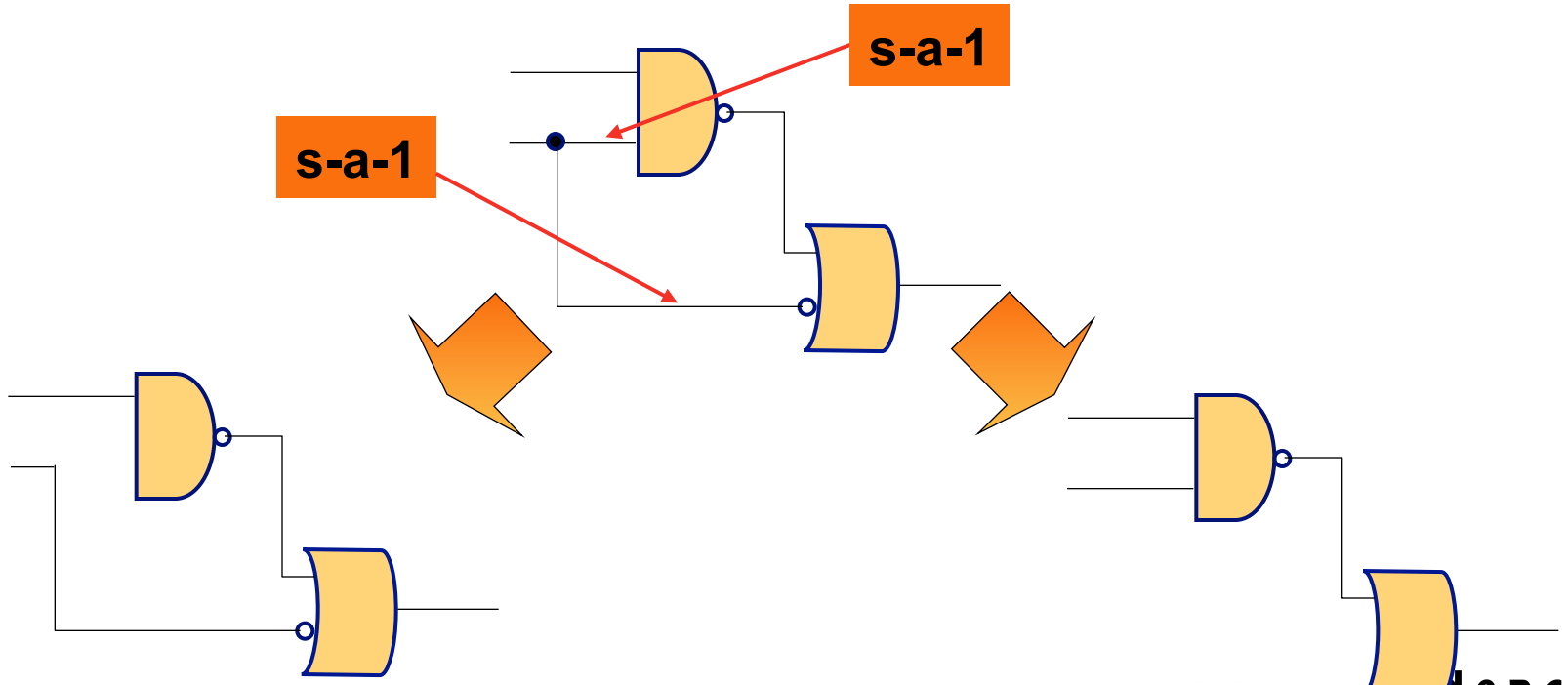
Why is it like this – three reasons?

- Reason # 2: Decision Threshold
  - The complexity of many synthesis algorithm is controlled by resource thresholds after which a transformation attempt is aborted. A small change of the design can cause a jump over the threshold spawning completely different results.

```
int search(unsigned max_backtracks)
{
  for(i = 0; i < max_backtracks; i++) {
    success = try_something(i);
    if(success) return 1;
  }
  return 0;
}
```

Why is it like this – three reasons?

- Reason # 3: Order of transformations
  - Certain transformation on single nets are mutually exclusive. Depending on the order in which they are applied a different outcome can be produced.



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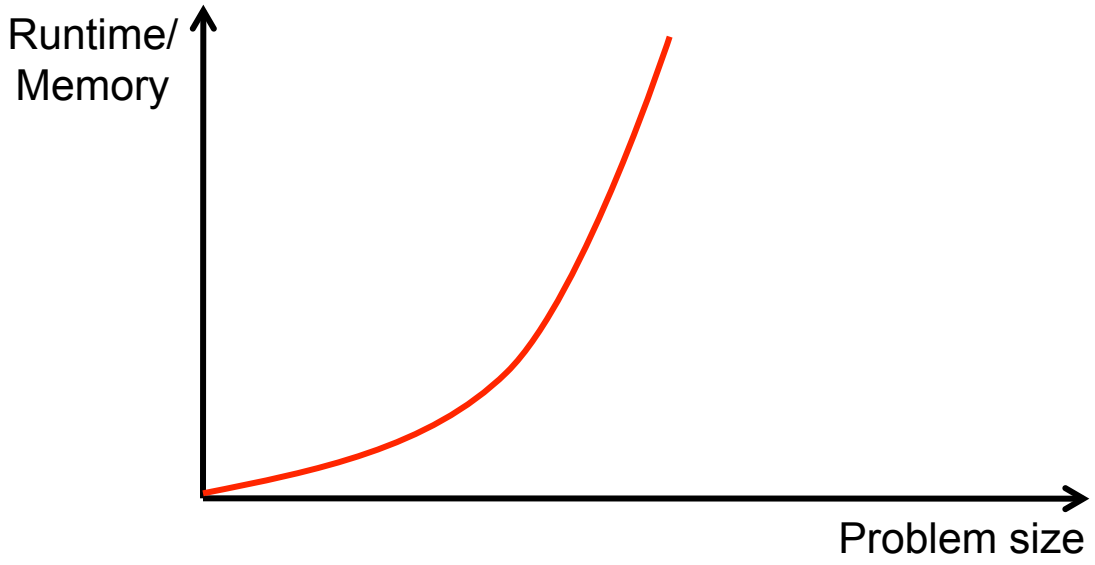
Most algorithms are computationally hard: NP-hard or worse

Logic optimization, technology mapping, placement, routing, verification, …



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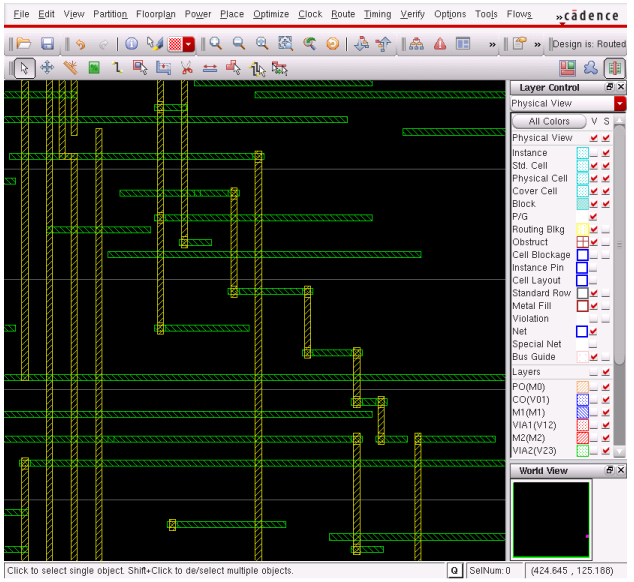
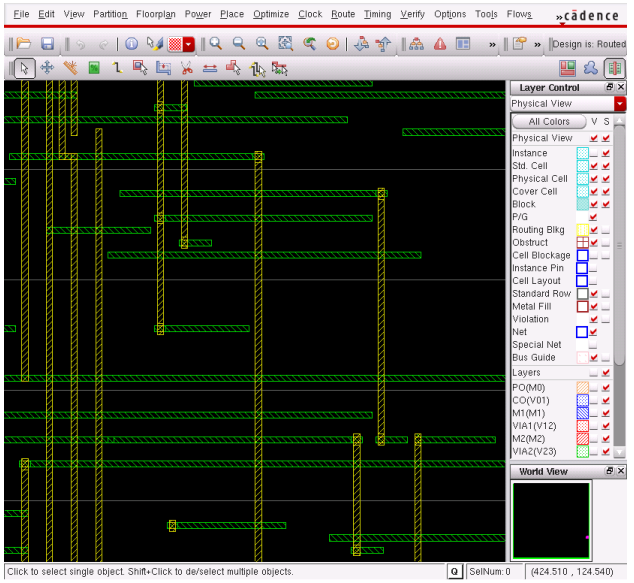
How do we solve the problem?

Ingredient #1:
Let's add another option to the tool!

```
…
setRouteMode -routemagictrick 34876
…
```





- Can solve any problem such as
  - "I know a better route"
- Number of options:
  O(n*m*k)
  - n – number of designs
  - m – number designers
  - k – number of features to be controlled

How do we solve the problem?

Ingredient #2:

If you don't like what the tool does …

… why don't you program it yourself!

```
…
Source my_magic_script.tcl
…
```

Very clever!

- Outsources programming from the tool provider to its customer
- Gives the illusion of freedom
- Makes tool sticky

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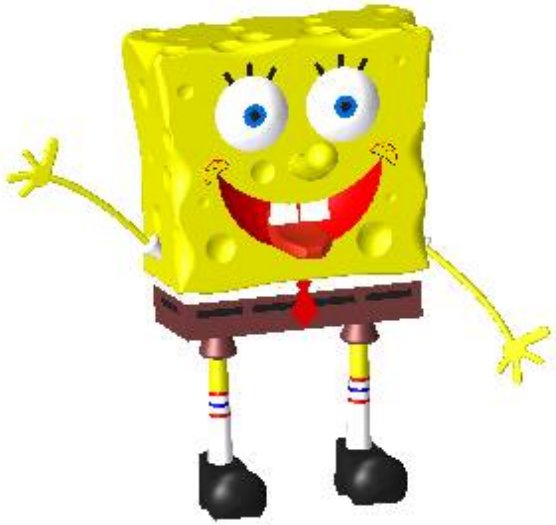
How do we solve the problem?

Ingredient #3:

We ship a neural network with the tool that helps you navigate through the maze

Also called:

Application Engineer



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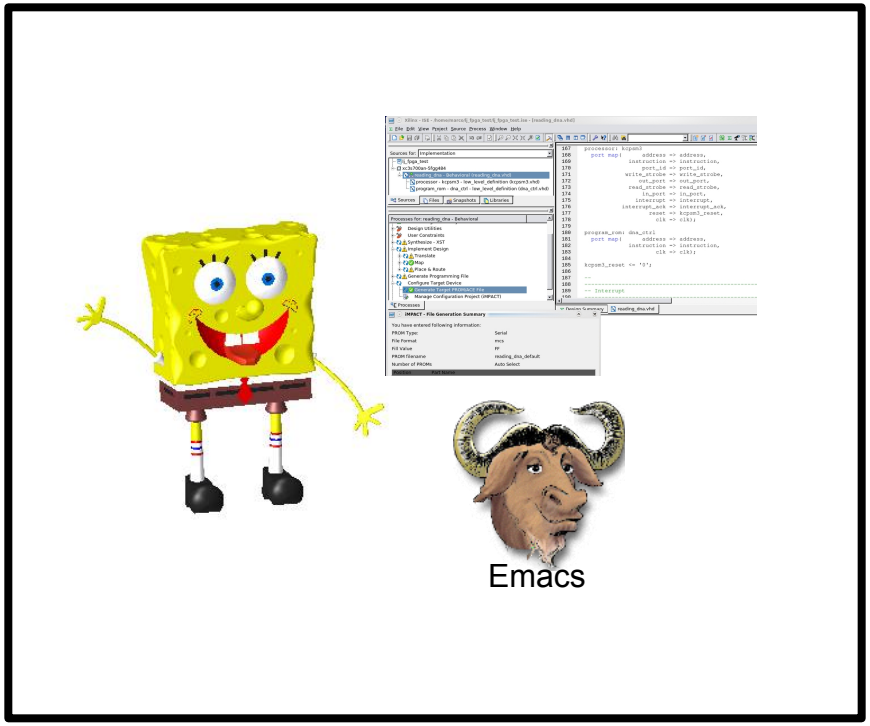
All together it makes…

SiliconCompiler 2.0



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Thank you!

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