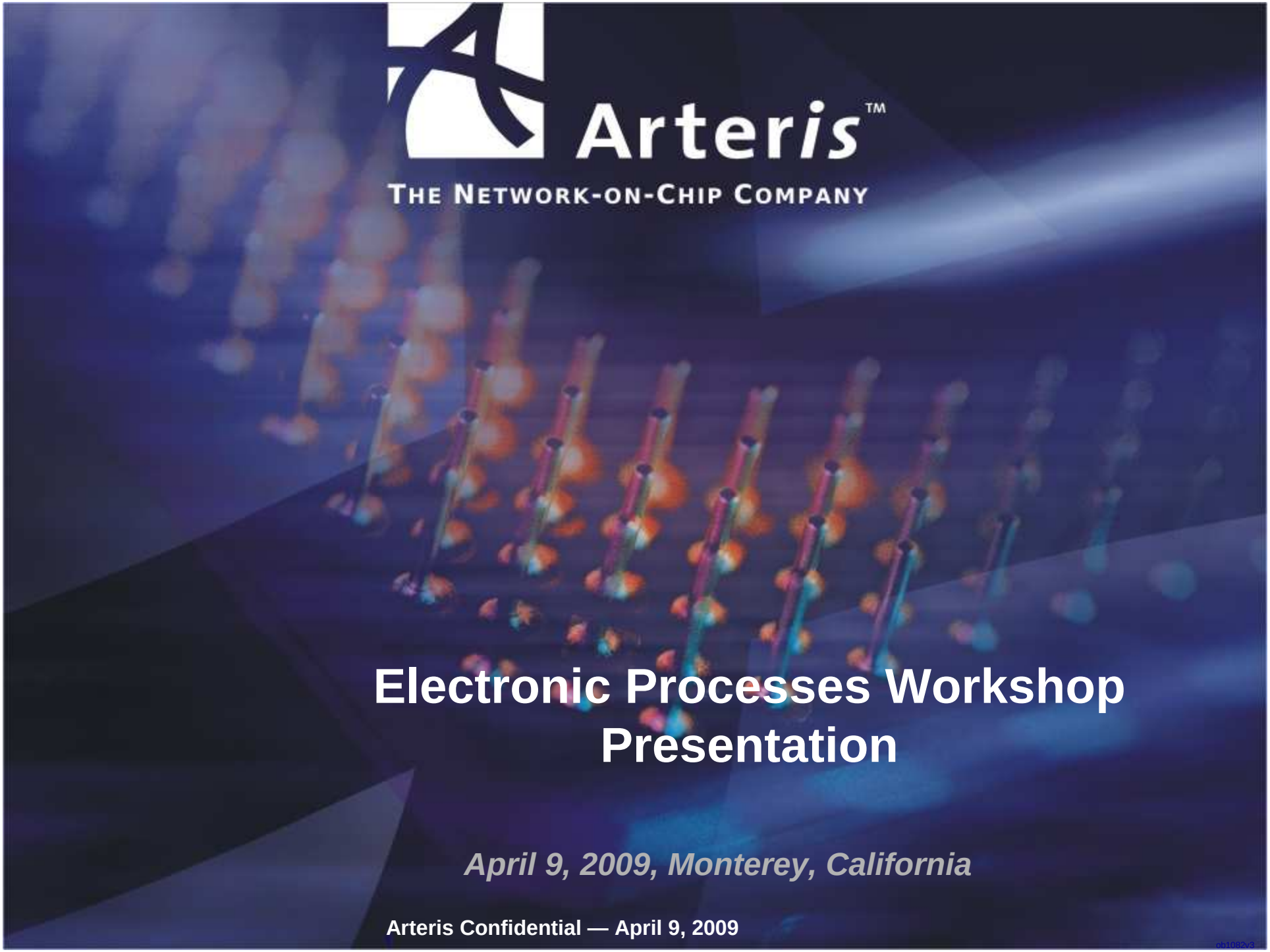
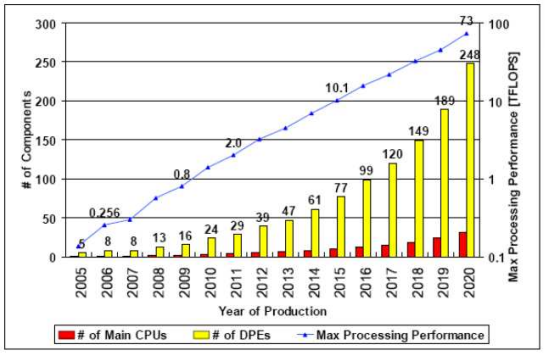


Electronic Processes Workshop Presentation

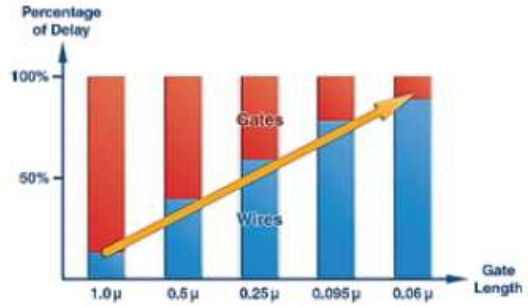
April 9, 2009, Monterey, California

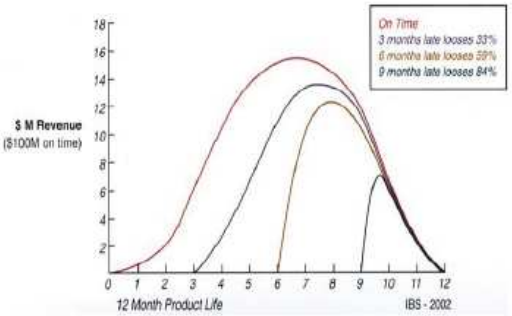
Why is it Time to Get off The Bus? (at the top level)

- SoC Complexity Increasing
  - More software applications on a single device
  - Number of IP blocks on Chip increasing
  - Heterogeneous IP communication standards
- Creating SoC Delivery Bottlenecks
  - Access to data (Memory bandwidth)
  - IP block interconnect
  - SoC design verification
  - Software development of final application
  - Too many physical wires in the design
- Impacting Time to Market (and Money)
  - Missing a market window causes profit losses
  - Being quicker to market applies to all SoCs



Source: International Technology Roadmap for Semiconductors



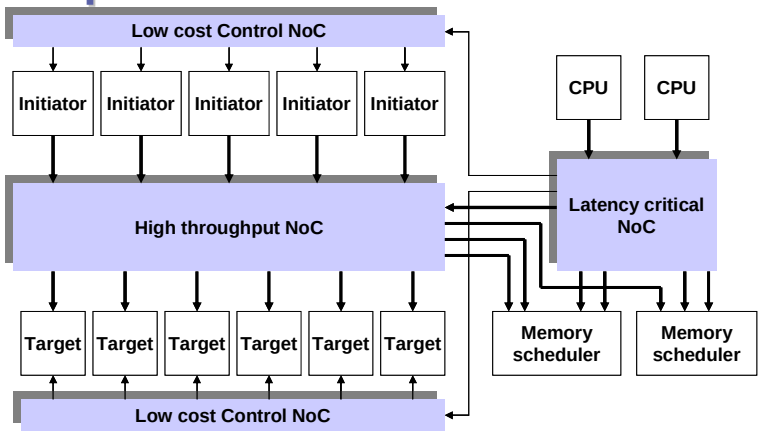


Who is Hitting These Problems First? The Mobility Eco-System

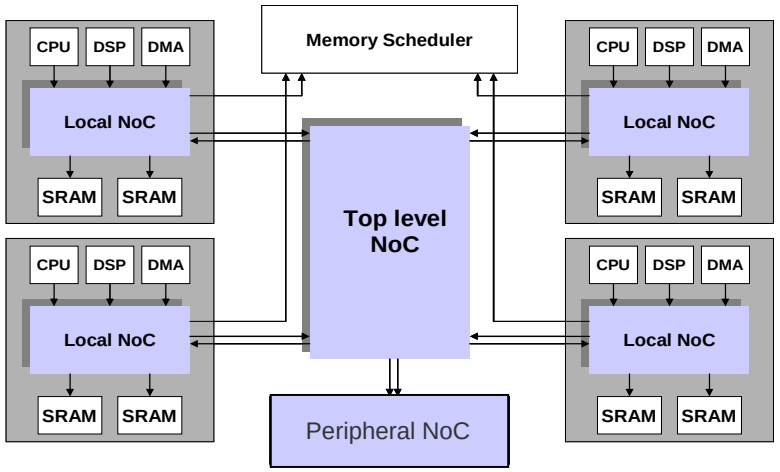
- Leading SC, device, portal and wireless companies will design and deploy 1,000,000,000 complex SoCs to enhance capabilities and differentiation
- A race to built a true and connected personal computer

What is the Answer? A Unified NoC Architecture

Separated traffic Classes



Clustered design

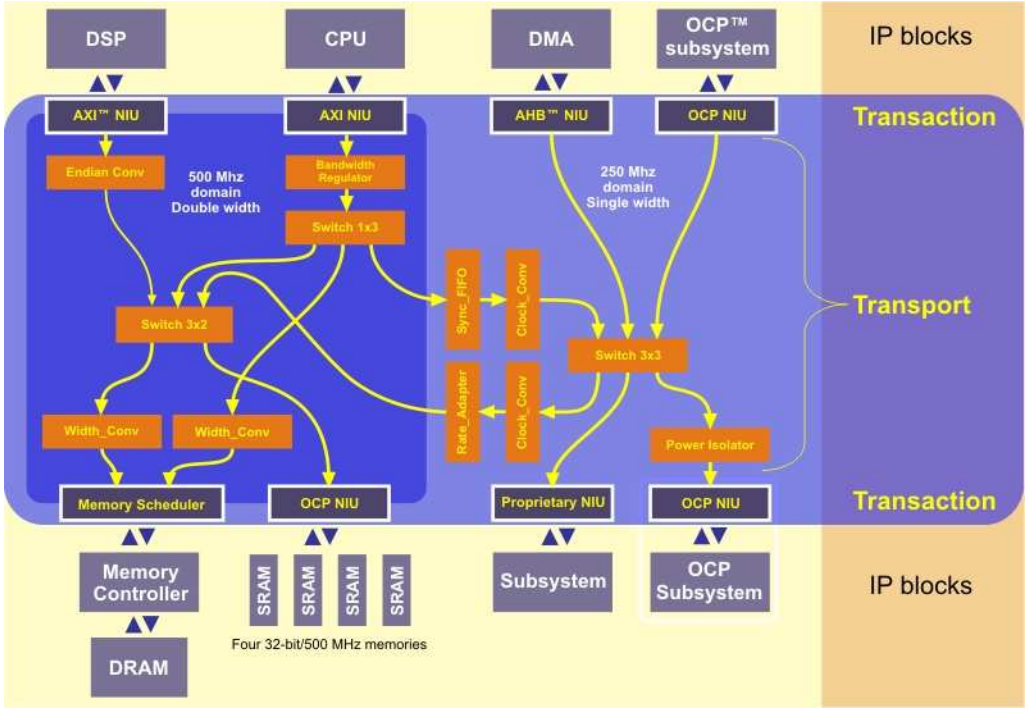


- Top level interconnect: **Scalability, Power, Performance**
- Block level interconnect: **Latency, IP Flexibility, Fast Cycles**
- Multiple Dies in SIP: **Speed, Latency, Simple Software**
- Peripheral interconnect: **Wire conservation, area**

NoC Technology Keeps Pace with SoC Innovation

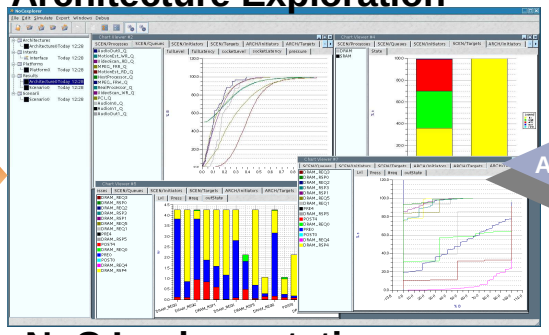
A NoC Instance consists of parameterizable NoC IP elements, Enhances SoC Scalability, low power and high performance

- Network interface units
- Switches
- Rate adaptors
- Width adaptors
- Arbitration blocks
- Sync./Async. FIFOs
- Endianness converters
- Statistical counters
- Clock/reset units
- …..



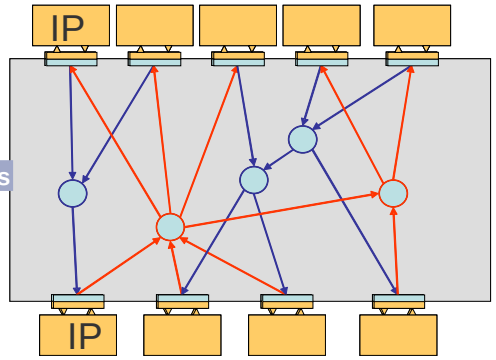
NoC Tools Accelerate SoC Delivery

Architecture Exploration

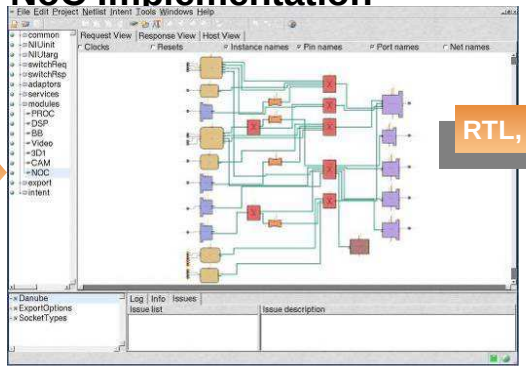


ARTERIS NoC library

Application Requirements

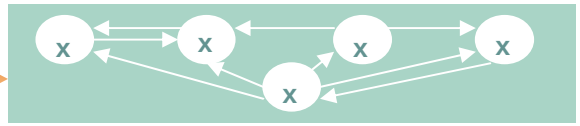


NoC Implementation



ARTERIS RTL NoC library

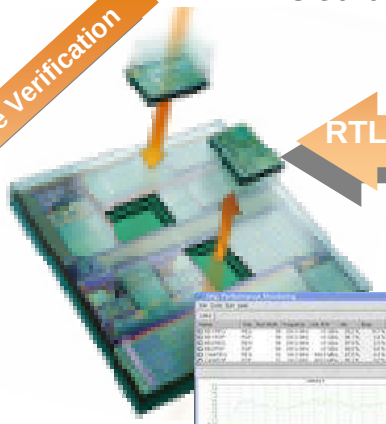
RTL, Scripts, Test bench



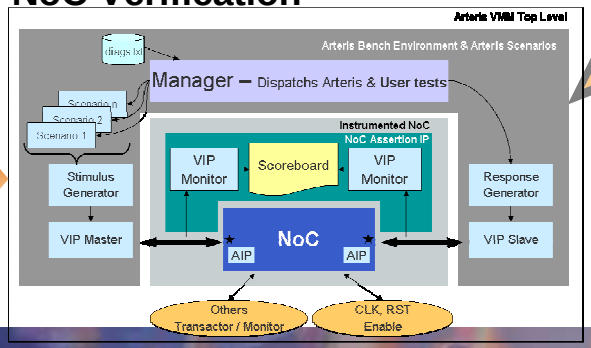
ARTERIS Generated NoC Instance

NoC Instance Verification

RTL to GDSII

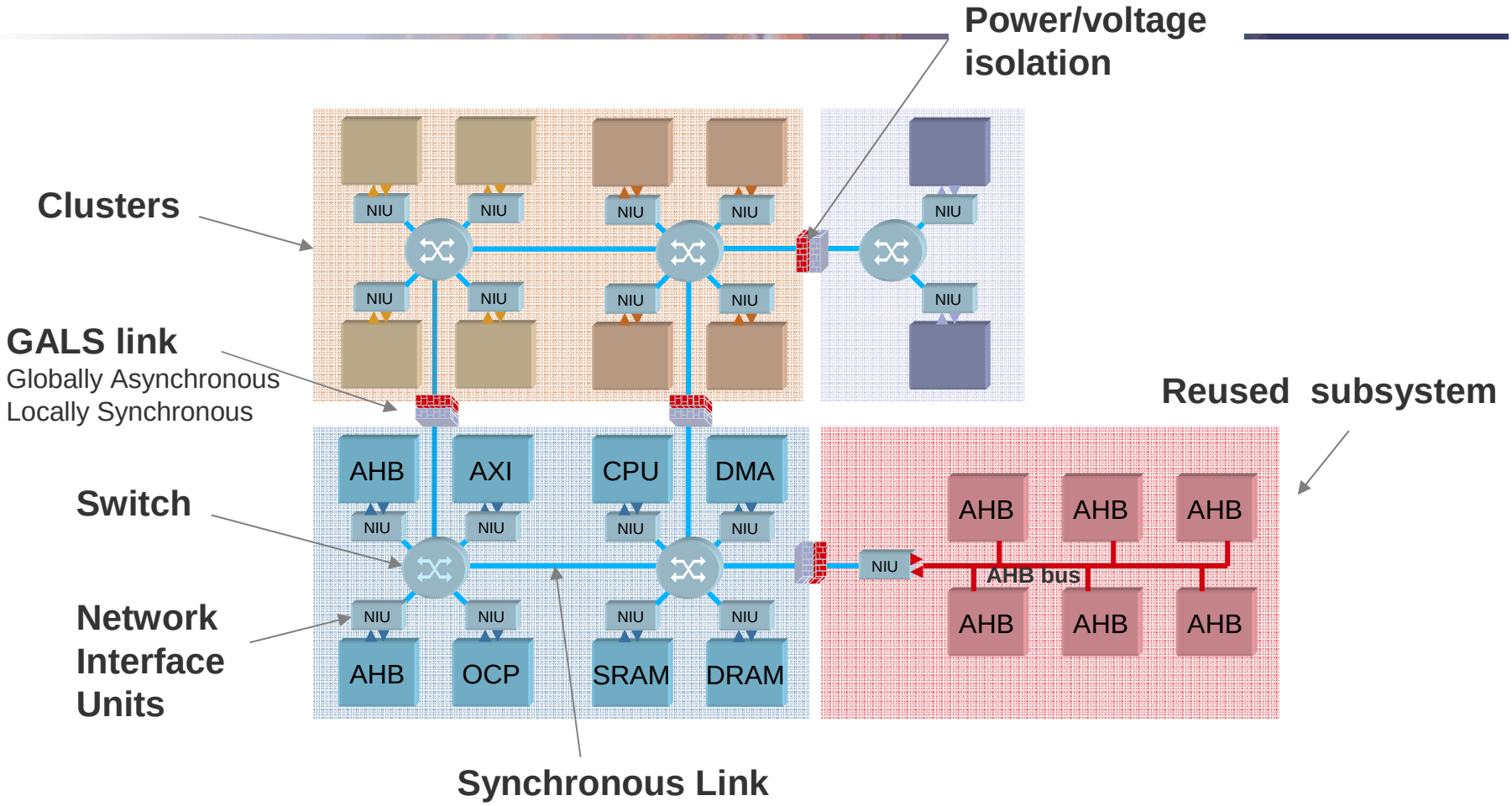


NoC Verification



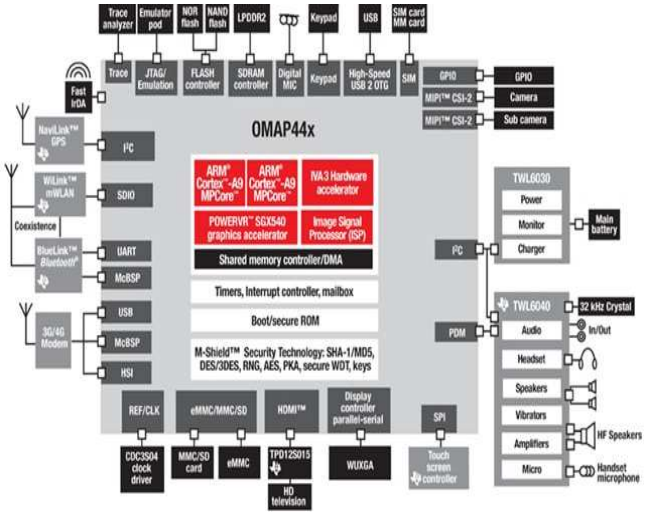
Synopsys Verification IP

GALS: Divide and Conquer, Without Redoing Everything

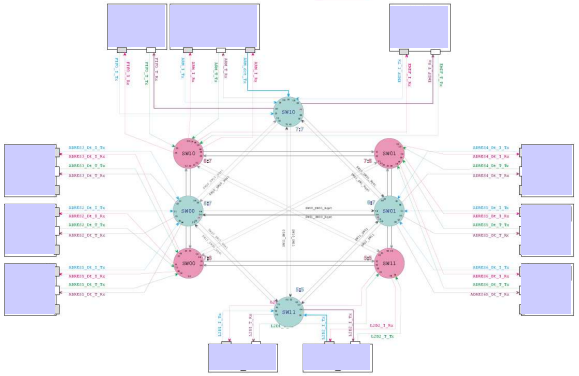


- Low power – <1mW idle power for 500K gate NoC IP at 65nm LP
- High speed – up to 750Mhz using 65nm TSMC Library
- High bandwidth – NoC links scalable from 16 to 256 bits

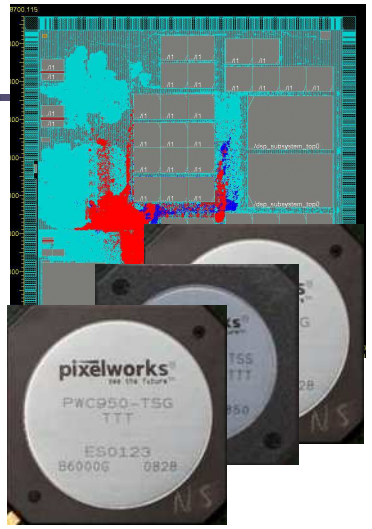
Are NoCs a Commercial Reality? Yes They Are!

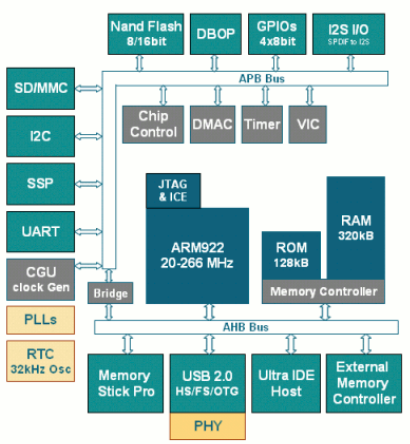


Wireless Application Processor



Multimedia Processor





Automotive Infotainment

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