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Is the SoC Analog (EDA) Revolution Really Here?

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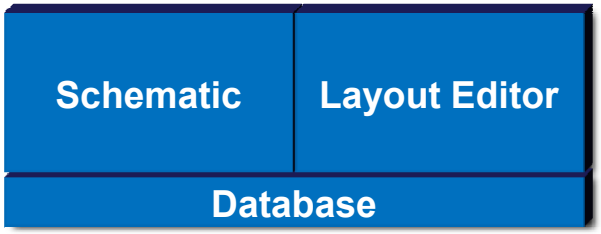
Analog Physical EDA: 15 Yrs of Evolution

- Trickle of EDA innovations
  - CAD frameworks in the early 1990s
    - Unified electrical, physical representation
  - PCells for device layout
  - Schematic Driven Layout in mid-1990's
  - Shape-based routing for top-level assembly
  - Productivity and usability features in layout tools



- Several commercial attempts at radical automation
  - Neolinear, Barcelona …
  - Limited use on production designs

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You Say You Want a Revolution …

… so why are we still doing it the same old way ?

- Not enough value?
  A. QoR penalty too large?
  B. Productivity benefit too small – too much setup/use effort ?

- Cultural ?
  - ~~"Analog people don't want tools" (!?)~~ disagree !
  - Decline of "strategic CAD" → emphasis on current-design payoff
    - Means quick Design Team adoption is critical
      - Alternative is not "don't automate" but "automate next time"
    - Revolution = huge value proposition with no risk

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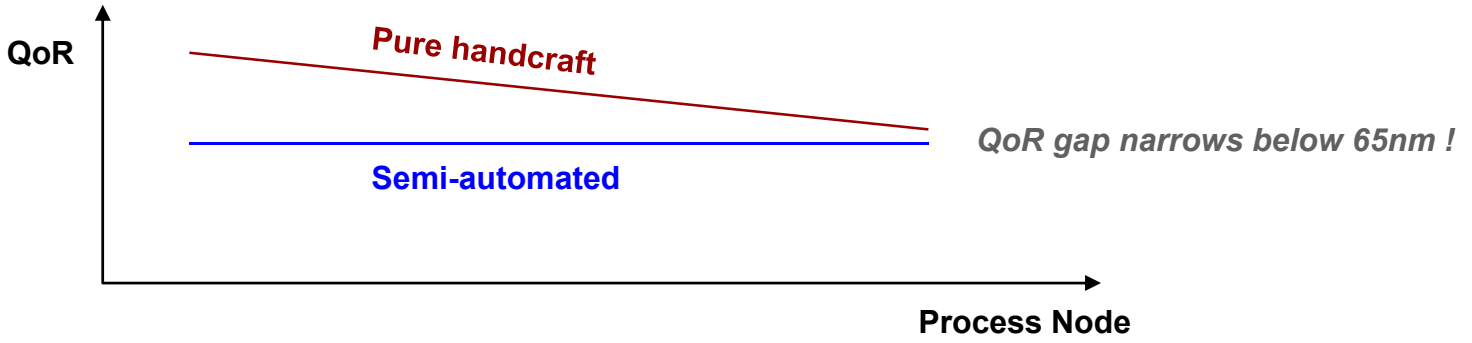
A. QoR – 3 Components

1. Circuit requirements – matching, symmetry …
   - Requires experienced designer
2. Device-level optimizations – abutment, well merging …
   - Automate, but accept human designer can usually do better
3. Optimization to design rules
   - Automation may outperform human designer below 65nm



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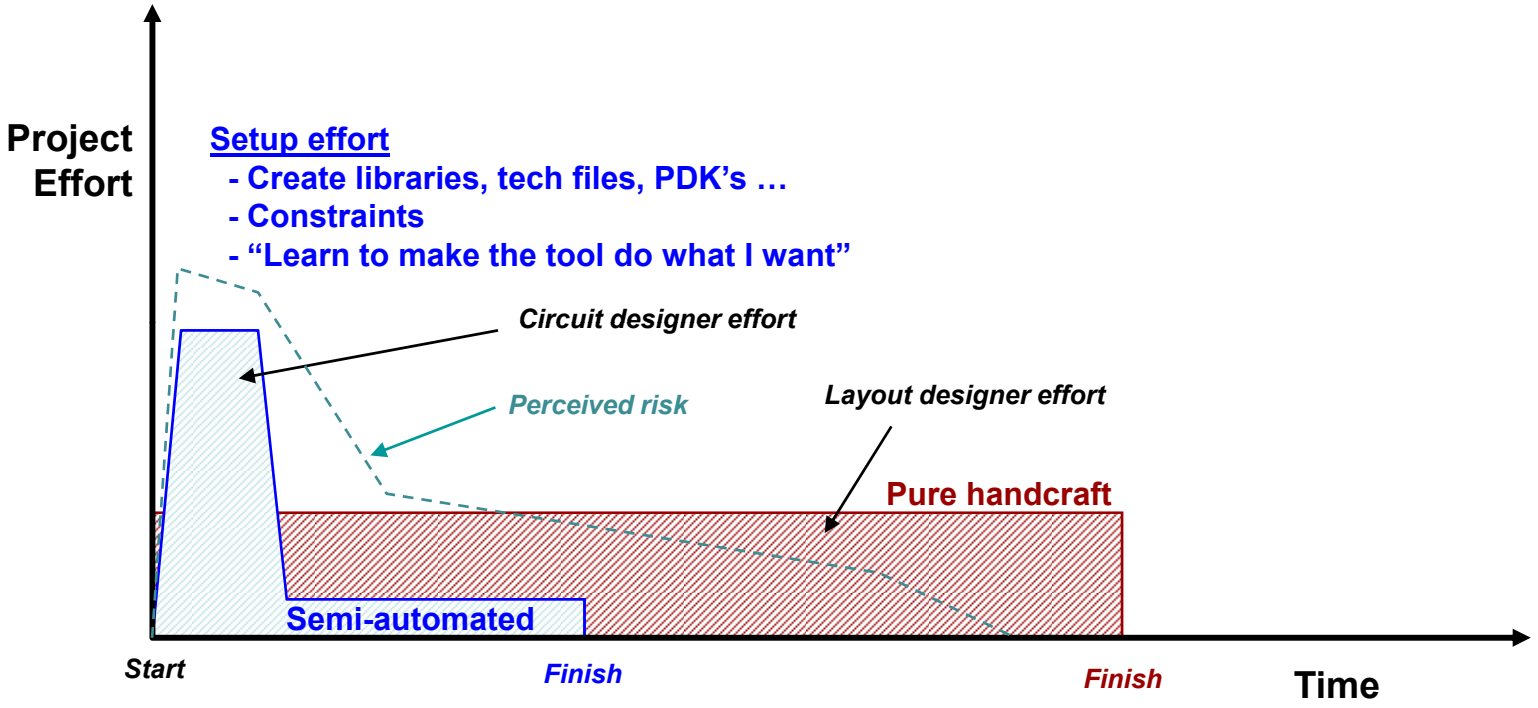
B. TTM and Productivity



Don't laugh! … this is a big deal to design teams, and CAD groups are no longer funded to make visionary methodology investments!

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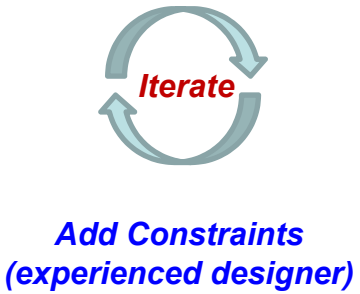
TTM: Iterations are Inherent



- Example: communications circuit, 832 devices, 90nm
- 4 levels hierarchy, 24 subcircuits
- Total cycle netlist-to-fully-constrained placement = 11hrs
- ***40-50*** total constraint/placement iterations used

  Must be easy – must be fast!
  - 1-3 runs on each leaf-level subcircuit
  - 3-5 runs at mid-levels
  - 2-4 runs on full design
- Placement run times (1 CPU)
  - Full circuit – minutes
  - Subcircuits – seconds

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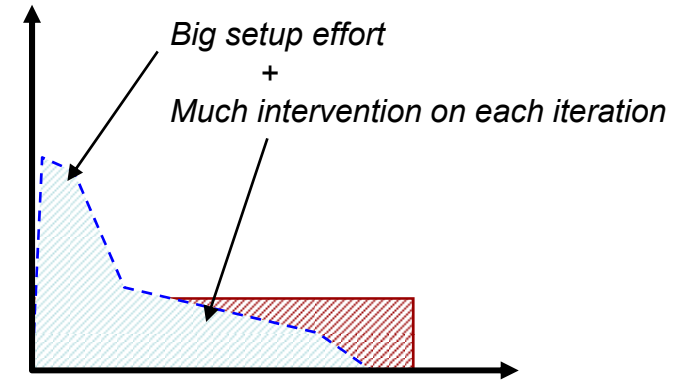
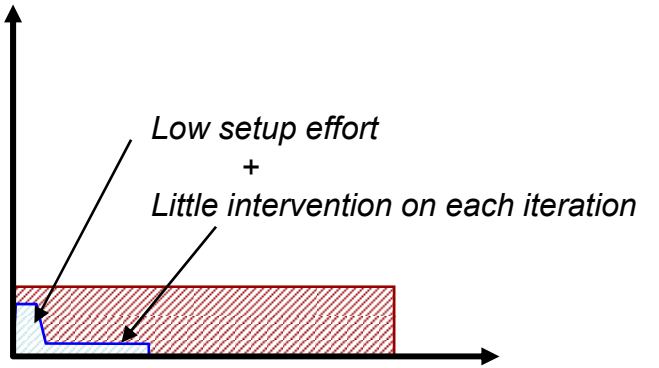
Summary – it's an ENGINE Revolution



Designers Don't Accept … Revolution Fails!



Designers Accept … Revolution has Chance for Success

Automation = QoR + Low *Setup* Effort + Low *Iteration* Effort

- Layout engine must be easy to control by designers
  - Good QoR from simple (and "imperfect") geometric constraints
- Must do device-level optimization and DRC-correct automatically
  - NO manual editing allowed within iterations
- Run times must be fast

This is architecture stuff – not GUI / flow stuff

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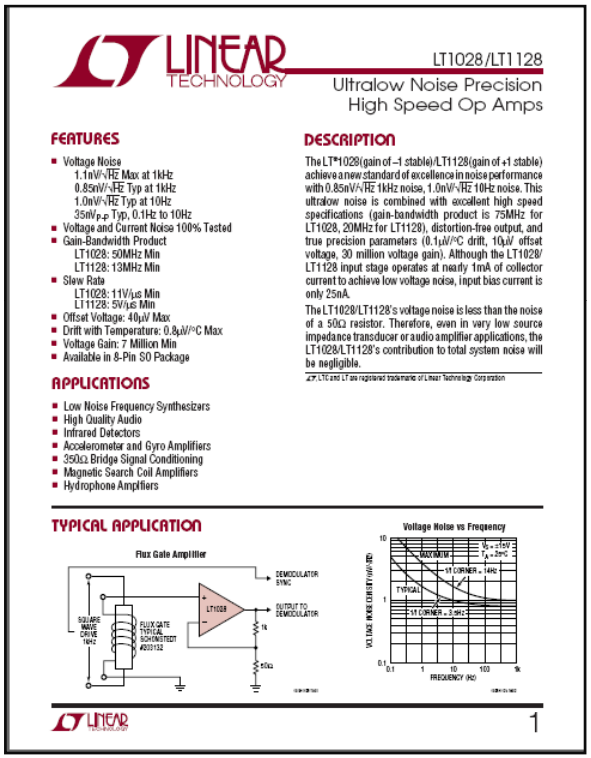
Target Market: "Analog" vs "SoC Analog"

Traditional Analog/Mixed-Signal



LINEAR TECHNOLOGY

LT1028/LT1128

Ultralow Noise Precision High Speed Op Amps

FEATURES

- Voltage Noise
  - 1.1nV/√Hz Max at 1kHz
  - 0.85nV/√Hz Typ at 1kHz
  - 1.0nV/√Hz Typ at 10Hz
  - 35nV$_{P-P}$ Typ, 0.1Hz to 10Hz
- Voltage and Current Noise 100% Tested
- Gain-Bandwidth Product
  - LT1028: 50MHz Min
  - LT1128: 13MHz Min
- Slew Rate
  - LT1028: 11V/µs Min
  - LT1128: 5V/µs Min
- Offset Voltage: 40µV Max
- Drift with Temperature: 0.8µV/°C Max
- Voltage Gain: 7 Million Min
- Available in 8-Pin SO Package

DESCRIPTION

The LT®1028 (gain of –1 stable) /LT1128 (gain of +1 stable) achieve a new standard of excellence in noise performance with 0.85nV/√Hz 1kHz noise, 1.0nV/√Hz 10Hz noise. This ultralow noise is combined with excellent high speed specifications (gain-bandwidth product is 75MHz for LT1028, 20MHz for LT1128), distortion-free output, and true precision parameters (0.1µV/°C drift, 10µV offset voltage, 30 million voltage gain). Although the LT1028/LT1128 input stage operates at nearly 1mA of collector current to achieve low voltage noise, input bias current is only 25nA.

The LT1028/LT1128's voltage noise is less than the noise of a 50Ω resistor. Therefore, even in very low source impedance transducer or audio amplifier applications, the LT1028/LT1128's contribution to total system noise will be negligible.

LT, LTC and LT are registered trademarks of Linear Technology Corporation

APPLICATIONS

- Low Noise Frequency Synthesizers
- High Quality Audio
- Infrared Detectors
- Accelerometer and Gyro Amplifiers
- 350Ω Bridge Signal Conditioning
- Magnetic Search Coil Amplifiers
- Hydrophone Amplifiers

TYPICAL APPLICATION

Flux Gate Amplifier

Voltage Noise vs Frequency

1

Compete on Analog QoR

Need "good enough" TTM

SoC Analog/Mixed-Signal

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Introducing BlueCore7

Bluetooth, Bluetooth low energy, GPS and FM radio in a single chip

See it in action ▸

Home | Bluetooth | Bluetooth low energy | FM Rx / Tx | GPS | Device details | Development | Find out more

Single-chip breakthrough combines Bluetooth, Bluetooth low energy, GPS and FM radio technologies

BlueCore7 is a breakthrough solution for adding wireless-related connectivity features into mobile handsets. Combining Bluetooth, Bluetooth low energy (ULP), enhanced GPS and FM radio reception and transmission, the single-chip is the world's most highly integrated wireless solution for embedded applications.

CSR has created many innovative RF chips that combine Bluetooth functionality with other attractive consumer features. The ROM-based BlueCore7 takes this formula to a new level, with no less than four major wireless systems, giving handset developm to create exciting new product ranges.

Key functions are:

- A Bluetooth v2.1 + EDR radio delivering +10dB
- An AuriStream voice CODEC that can provide or reduced power consumption
- A Bluetooth low energy radio - very low-power devices such as watches, training shoes, TV remote con
- Enhanced GPS, a revolutionary platform for int handsets, offering fast and reliable positioning data - even d life
- An FM radio receiver *and* short-range transmitter. The receiver has speaker drivers for direct

Compete on TTM with More Features

Need "good enough" QoR on analog/mixed-signal IP

Right target market for automation: integration of analog/mixed-signal content into Nanometer CMOS SoC's

Automation = trade off a little QoR for a lot of TTM

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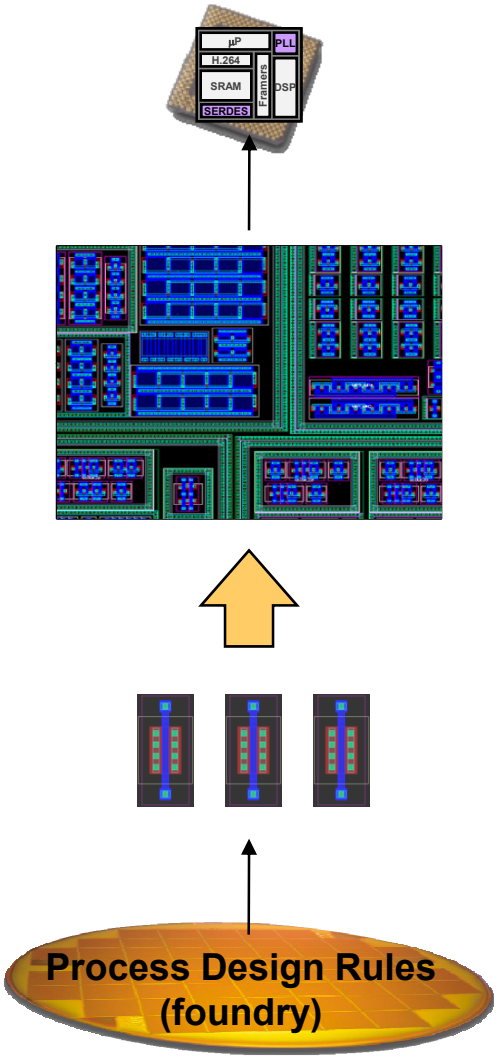
Solve Device and Circuit Layout Together



No clean division

- *Circuit (Schematic)*
- *Devices (PCells/PDKs)*
- *Design rules*

Must automate at both levels at once, in full context of design rules

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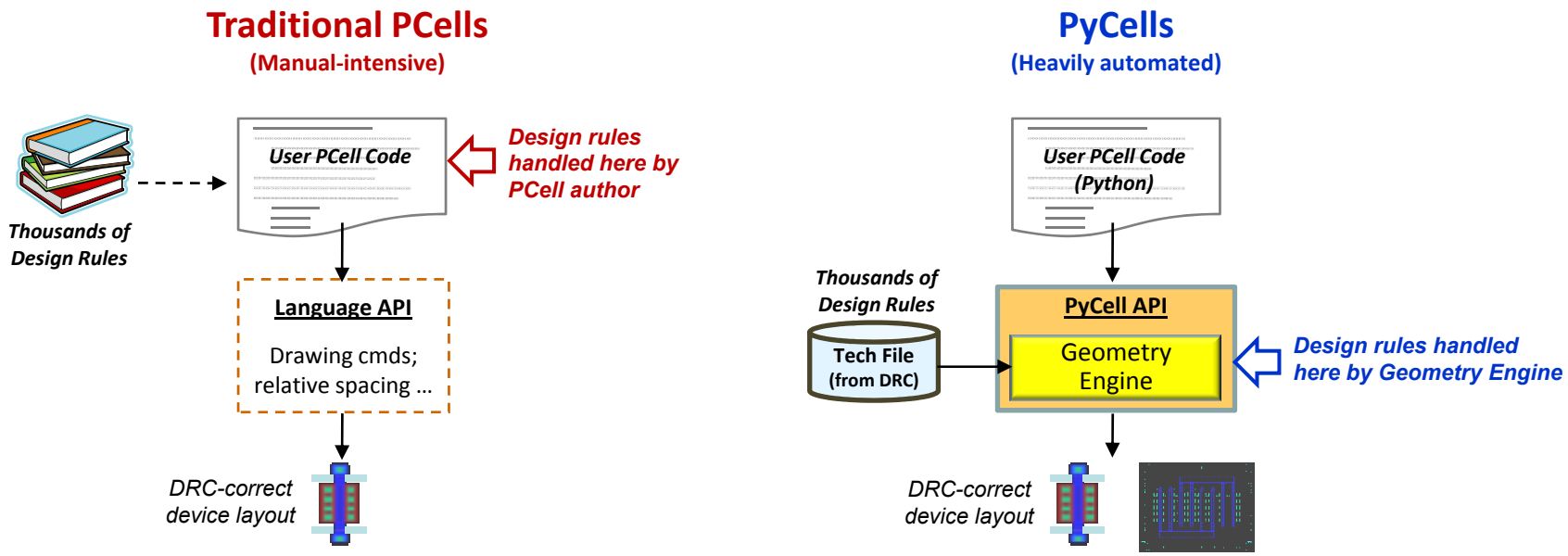
Nanometer PDKs – Revolution is Underway



PyCells – intelligent PDK's

- << ½ the lines of code at 65nm and below
- Fast to port PyCells to new process nodes → *essential for porting higher-level IP*
- Facilitates higher-level PDK IP

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Nanometer PDKs – Revolution is Underway

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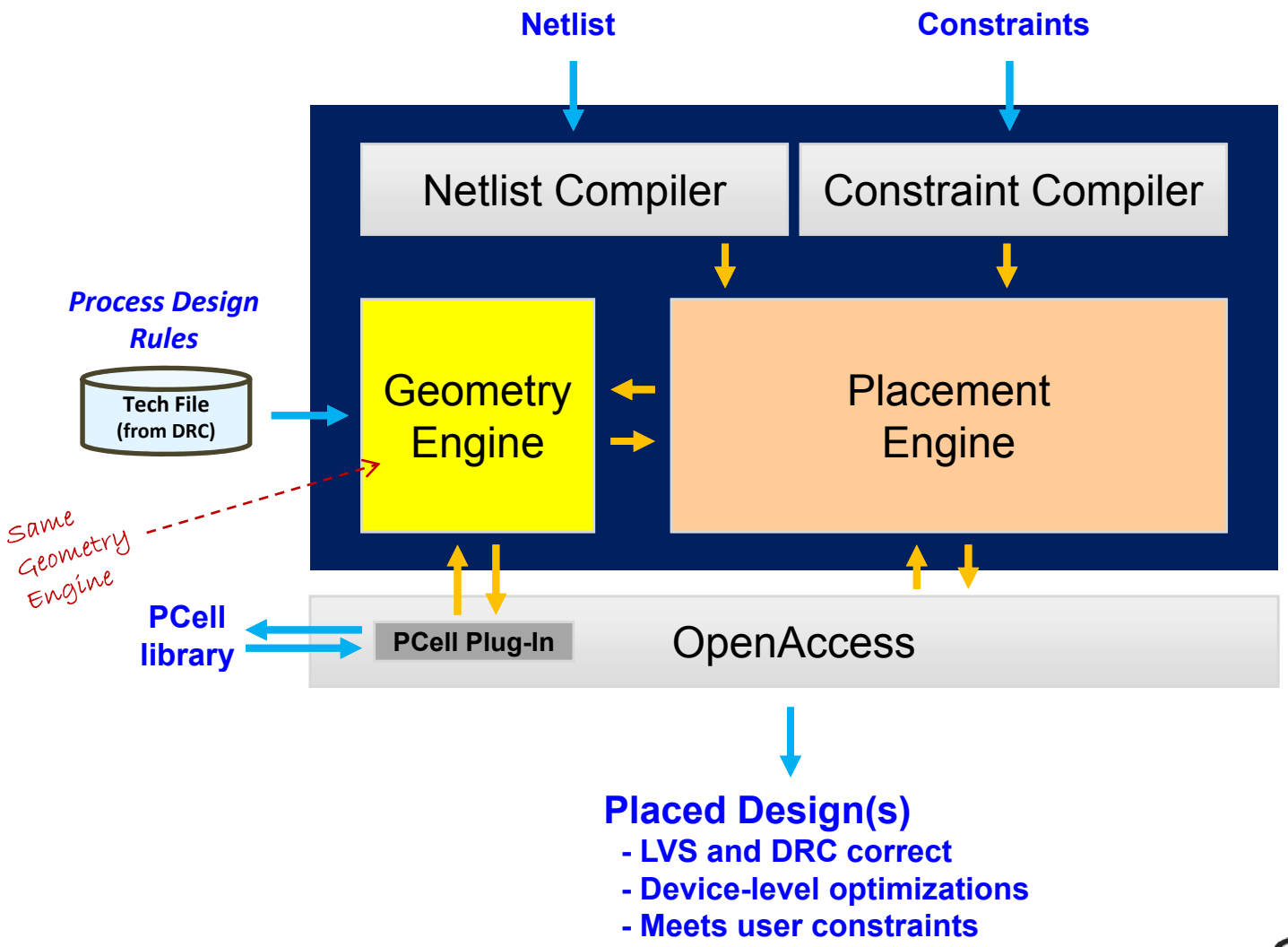
Taiwan Semiconductor Manufacturing Company Limited

CIRANOVA AND TSMC ANNOUNCE STRATEGIC PARTNERSHIP ON ADVANCED PDK TECHNOLOGY

Issued by: Ciranova and TSMC
Issued on: 2009/03/24

SANTA CLARA, Calif. – March 24, 2009 – Taiwan Semiconductor Manufacturing Company, Ltd. (TSE: 2330, NYSE: TSM) and Ciranova™ announced a multi-year strategic partnership to collaborate on the development of advanced Process Design Kit (PDK) technology based on Ciranova's PyCell architecture. The results of

Automated-Placement Architecture



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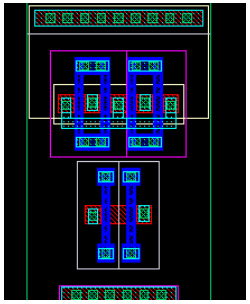
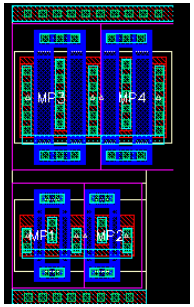
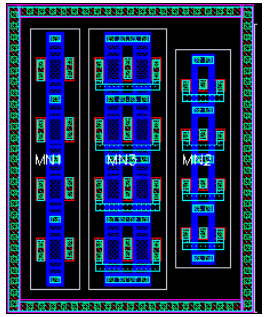
Placement QoR



Device Abutment



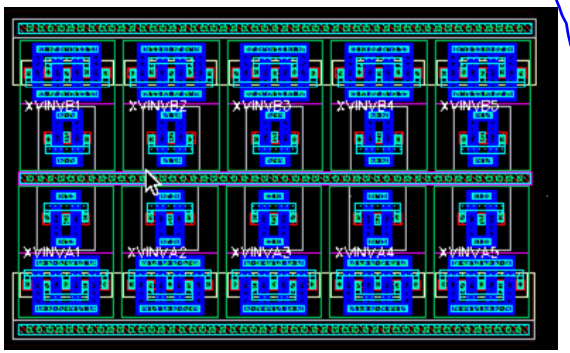
Well Merging



Row Stacking

Device-Level Optimizations
(automated)

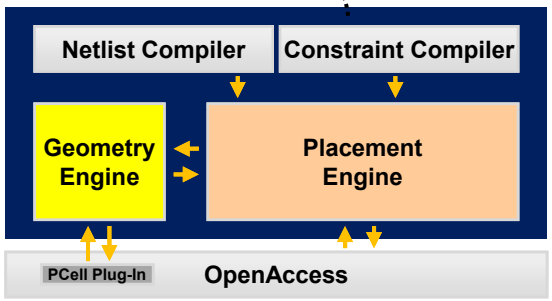
Circuit Requirements
(designer defines, tool implements)



Symmetry

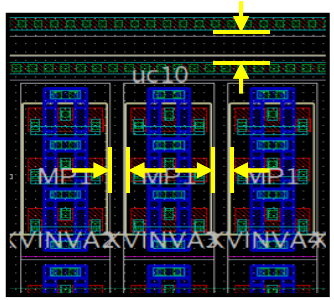
- Align inverters XINVA1-5 in a row
- Align inverters XVINB 1-5 in a row
- Stack the two rows in a column
- Flip the top row vertically

Can override



Your Backbone Schematic/Layout Flow

DRC Optimizations
(automated)



Spacing

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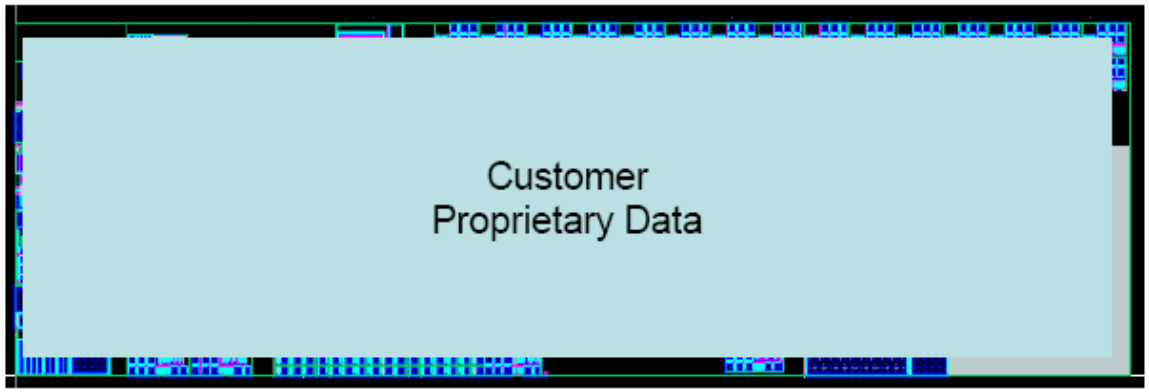
Customer Design



- PLL, 3193 devices
- Major foundry 90nm
- 4 levels of hierarchy, 38 subcircuits

- Total time netlist-to-good placement = 16 hours
  - Run times
    - Full PLL – 15 min
    - Subcircuits – seconds
  - 60-80 total placement runs
    - 1-3 runs on each leaf-level subcircuit
    - 3-5 runs at mid-levels
    - 2-4 runs on full design

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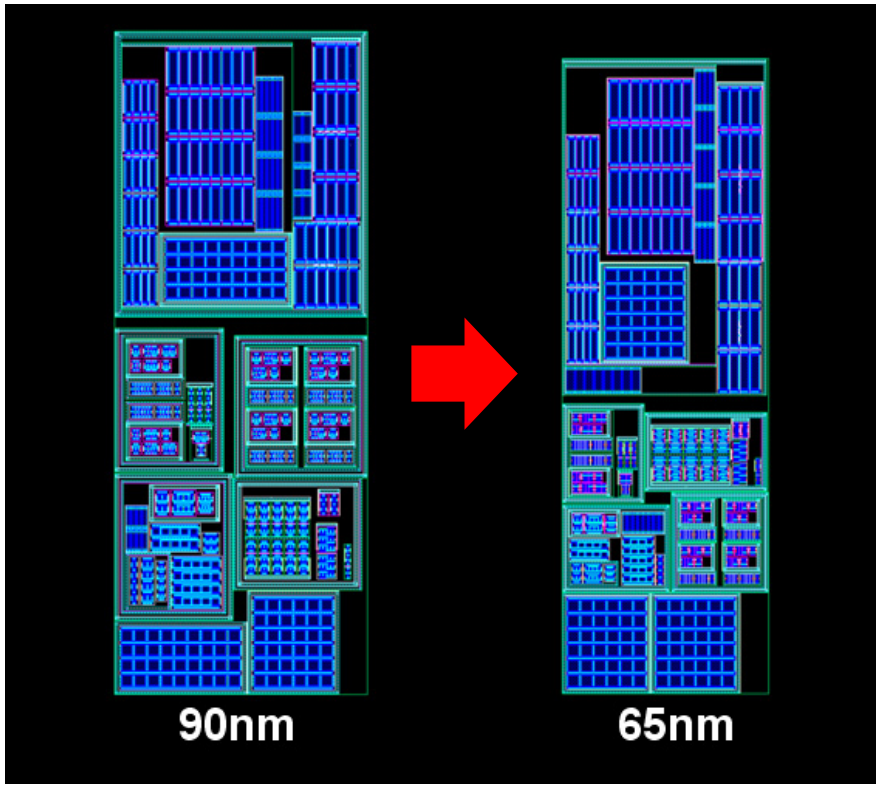
Analog/Mixed-Signal IP Re-Use



Analog/MS IP Reuse in New Technology

- **Same constraints**
- **Same netlist**
  - **active devices resized if necessary; by hand or possibly by a circuit optimizer**
  - **At least one of our SoC customers is designing circuits to work at multiple process nodes w/o resizing … trades off some die area for TTM**
- **New tech file**
- **Same PyCells w/ new tech file**

Not a geometric shrink, but a full re-layout of the same circuit, optimized for new design rules

(ie the same way a layout team would do it!)

→ Port takes 1 iteration, not 50!

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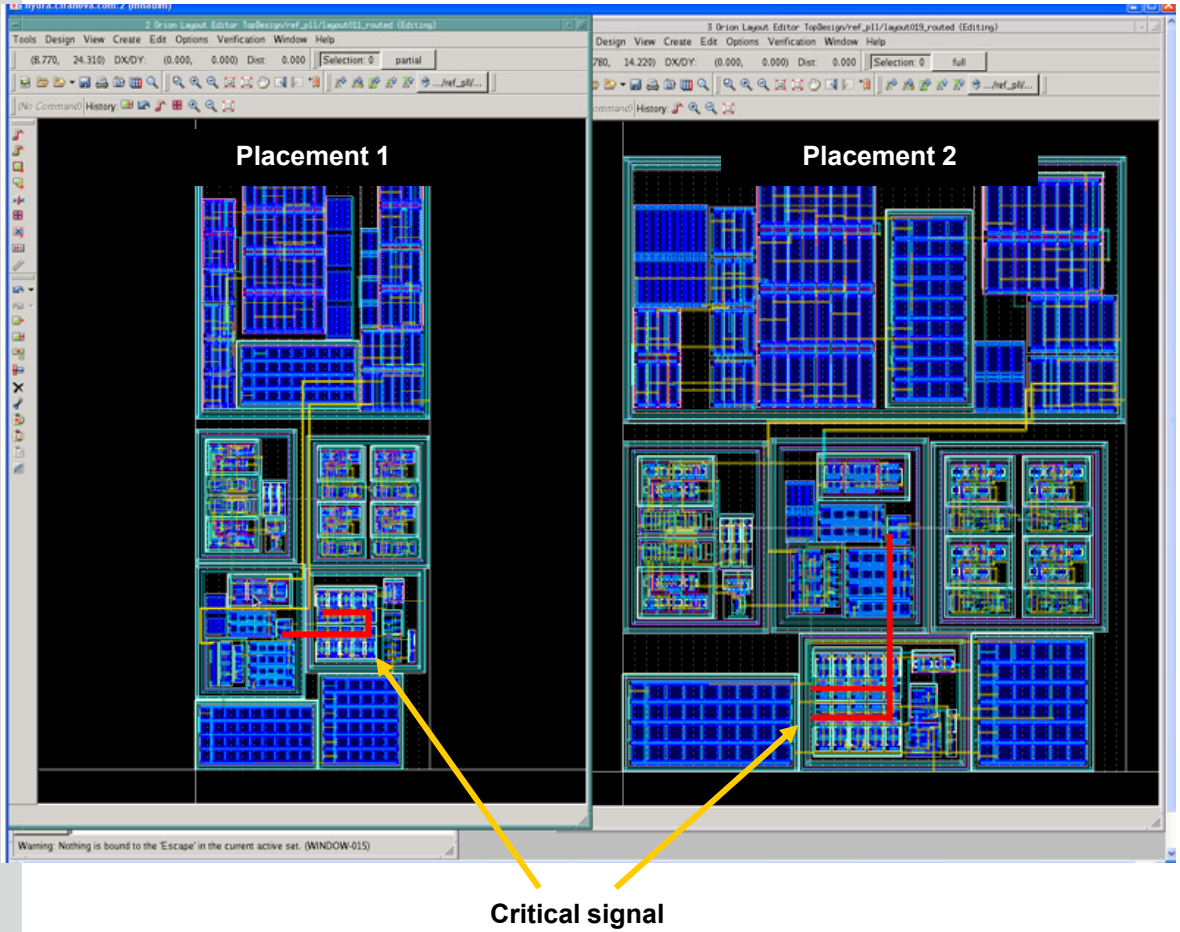
Trial Routing



- Routing is complicated!
  - But less important than placement
- "Trial" route – first-pass interconnect
  - Layout parasitics
  - Routability
  - Not enough experience yet

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Experiences with Users

- Capacity is important – 20,000+ devices
- Routability hasn't been a practical issue
- Floorplanning is a big win
- Most power users drop the GUI and hack the constraint file
  - Still need the GUI for learning (and probably re-learning)
- There is a mental shift
  - "Make all the decisions" vs "make the key decisions and let the computer do the rest"
- Golden netlist often isn't; golden PDK's often aren't
- It doesn't take much "tool overhead" to make a big difference in designer enthusiasm
- Resist the temptation to add new constraint classes

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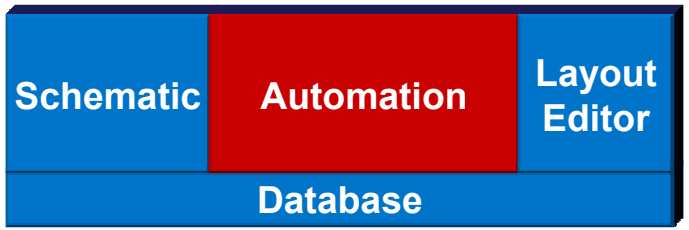
Long Live the Revolution

- Tools: automation formula =
  - Very good QoR:
    1. Circuit level – assist designer; use model critical
    2. Device level – automate
    3. DRC correct – automate
  - Low setup effort, low iteration effort, very high speed and capacity
  - Solve both device (PDK) and circuit levels concurrently

- Market
  - Integration of mixed-signal content into nanometer CMOS SoC's

- EDA revolution
  - PDK's – now
  - Layout – now ?



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