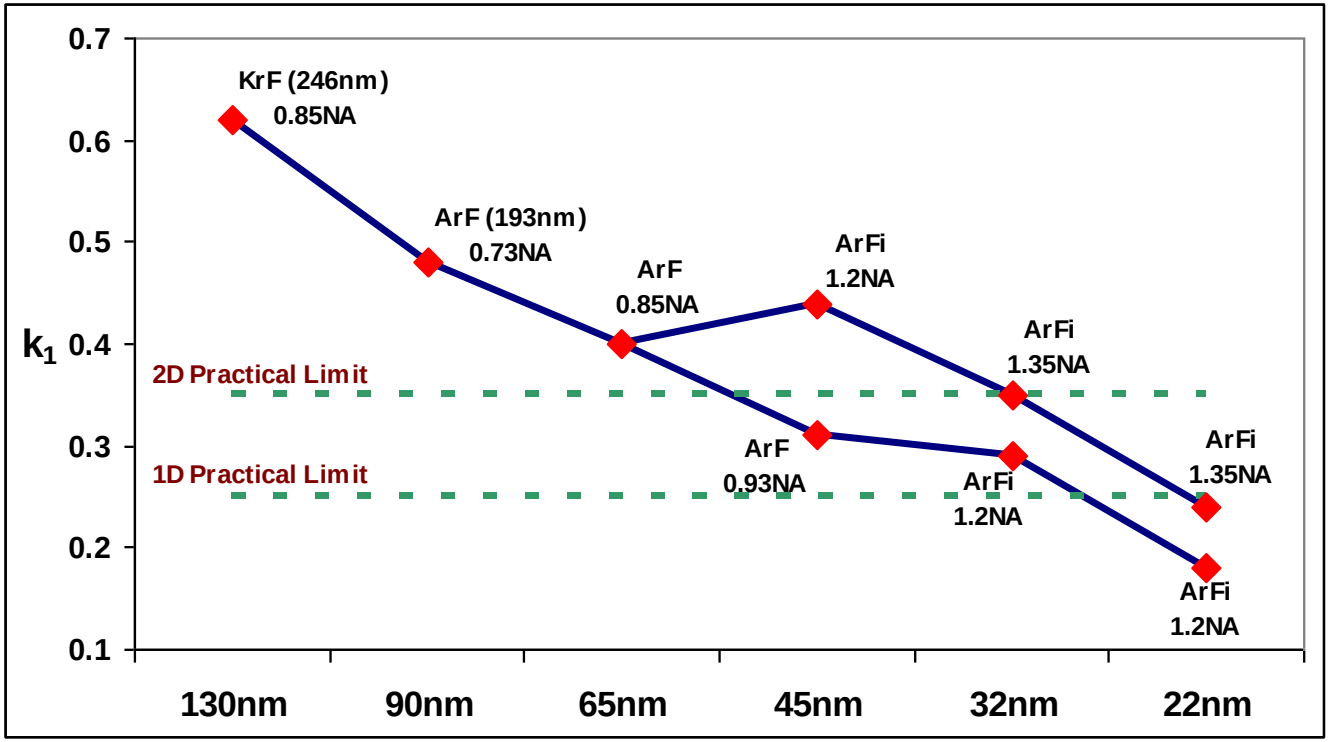
Restrictive Design Rules and Their Impact on 22nm Design & Physical Verification

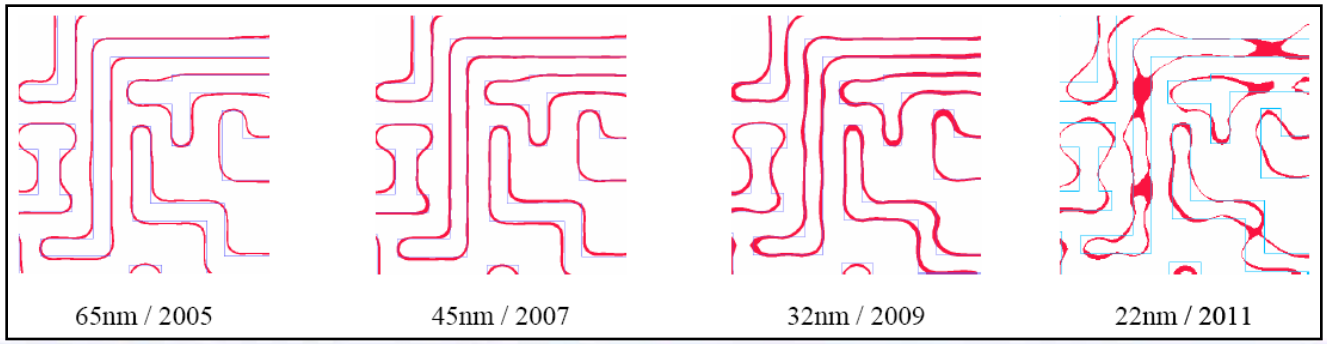
David Abercrombie – Mentor Graphics
Praveen Elakkumanan – IBM
Lars Liebmann - IBM

Outline

- Introduction
- Restricted Design
- Basics of Gridding
- Checking Implementation
  - Grid Checking
  - Pitch Checking
- Summary

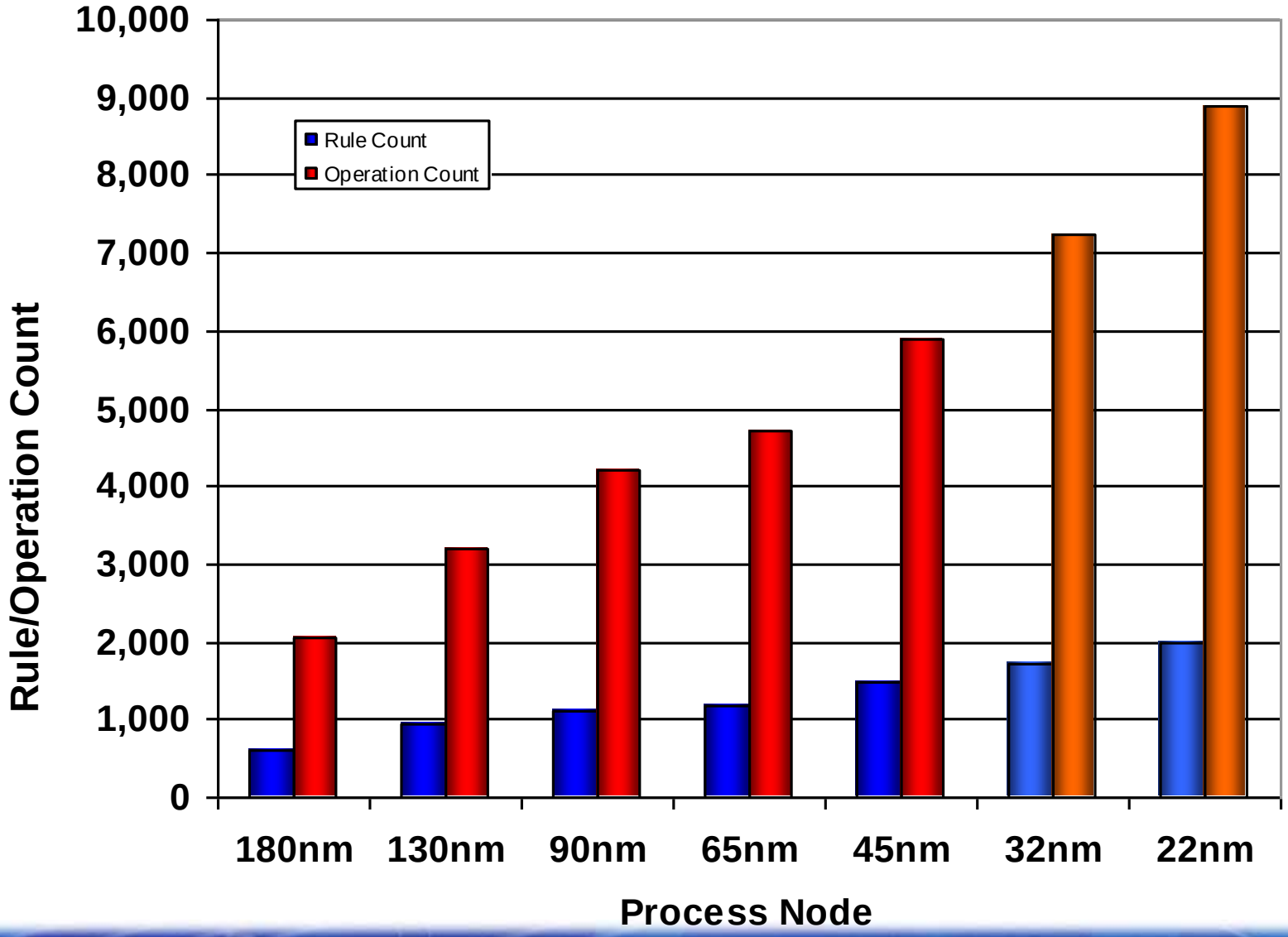
The 22nm Litho Challenge



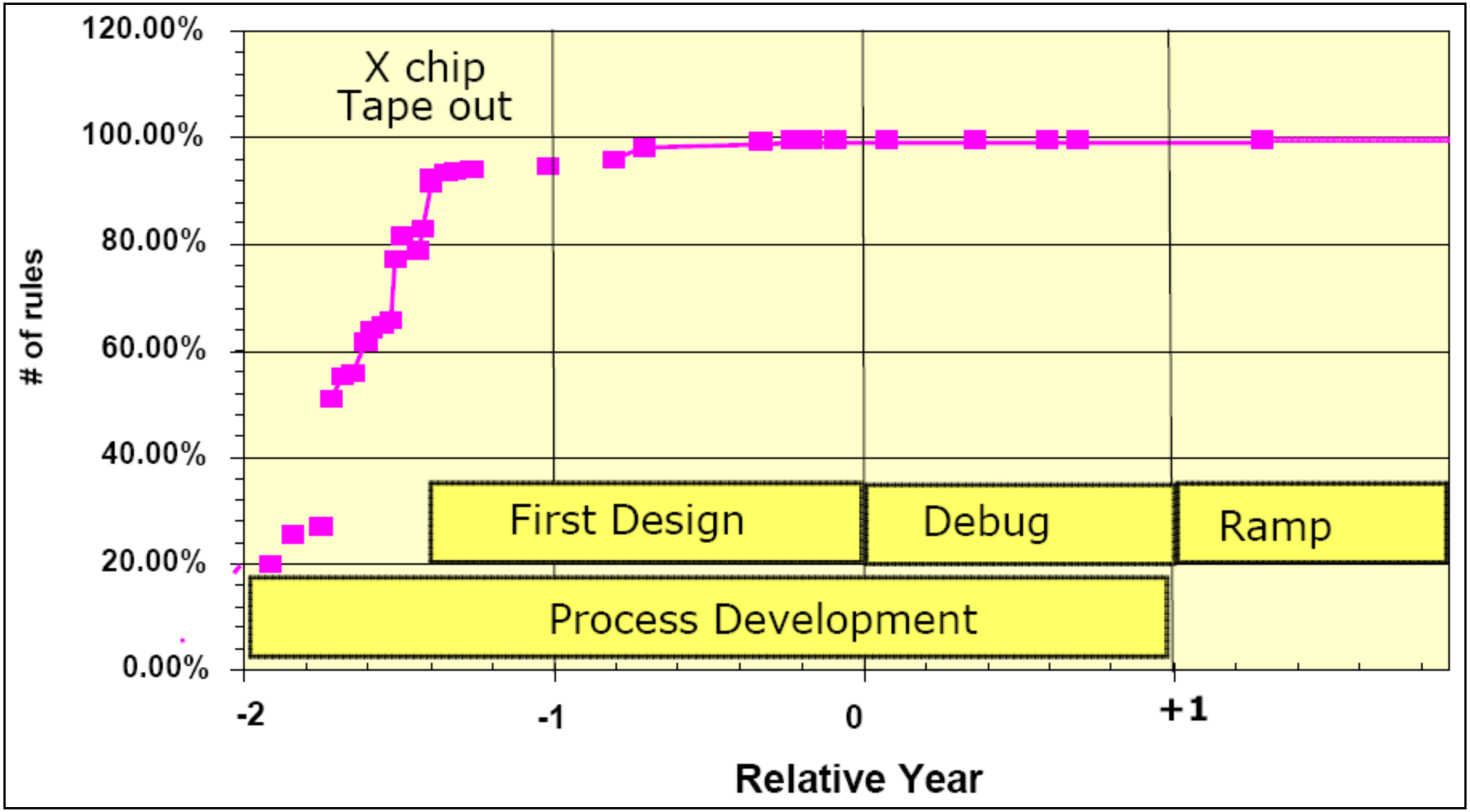


"Lithography for the 32nm Technology Node," W. Arnold, 2006 IEDM 32nm Technology Short Course
"DfM, the teenage years". Lars Liebmann, Proc. SPIE Vol. 6925, 692502 (Mar. 4, 2008)

Design Rule Count & Complexity

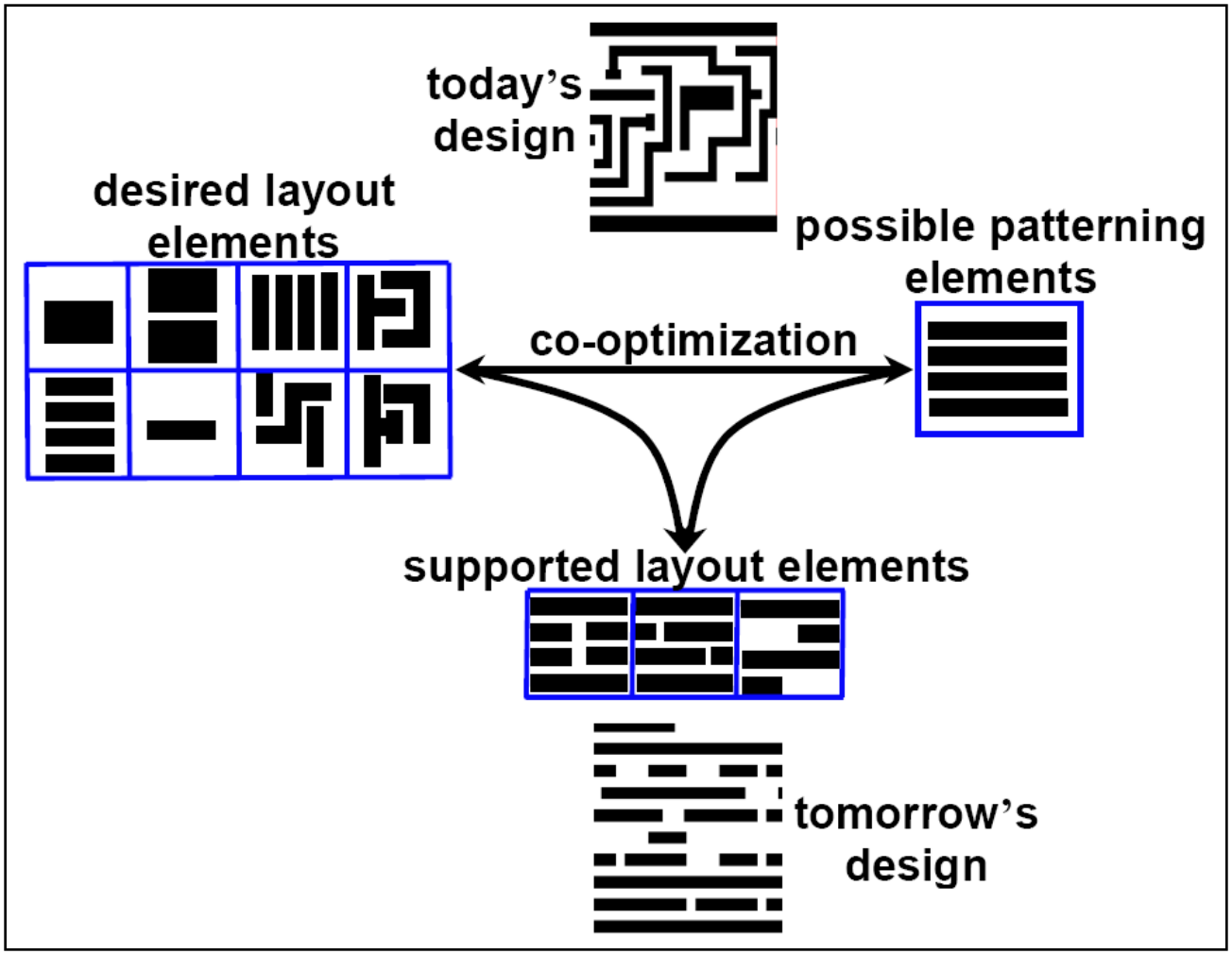


Design Rule Development Lag



"Intel design for manufacturing and evolution of design rules". Clair Webb, Proc. SPIE Vol. 6925, 692503 (Mar. 12, 2008)

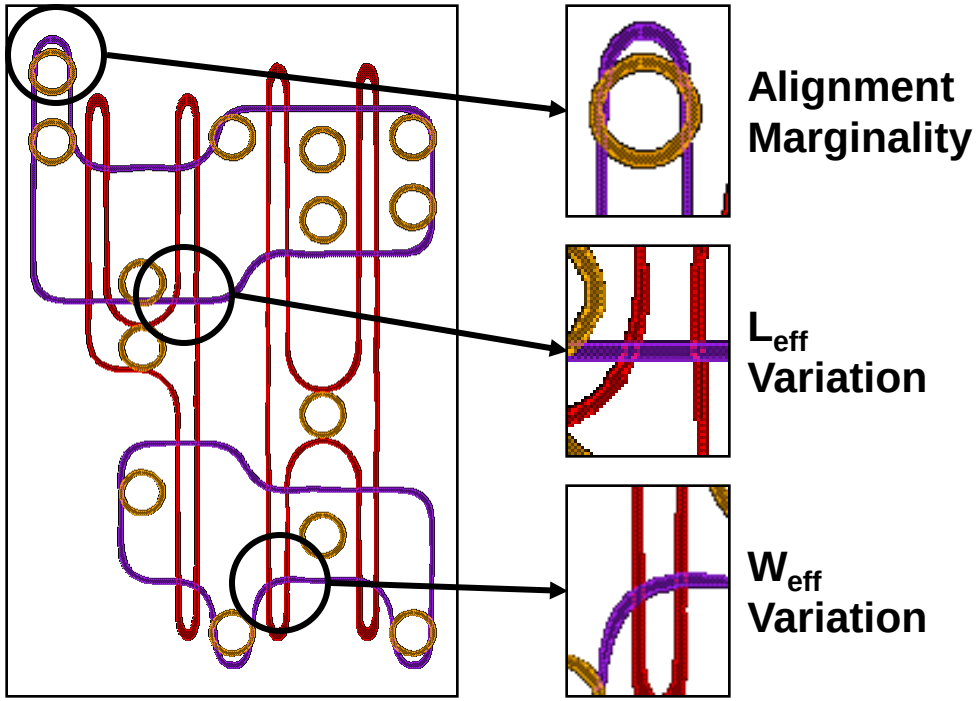
Simplifying the Problem with Restricted Layout



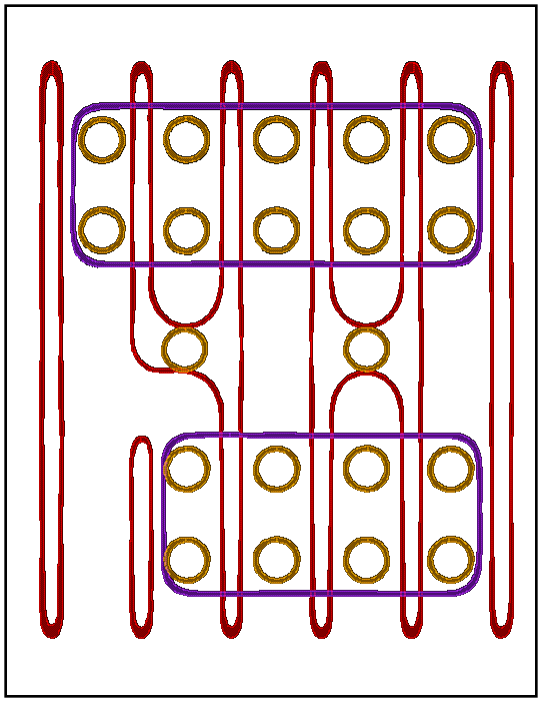
"DfM, the teenage years". Lars Liebmann, Proc. SPIE Vol. 6925, 692502 (Mar. 4, 2008)

Restrictive Design Benefits

Traditional Design Rule Based Cell



Restrictive Design Rule Based Cell



- **Maximizes Design Flexibility**
- **Increases Performance Variability**

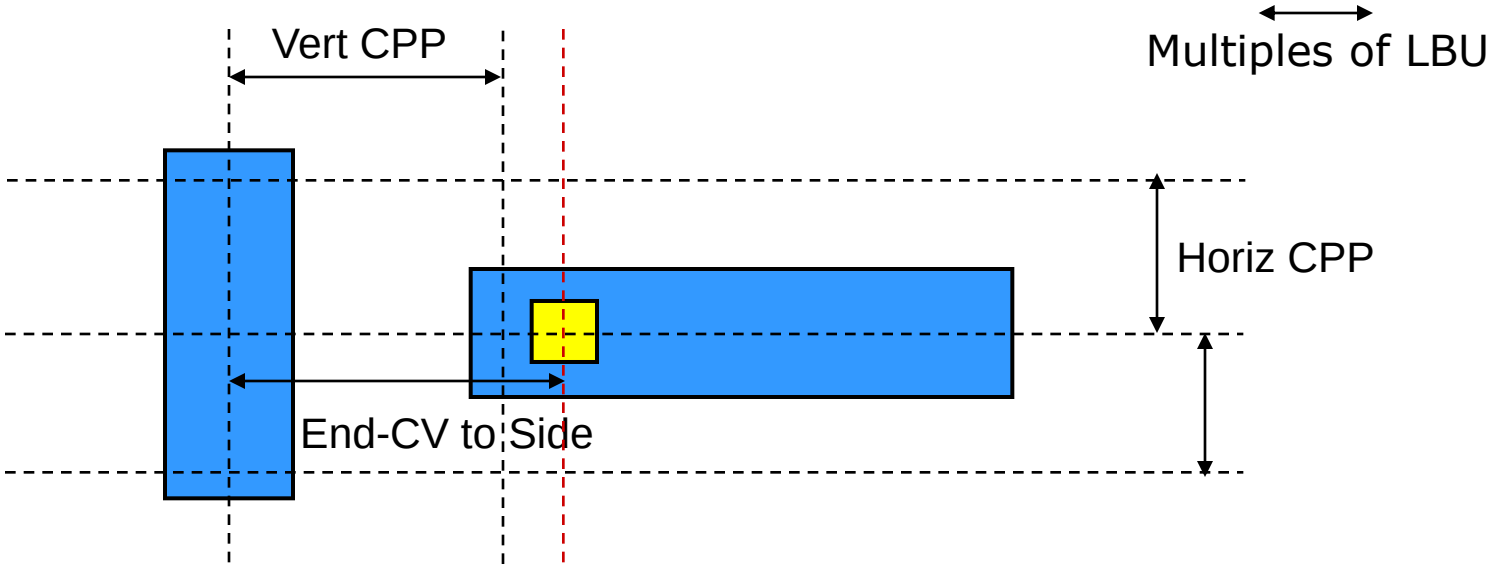
- **Decreases Performance Variability**
- **Minimizes Design Flexibility**

Basics of Gridding

- Three basic layout objects
  - Line Objects (polysilicon, metal)
  - Point Objects (contacts, vias)
  - Block Objects (diffusions, implants)
- The vertices of all layout objects lay on a grid called the Layout Base Unit (LBU) grid
- The anchors of all shapes lie on a coarser grid called the placement grid
  - Center lines, center points, edges, etc.

Placement Grids and LBUs

- Layout Base Unit (LBU) could be some arbitrary unit.
- Contacted poly pitch (CPP), wire pitches and placement grids are multiples of LBU
- Coarser the LBU => a lower number of design configurations are better for retargeting and manufacturability but not so good for density.

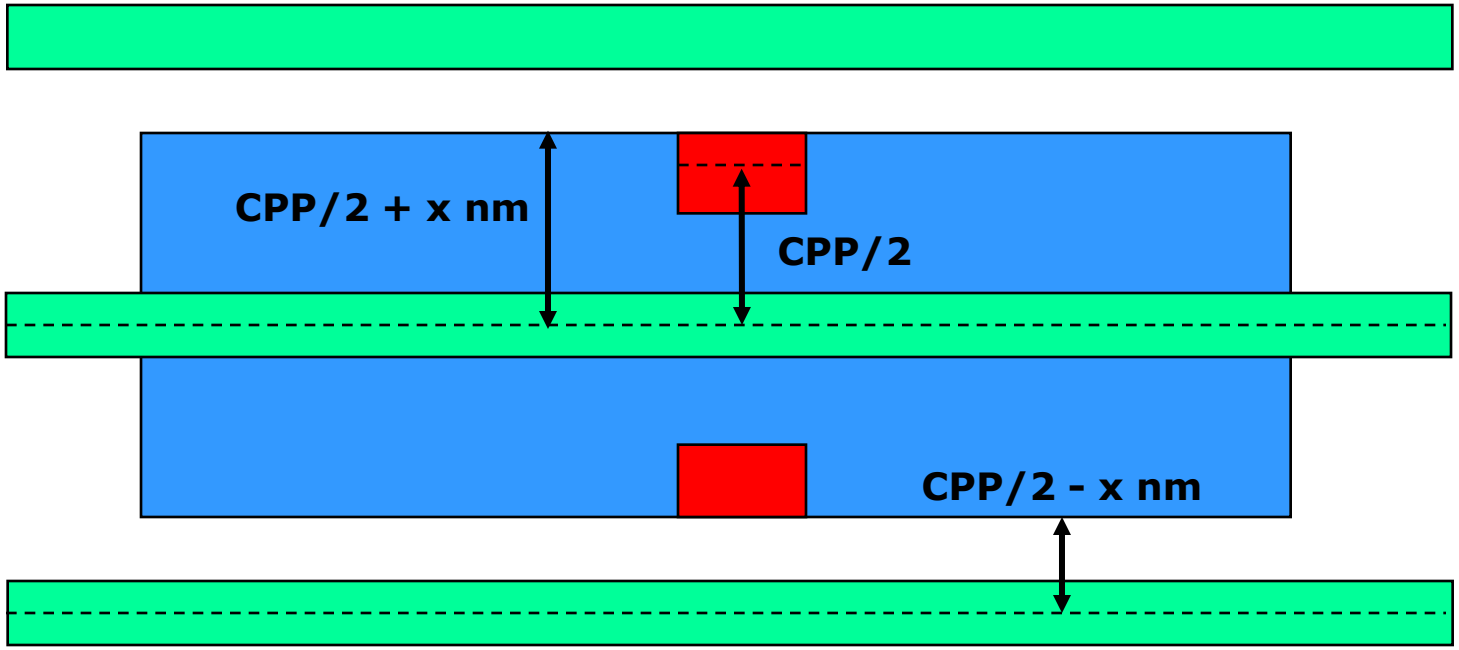


Grid Definitions – More Details

- Each layer has a set of X and Y grids that are legal
  - PC x-grid – centerlines 0, CPP, 2*CPP, 3*CPP etc
  - M1 x-grid – centerlines 0, CPP/2, CPP, 3/2 * CPP etc
- Placement periodicity is only a part of grid definition
- Each layer has a set of valid offsets or sub-grids as well
- General form for grid definition

  <level>:<D>= O1 [O2, O3…] + PG * n, where
  - <level is the level for the grid
  - <D> is the orientation (direction) for the grid
  - n is an integer
  - O1 is the normalized offset with respect to a global origin & O2, O3.. are optional additional offsets (sub-grids)

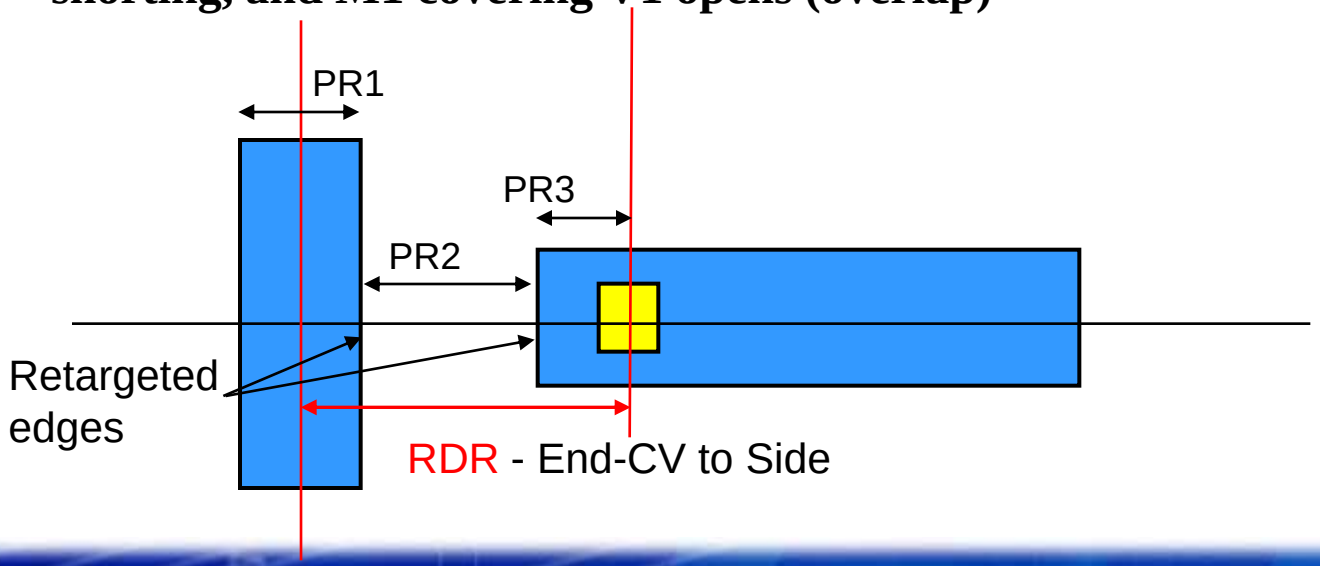
Grid Example



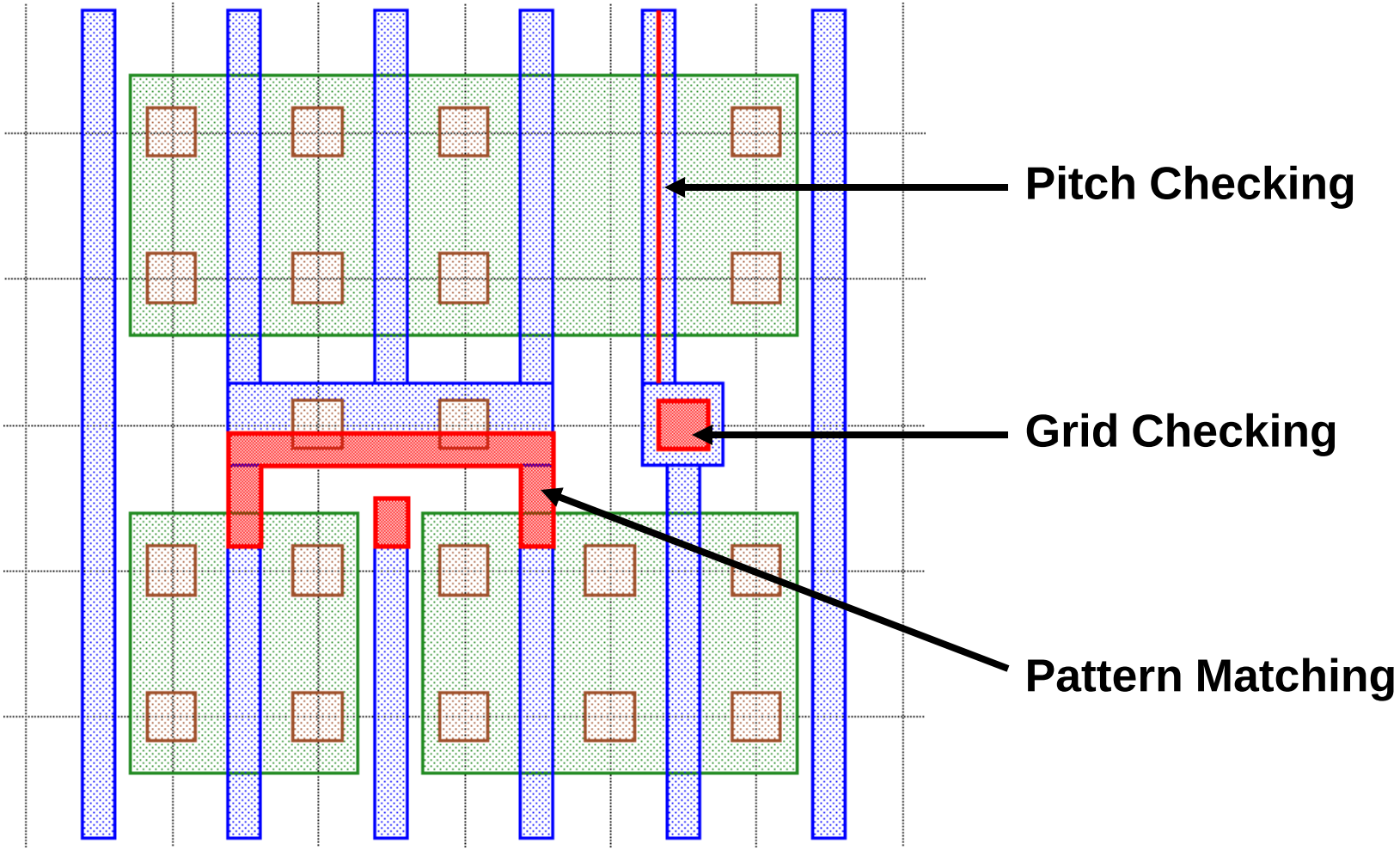
- Top and bottom edges of RX have two different offsets (CPP±x) but the same placement grid (CPP); x=half contact size
- CA on active has a single offset of CPP/2 and placement grid of CPP
- Diffusion grid definition: (-CPP/2-x, CPP/2+x) + CPP*n where global origin is in the center of a PC

Anatomy of an RDR Configuration

- RDR based design leaves some edges only roughly specified, with retargeting setting the exact edge positions
- Valid minimum for RDR determined by looking at process restrictions PR1/2/3, and as necessary each in the specific context
  - Typically, two or more PRs may define a single RDR (many to one relationship)
- Balance between competing limitations is used to set the retargeting. In this case the 3 effects are necking of the vertical M1, M1 tip-to-line shorting, and M1 covering V1 opens (overlap)

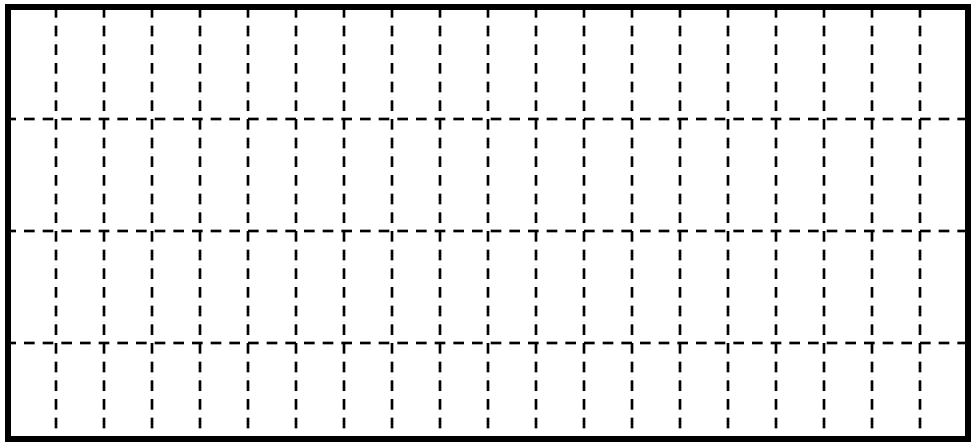


Physical Verification Needs for RDR



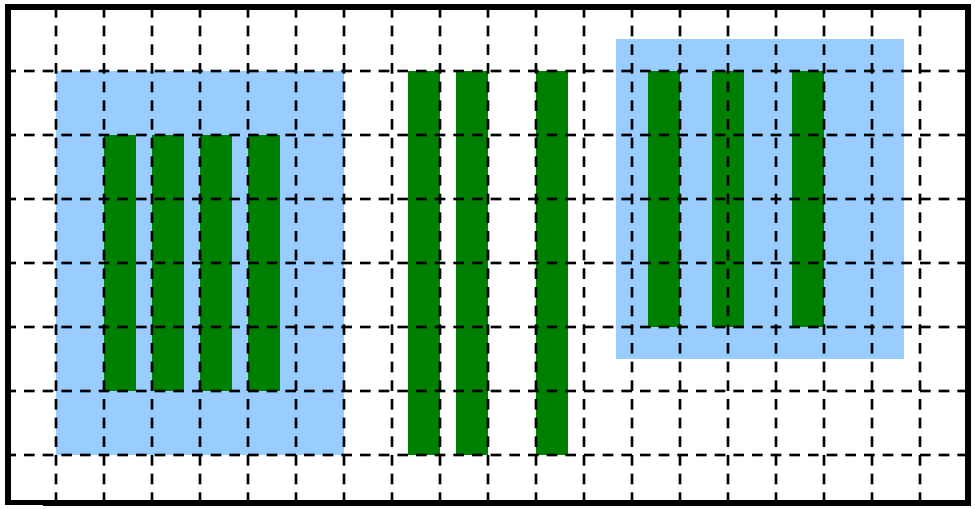
Grid Definition PV Requirements

- Set of “invisible” lines that define locations of proper alignment in X and/or Y orientation
- Grids do not have to be defined or the same in each orientation
- Grids do not have to be the same per layer or check but may relate to one another intentionally

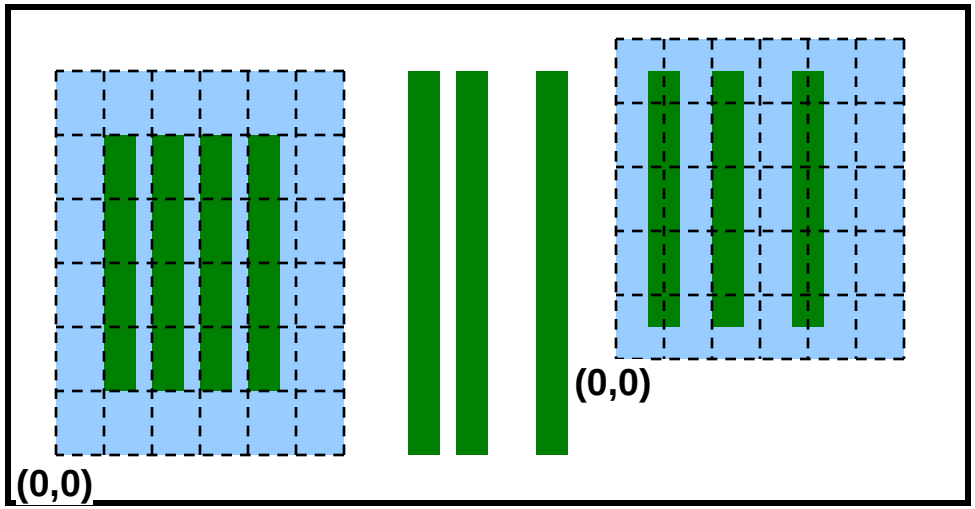


Grid Definition - Origin

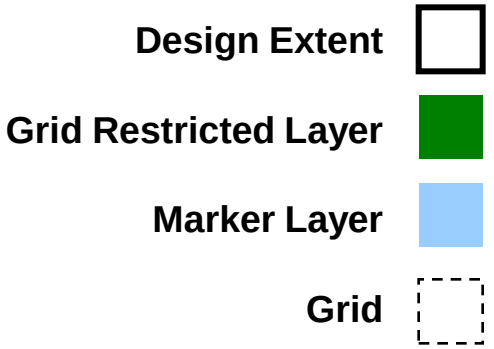
Chip Extent Grid Origin



Marker Layer Grid Origin



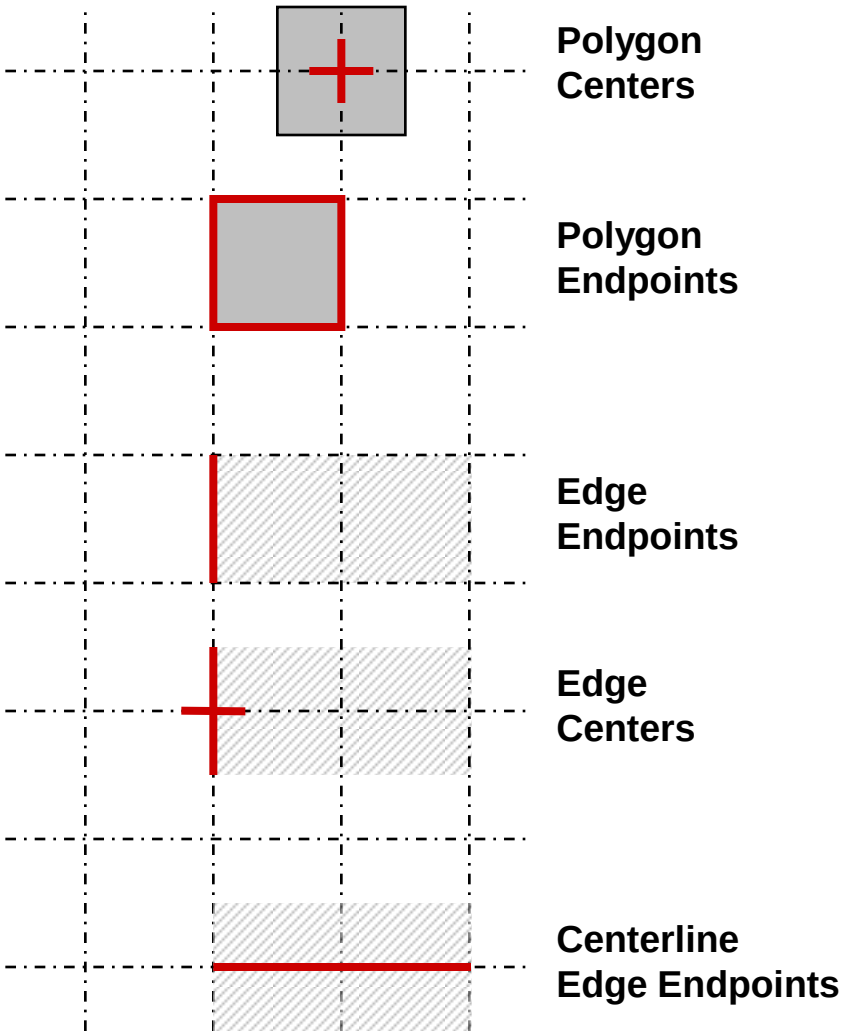
Grid origins can be defined in relation to the design extent or to shapes in a specified layer (ex. Marker layer)



Grid Definition – Feature of Interest

The grid restriction can be applied to various layout feature elements including:

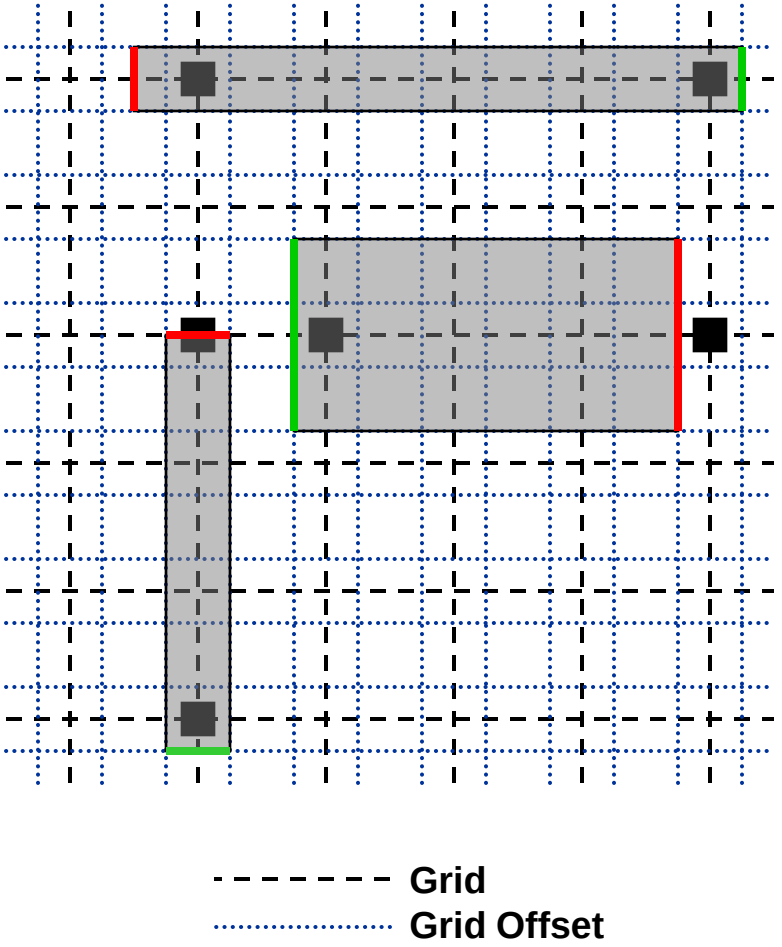
- **Polygon Centers**
- **Polygon Endpoints**
- **Edge Endpoints**
- **Edge Centers**
- **Centerline Edge Endpoints**



Grid Definition - Offsets

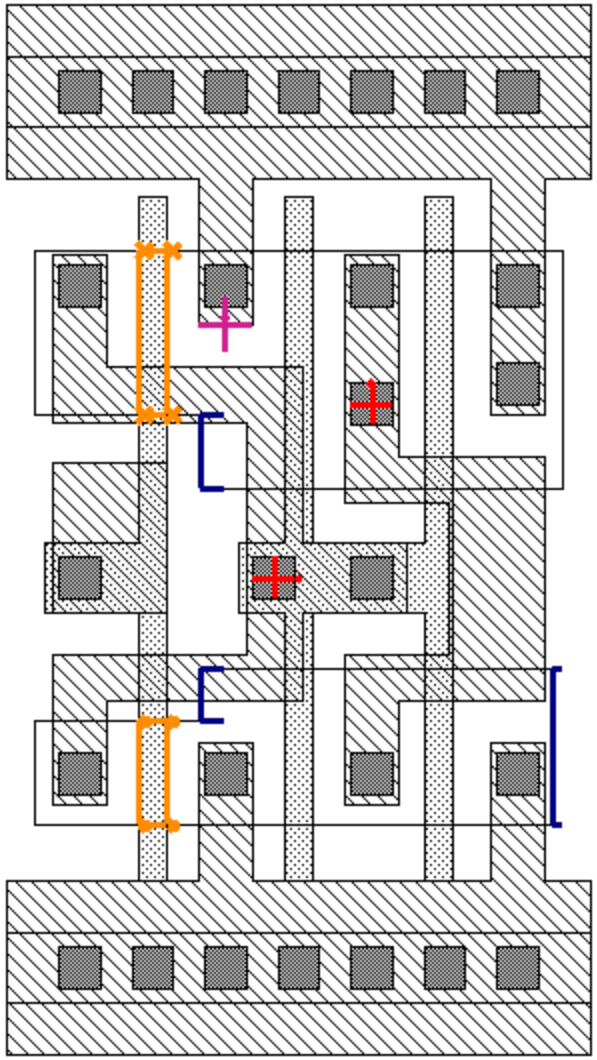
Offsets to the grid may be defined to specify how shapes should extend beyond, remain short of or enclose the primary grid

- **For example: metal lines should extend beyond the via grid by x or y offset**



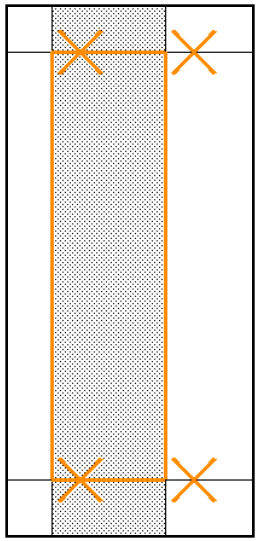
Example Grid Checks

- All contact center points must be on the specified x-y grid
- All gate vertices must be on the specified x-grid
- Gate facing active edges that enclose contacts must be offset to the contact grid else they must align with contact grid
- M1 line ends must extend beyond the contact by a specified offset to the contact grid

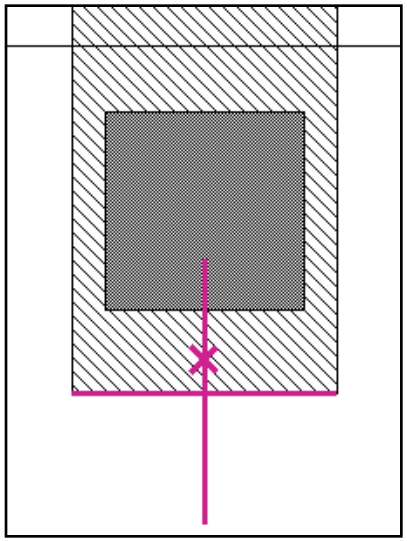


Hint Marker Guided Off Grid Correction

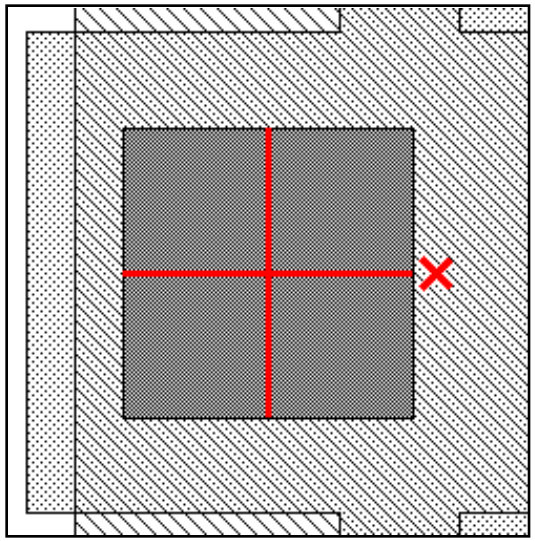
Fixing off-grid errors can be challenging because the grid is not visible to the designer and the definition of the grid can be complex. Hints to show the nearest allowed grid point location as shown here can be very helpful in debugging grid misalignment errors



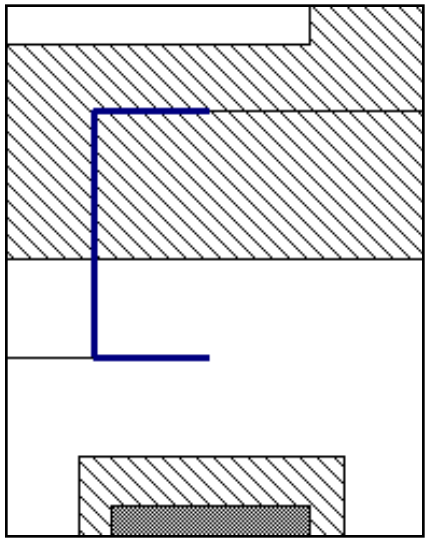
Polygon Vertex Grid Alignment Hint



Edge Center Point Grid Alignment Hint

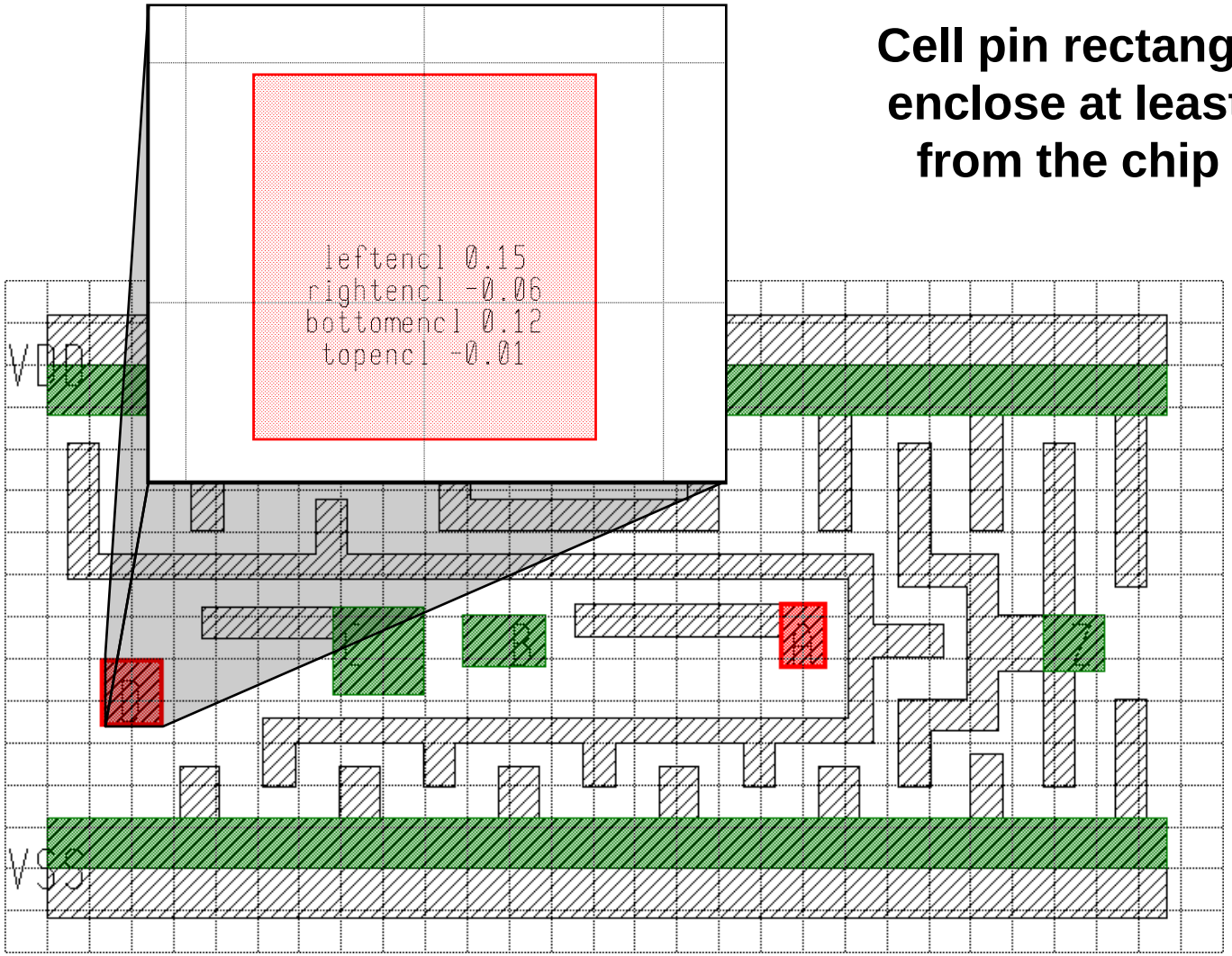


Contact Center Point Grid Alignment Hint



Edge Vertex Grid Alignment Hint

Example Older Technology Grid Check



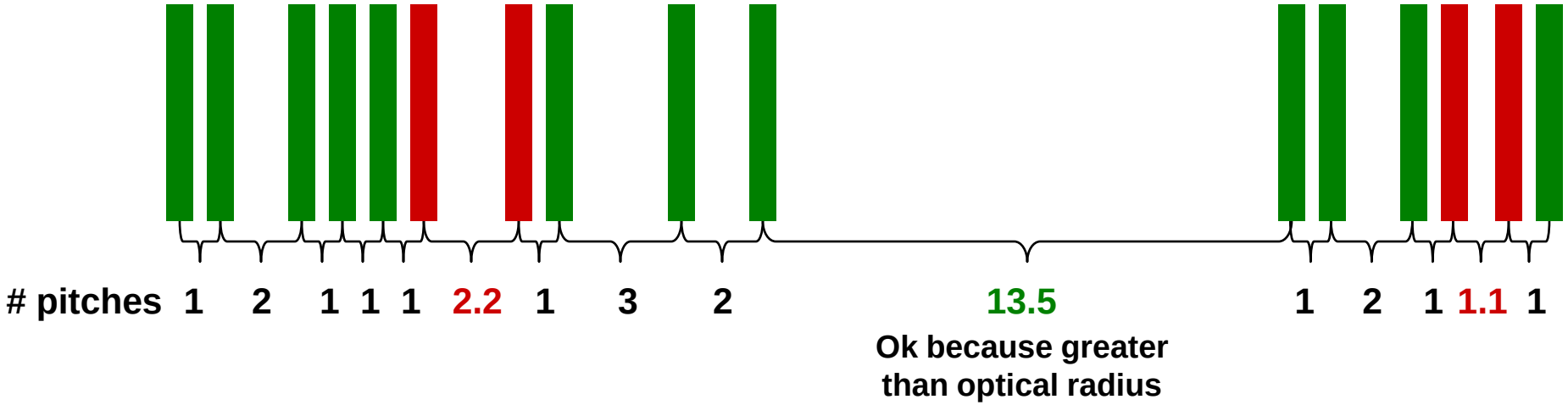
Cell pin rectangles must fully enclose at least one full grid from the chip routing grid

The grid would be invisible on the actual layout database *(it is shown here for clarity).*

The property calculations provide a hint about how far to extend polygons edges to meet the enclosure criteria.

Relative Pitch Definition

Pitch = space + width = x *(for example)*
Optical radius = influence distance of reflected light = 10x *(for example)*
Features must be placed on a even number of pitches *(no partial pitch)*

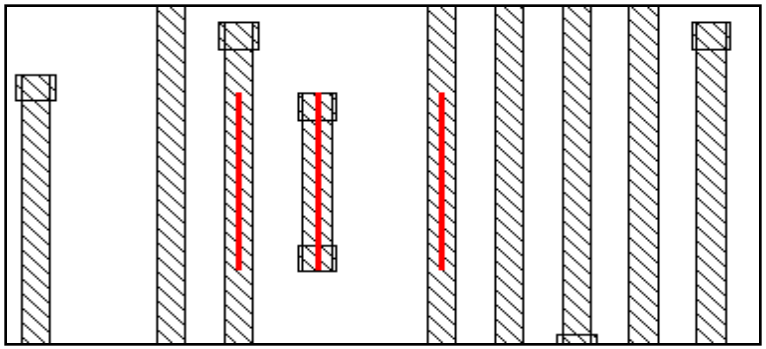


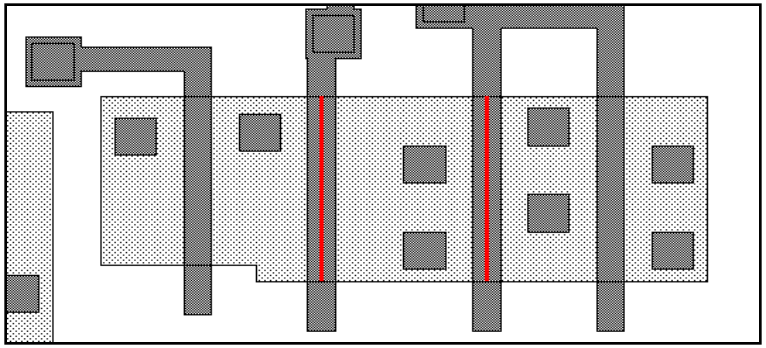
Implications:

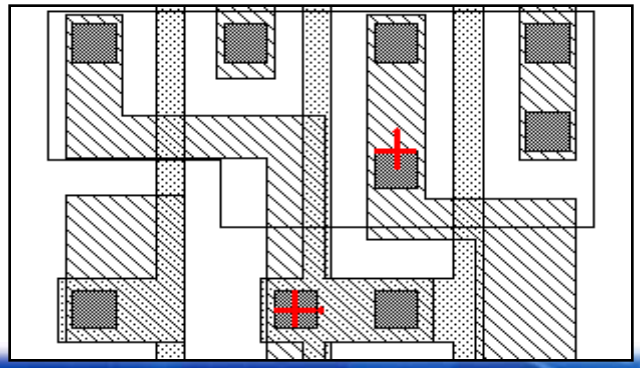
- **Features are considered grouped if they are within an optical radius distance**
- **Features within a group are restricted in relation to each other**
- **Separate groups of features are not restricted relative to one another**

Example Pitch Checks

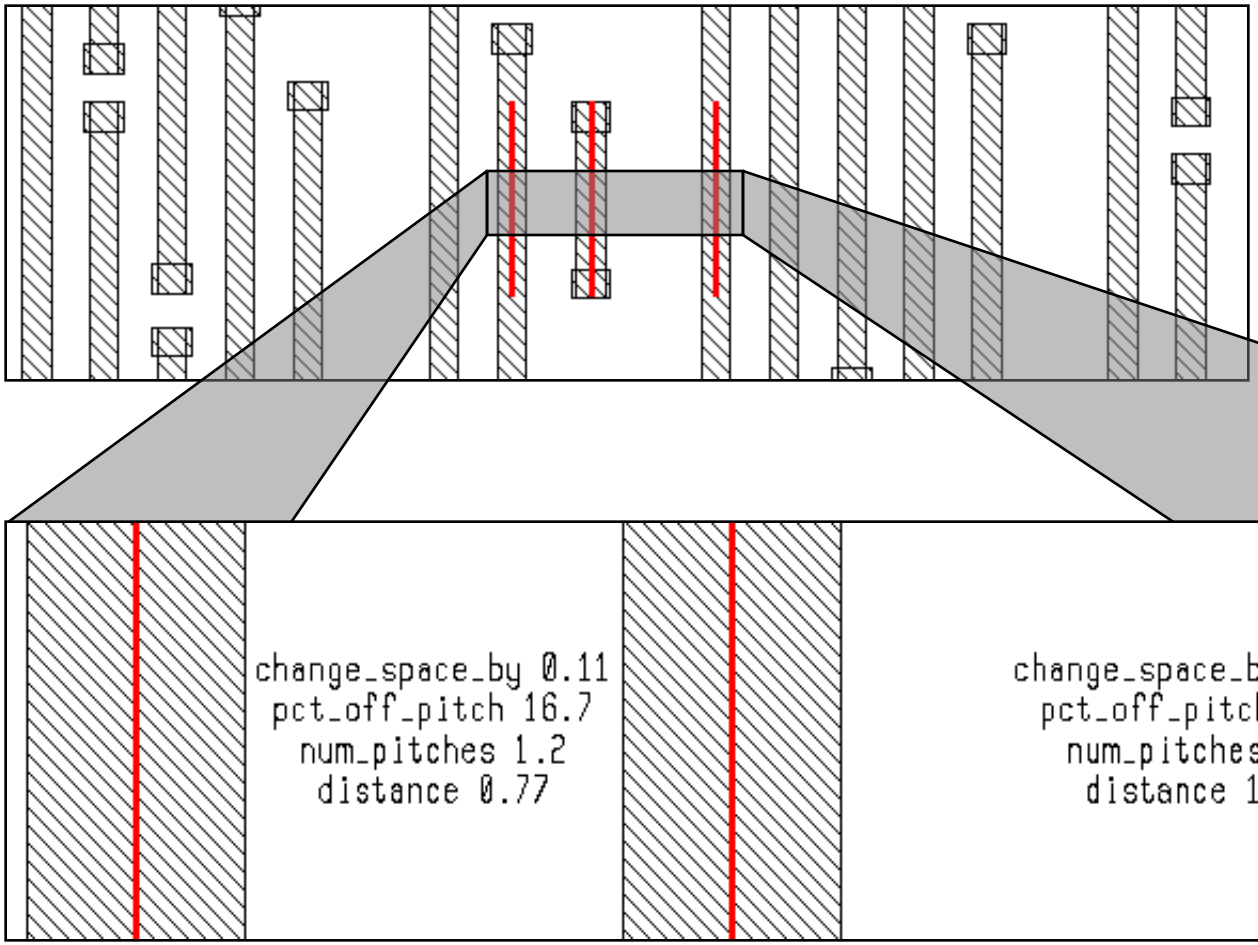
- Metal routing wires must be on specified relative pitch within an optical radius
- All gates within the same active must be on specified relative pitch
- All contacts must be on a specified relative pitch







Hint Property Guided Pitch Correction

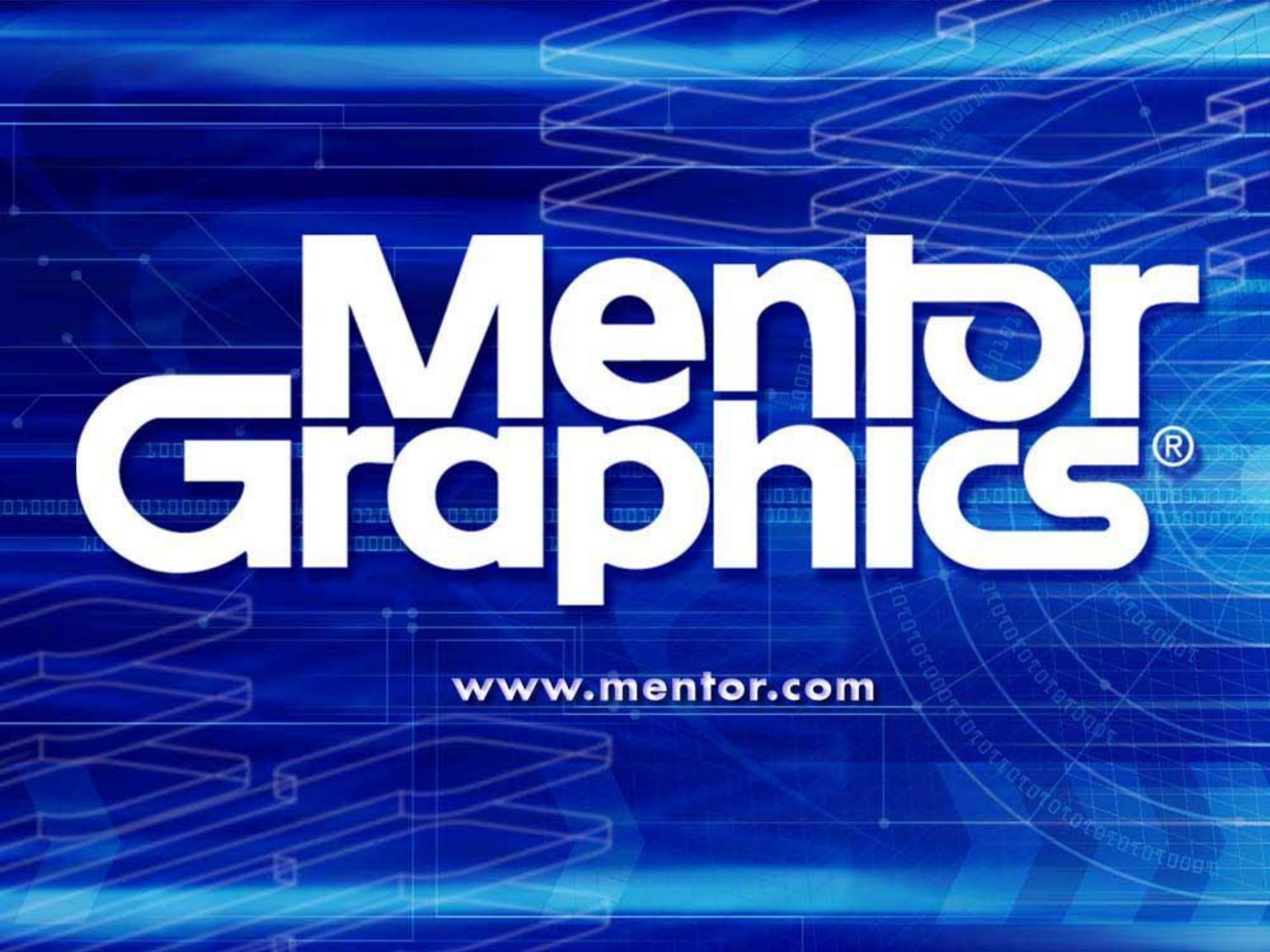


Fixing pitch errors can be challenging because the pitch is not visible to the designer and must be mathematically determined

Hints to show how much the shape should be moved as shown here can be very helpful

Summary

- Some form of restricted design rule methodology is likely for 22nm processes and below
- Restricted design requires the definition and physical verification of grid and pitch constructs
- Advances in DRC tool capabilities to define grids, offsets and calculate mathematical pitches are required to properly specify and check these RDR constructs
- Various forms of “hinting” are necessary for the designer to efficiently fix grid and pitch violations


Mentor Graphics®
www.mentor.com