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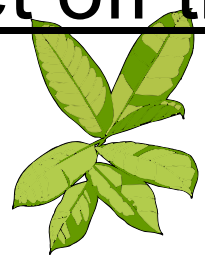
EDP Workshop Panel

Get off the bus, drive a Hybrid!



Invest in green interconnect

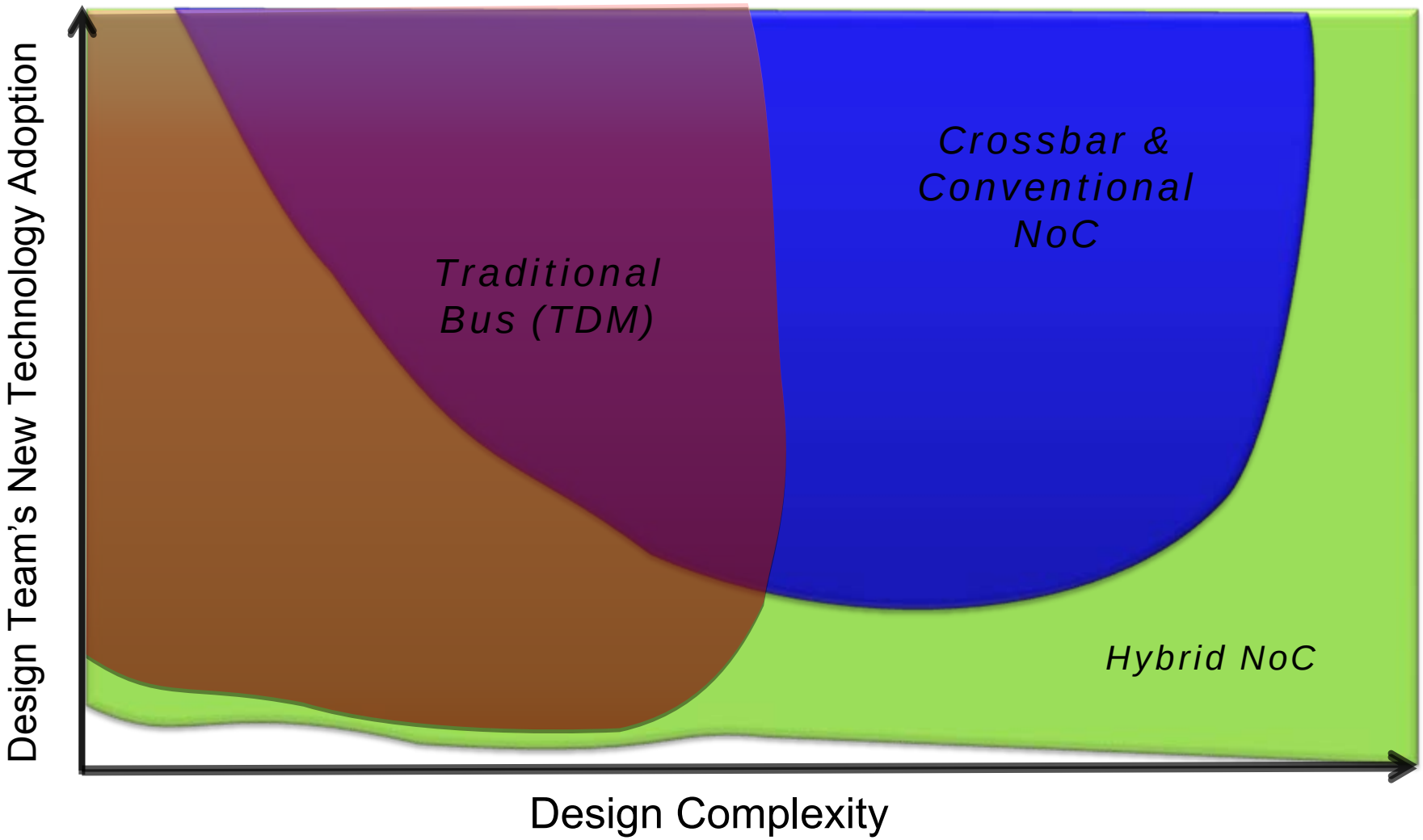
David Fritz (CEO)

April 2009

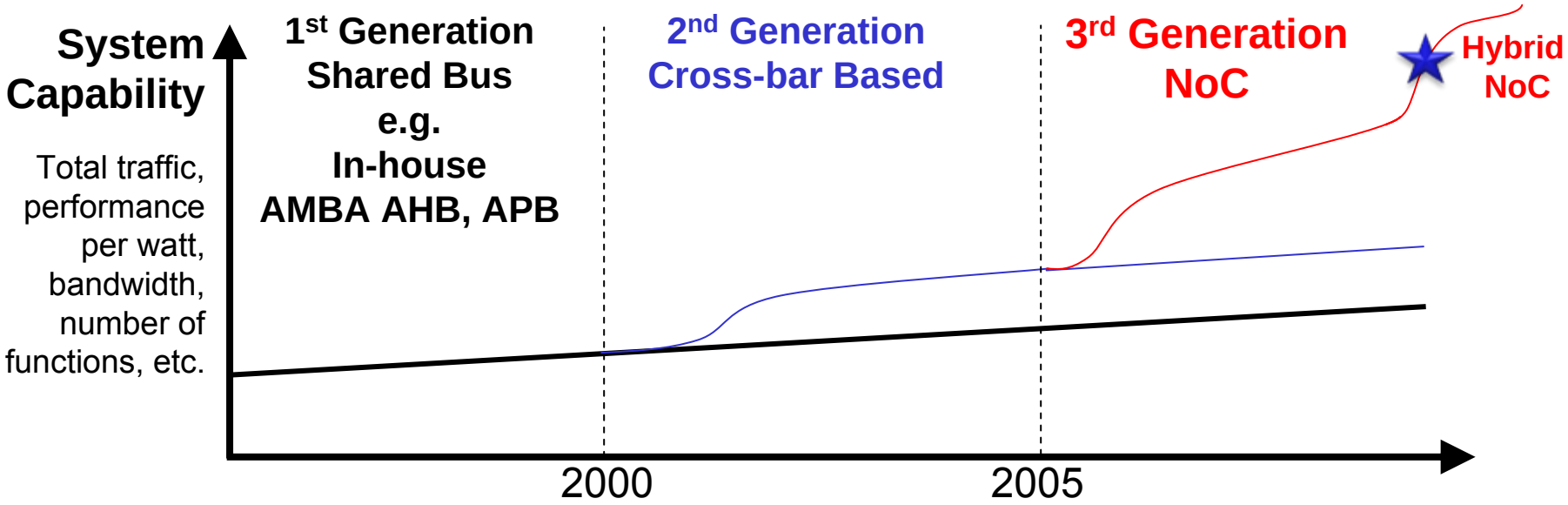
Is interconnect broken?

- Short Answer: Yes & No ...
- Traditional bus-based techniques will linger
  - Legacy subsystems will remain intact
  - Must avoid cost of re-verification
- However, a new solution is needed to address
  - Complexity and scalability
  - Power and clock management
  - Process technology physics
  - Timing closure and P&R

Applicability of Interconnect Technologies



On-chip Interconnect Evolution



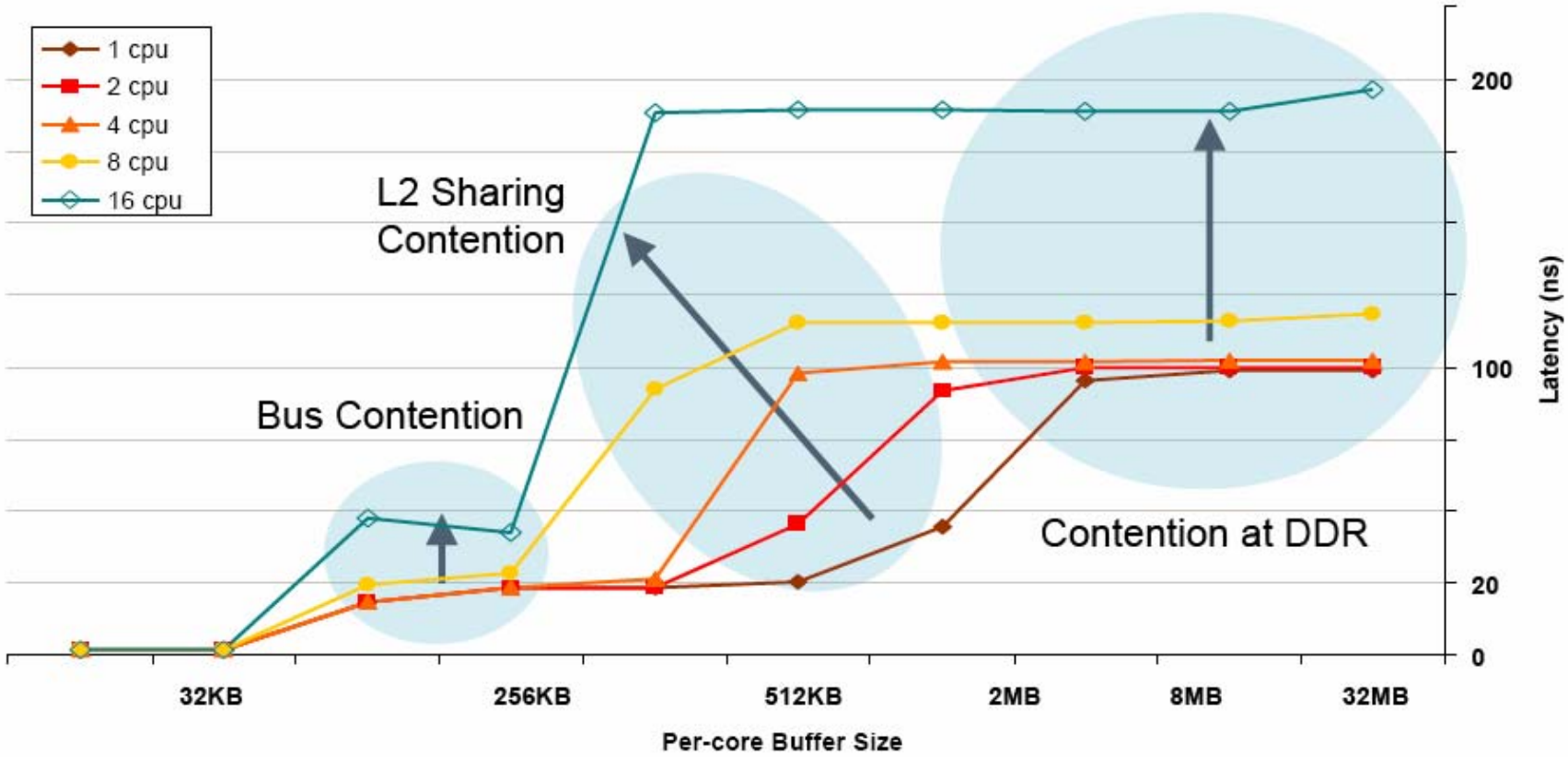
Next Generation Interconnect MUST:

Deliver architectural exploration & synthesis of predictable interconnect from an abstract set of requirements

Solve process variation complexity & timing closure issues through interconnect driven placement & Hybrid NoC technology

Complexity and System-level Scalability

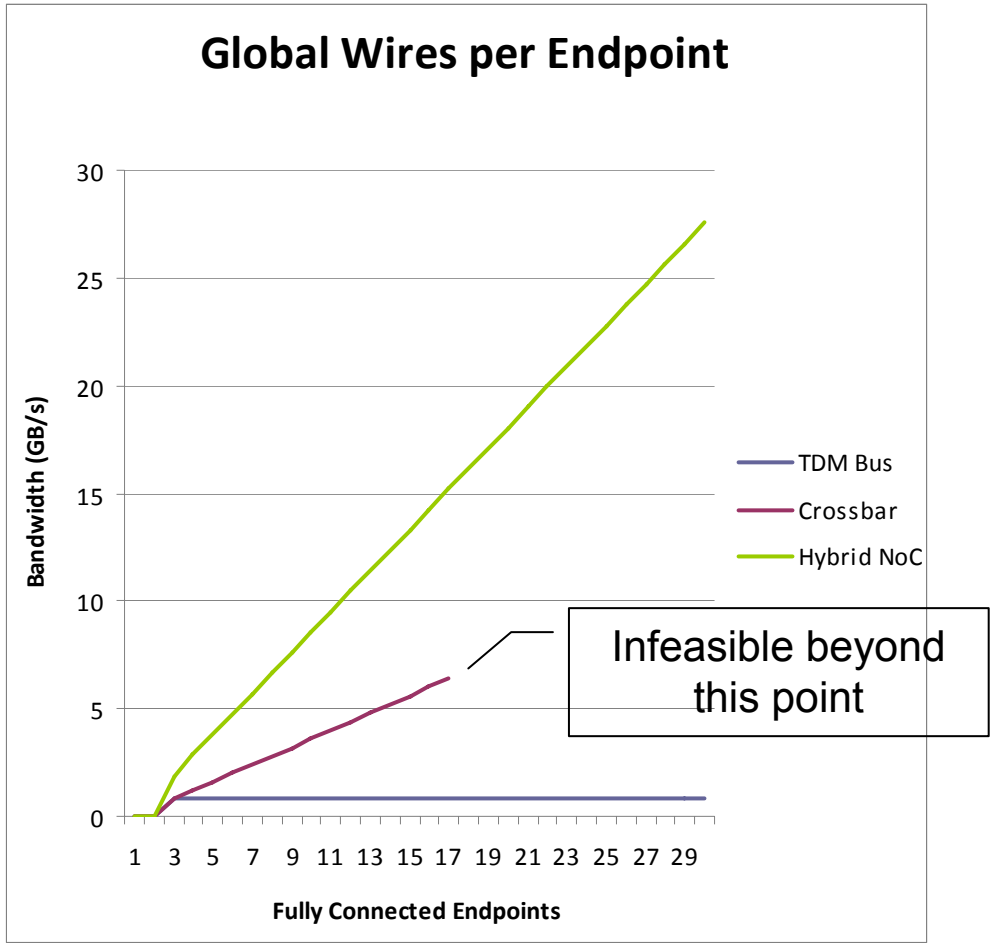
- Shared bus frequency and bandwidths decrease while latencies increase as system complexity increases
- Shared bus interconnect does not scale with number of cores creating a bottleneck



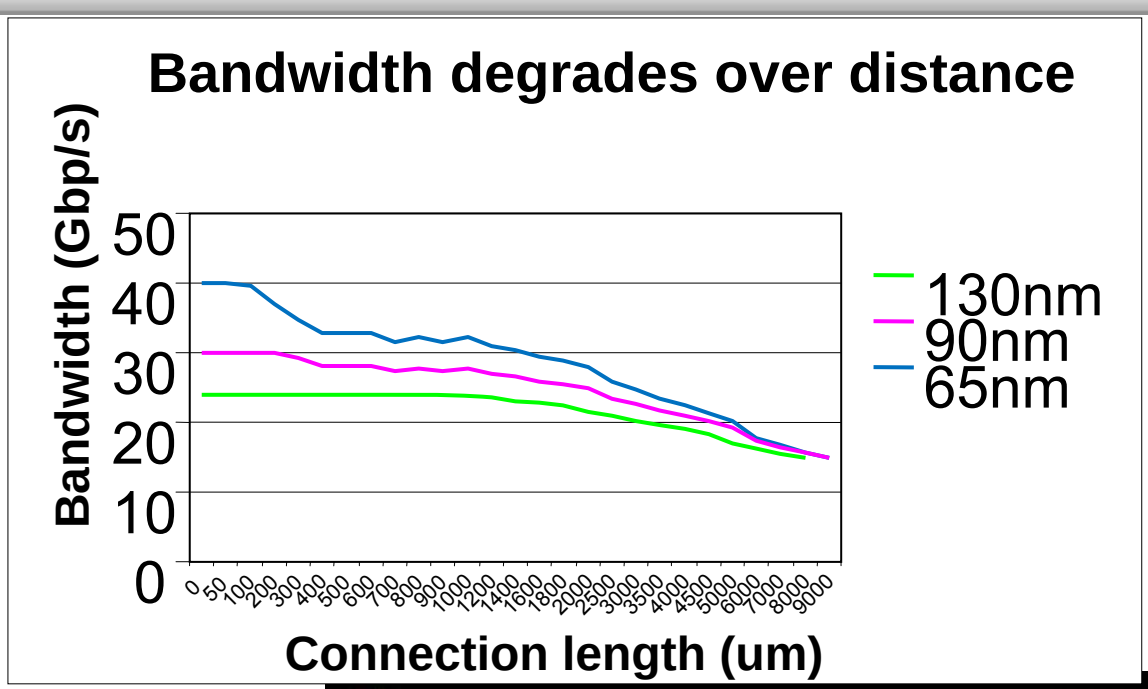
Source: Freescale Semiconductor, 2009

Bandwidth Scalability

- Bus bandwidth is fixed
- Crossbar & NoC bandwidths scale with number of endpoints
- Hybrid NoC delivers better bandwidth per wire and lower latency
  - Clockless links cycle at higher relative rates for global communication
  - Clocked links deliver low latency between localized blocks
- **Bus-only solutions cannot scale**

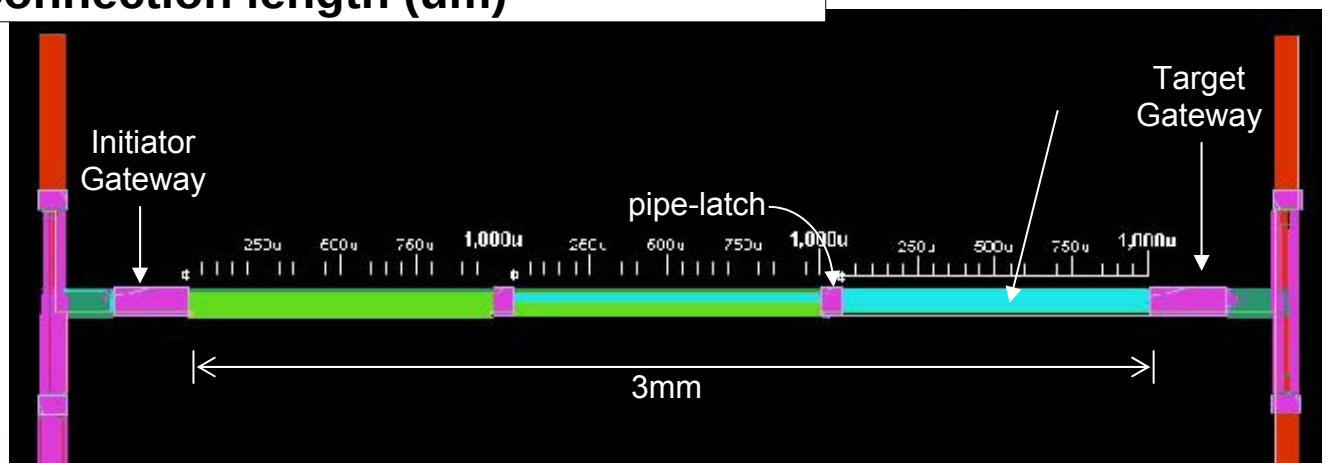


Bandwidth vs Wire Length Conundrum



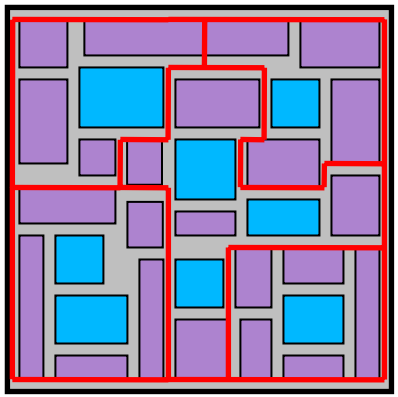
Long distance on-chip communication requires signal amplification that has:

- Near-zero latency cost
- Near-zero area cost
- Resolve global timing closure issues



Complexity and Process Physics

SoC
(Moderate Complexity)

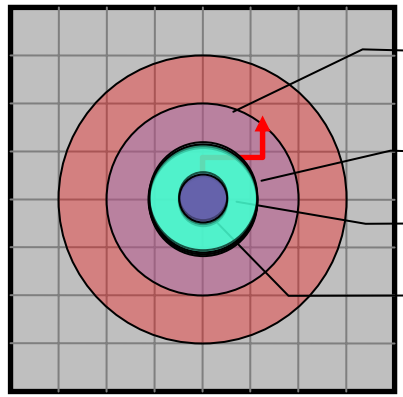


Initiators (8)

Targets (20)

Multiple subsystems communicating concurrently

8mm x 8mm Chip
(500MHz clock)



Wire delays dominate, takes multiple clock cycles to span a chip

Hybrid NoC uniquely solves chip-level and sub-system interconnect issues

Clockless circuit design exhibits a natural tolerance to process variation induced timing closure challenges common at deep sub micron nodes

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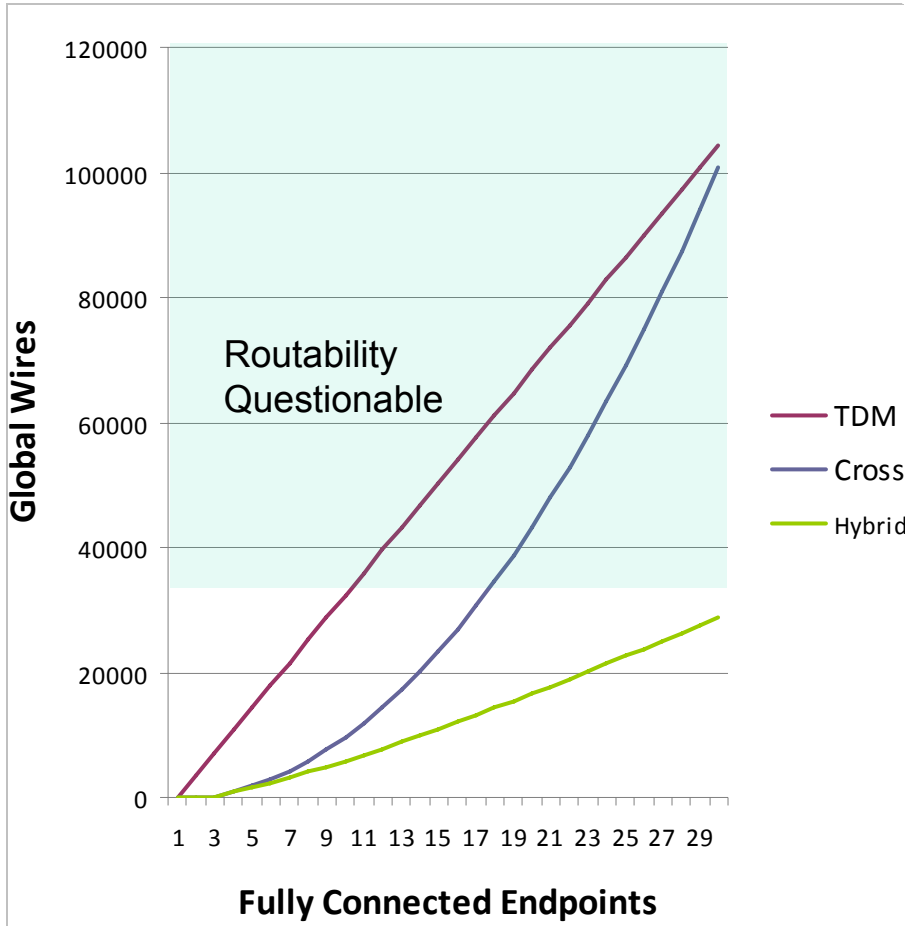
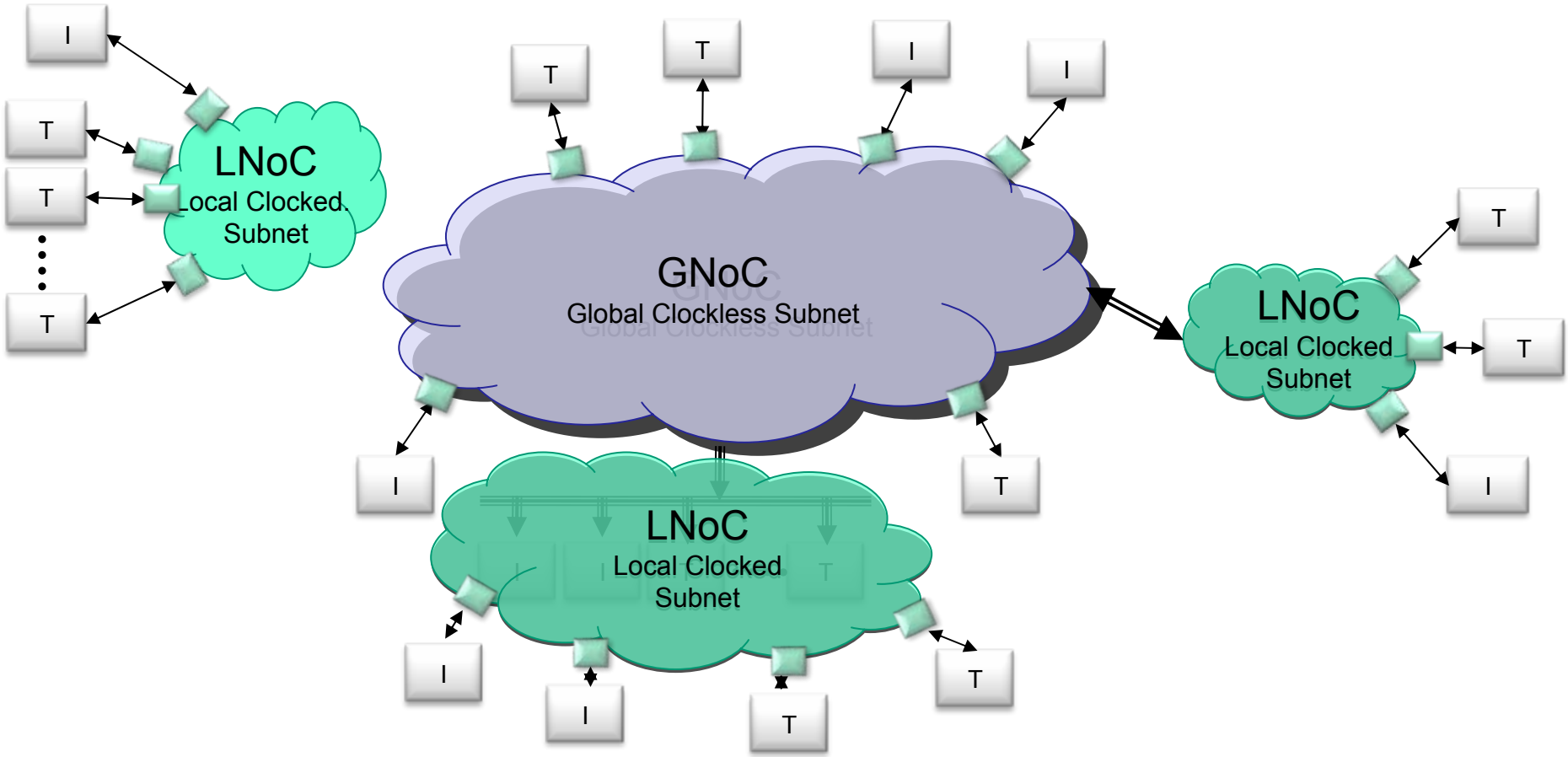
Back-end Nightmare

- Crossbar scalability is not linear
- Quadratic explosion of interconnect wires into a single point
- Routing & Congestion issues abound
- STA Timing Closure:
  - Max time harder to close as frequencies are scaling up on multi-load nets
  - Min time as the number of cores increasing and it is becoming extremely difficult to control clock skew between blocks/subchips
  - Transition time increasing as chips are becoming large and more complex. Wire delay dominates
- **A Hybrid NoC solution addresses these issues**

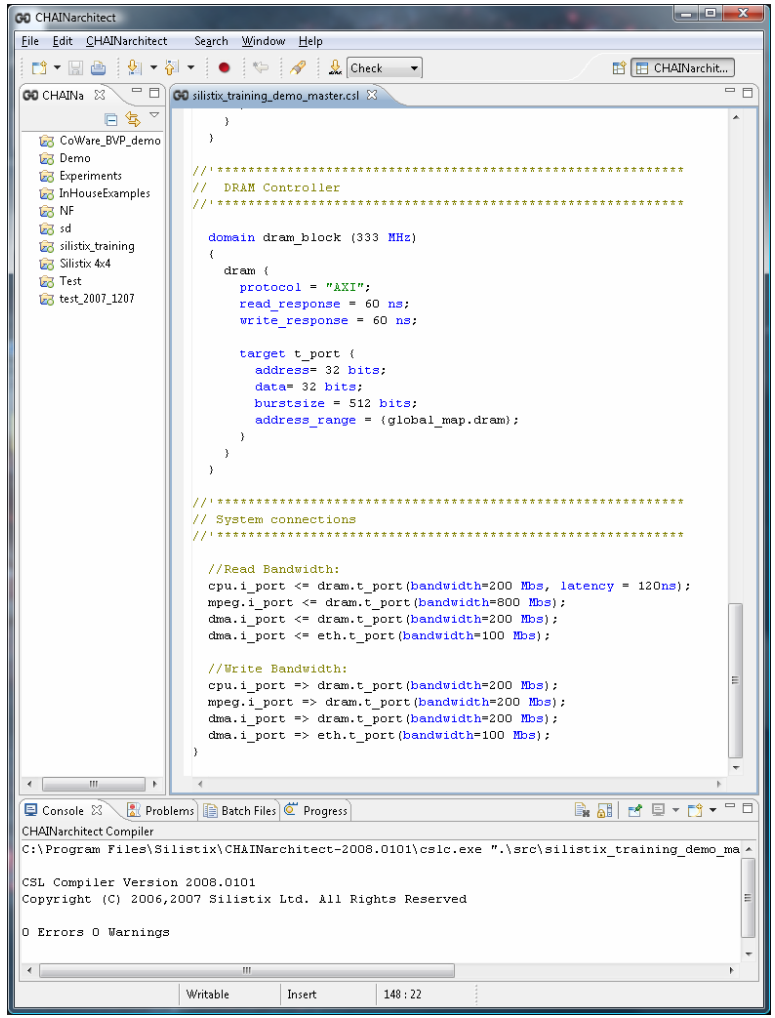


Hybrid NoC Migration



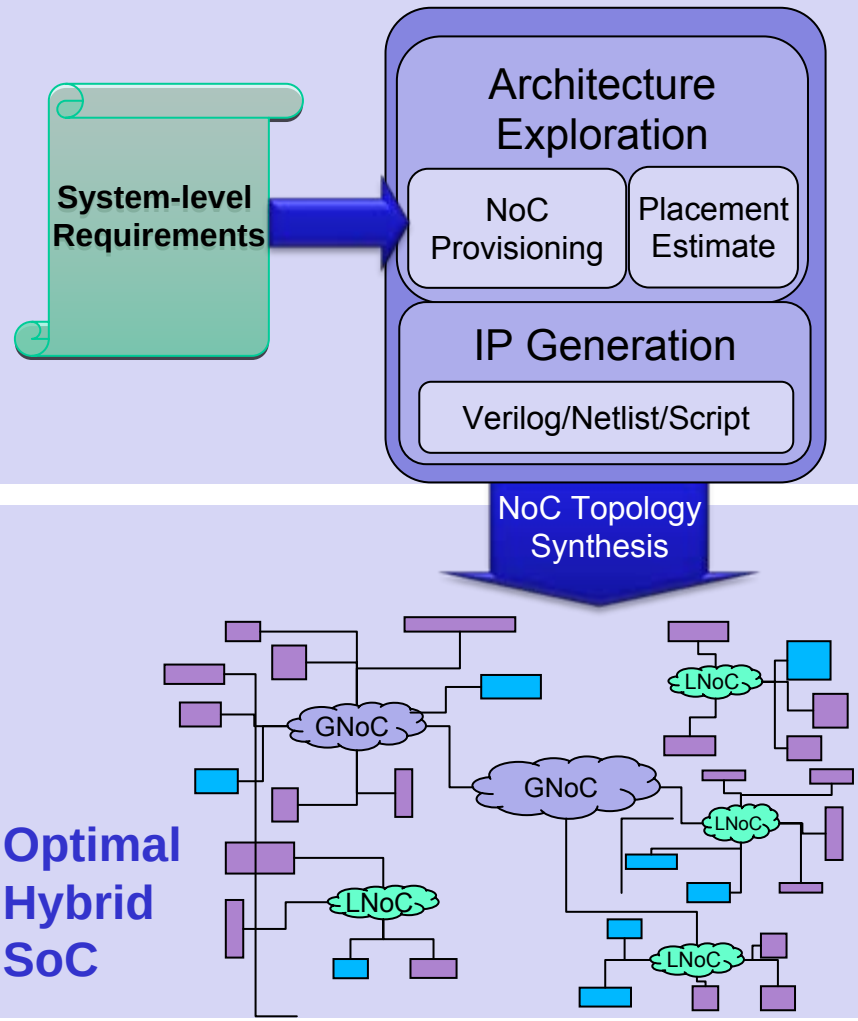
Managing Complexity through Increased Abstraction

- **Interconnect Requirements Capture**
  - Captures key system-level requirements:
    - Protocol and connection requirements of each port
    - Port-to-port connection requirements – bandwidth, latency, etc.
    - Clocking requirements and clock domains
- **Enables Architect to focus on System performance requirements**
- **Tools "Synthesize" Optimal NoC**
  - Topology and component parameters
  - Power, latency and area calculated for created topology
  - Requirements based synthesis vs. schematic capture
  - Quick and Easy tradeoff Analysis through Architectural Exploration



Synthesis of Hybrid NoC Interconnects

- **Tool Chain Necessary**
  - Captures requirements in the manner in which SoC architects think
  - Synthesizes optimal Hybrid NoC topologies
  - Ties into standard flows
- **Silicon IP Deliverables**
  - Configurable clocked and clockless NoC IP blocks
  - Supports common bus I/F protocols
  - Result in predictable behavior using standard tools



Summary

- With SoC complexity greatly outstripping EDA productivity, a holistic approach is desperately needed
- A hybrid Interconnect synthesis methodology enables easy exploration, rapid design and platform re-use while finding the ideal mix between:
  - Global clockless NoC to address DSM process complexity
    and
  - Local clocked NoC to leverage locality
- A successful next-generation interconnect solution MUST allow designers to easily follow the process technology curve into the future
- Eventually, busses will be seen as a a relict of the past

Future of Interconnect:
Synthesized hybrid NoC

Thank You

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- Questions?