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EDP 2009 Panel: “Will We Miss The Bus?”

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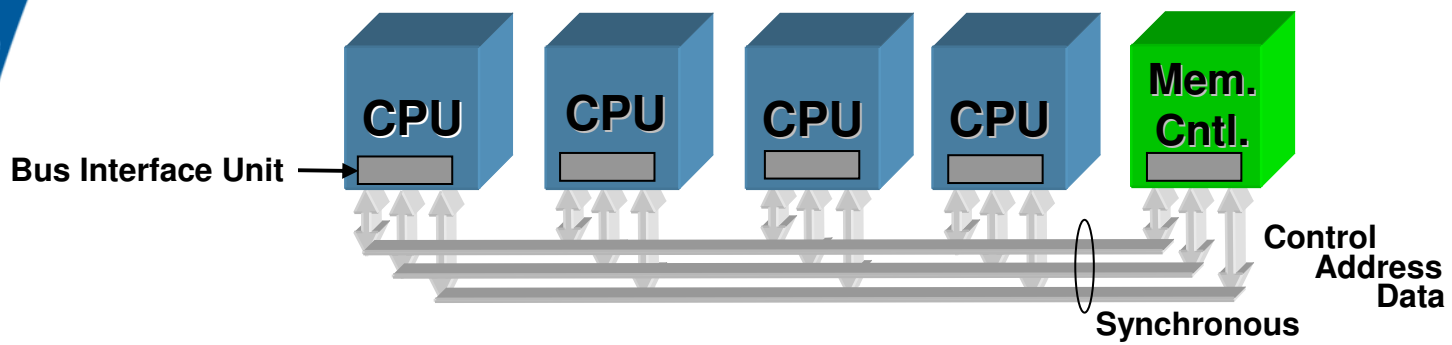
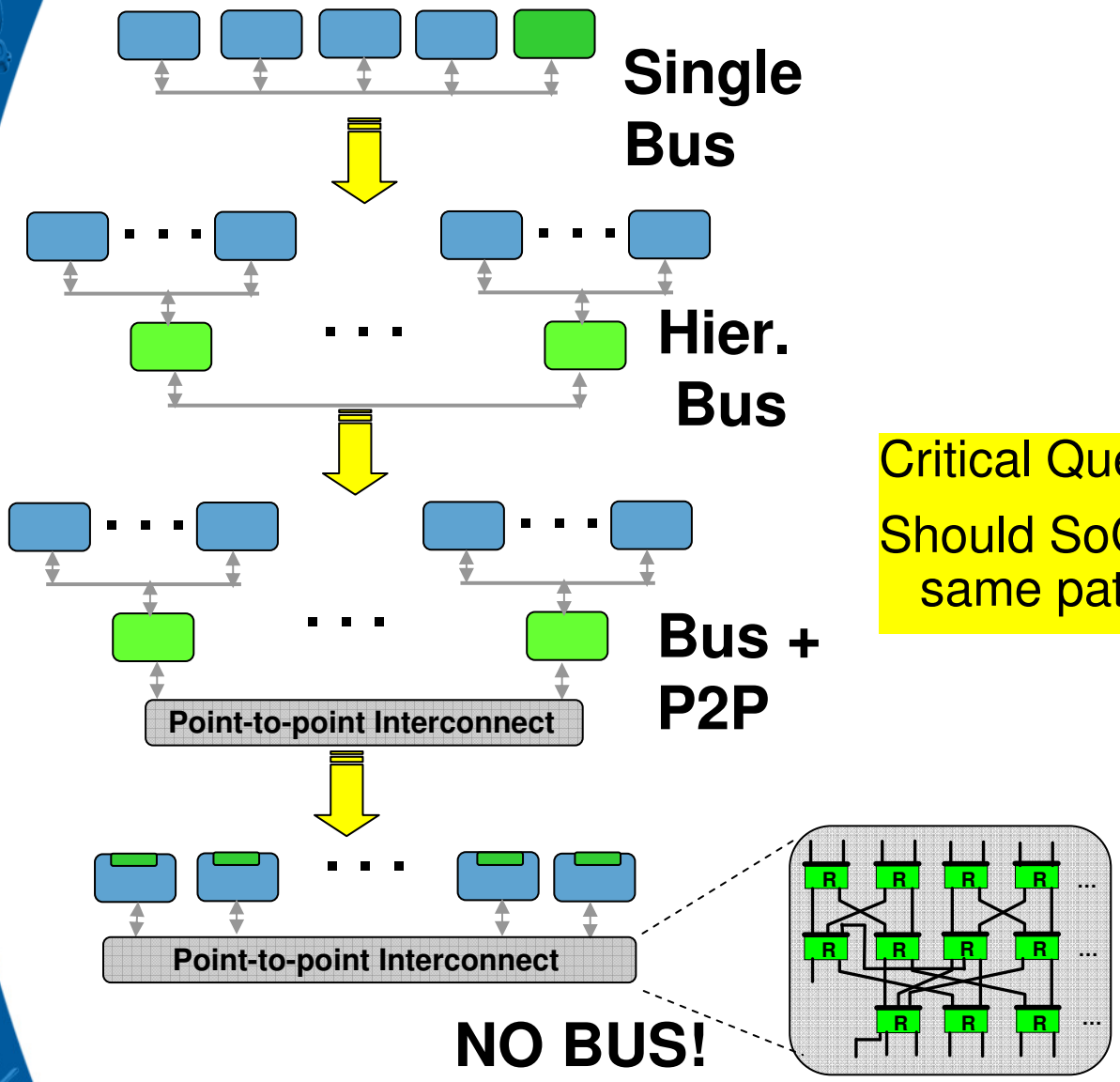
What is a Bus?



- Homogeneous Blocks
  - Address, data characteristics (width, endianness, …) SAME
  - Same "ISA" or same protocol
- Shared Component
  - Physical: Saves wires and pins
  - Logical: Easy "global observation" broadcast based semantics for coherency, ordering
  - Control: Centralized bus arbitration
    - Simple
    - NOT scalable
- PASSIVE
  - "**System View**" provided by Bus Interface Unit
  - Routing: Trivial

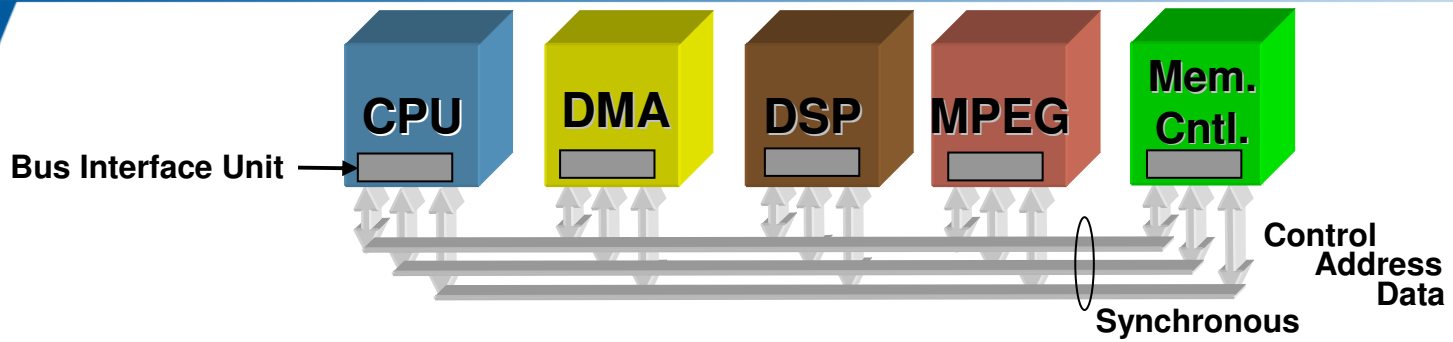
Bus Evolution



Critical Question:

Should SoC architectures follow same path of bus evolution?

Shoehorn Bus into SoC?



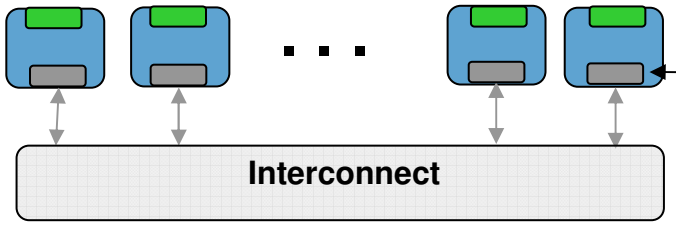
SoC Characteristics

- ~~Homogeneous~~
  - ~~Address, data SAME~~
  - ~~Same "ISA" or same protocol~~
- Shared Component
  - ~~Physical: Saves wires and pins~~
  - Logical: Easy - "global observation", broadcast based semantics for coherency, ordering
  - ~~Control: Centralized bus arbitration~~
    - "Simple"
    - NOT scalable
- ~~PASSIVE~~
  - Bus i/f unit provides "**System View**"
  - ~~Routing: Trivial~~

- HETEROGENEOUS IP Blocks!
  - Address, data characteristics varies widely
  - Simple to complex reads, posted/non-posted writes
- Shared Component – IS A NON-ISSUE
  - Physical: PLENTY of WIRES (modulo P&R issues)
  - Logical: Coherence ease
    - Coherence – not there yet
    - For SoCs, snoop based coherence may not be answer
    - Control: Components have none to simple flow control to complex arbitration – bus solution neither here nor there
    - Need for scalability – 10s to 100s of IP Blocks
- Need for interconnect to be ACTIVE
  - Use (later reuse) of internal/external IP ➔ core IP block retains "local" view
  - **Interconnect provides "system" or "global" view**

What is an ACTIVE Interconnect?

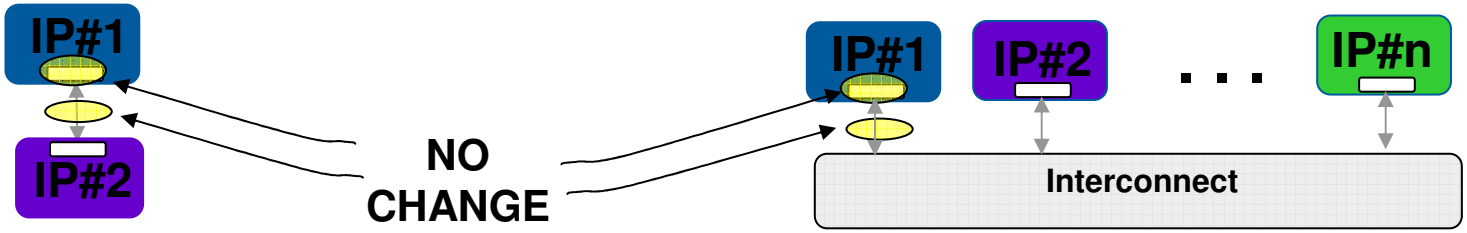
- Is the answer, then?



Interface unit enables system features:
Communication (routing, node ids),
Global address map, …

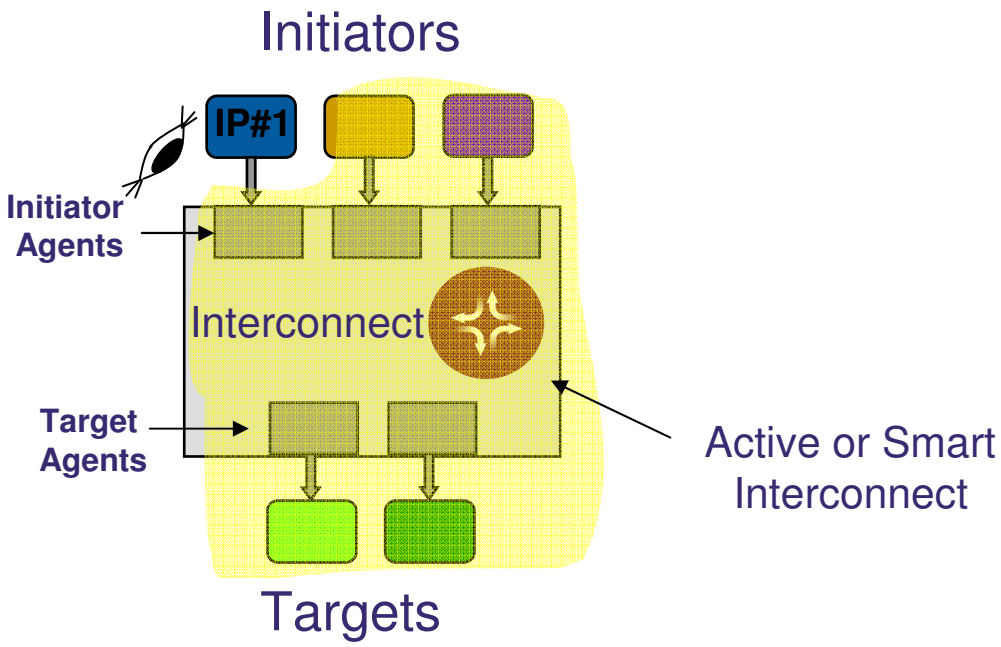
- BUT SoC architectures are composed of heterogeneous blocks - predesigned internal/external IPs with intent to reuse
- Ideally from a core IP's perspective:

  "**Local View**" should be identical to "**System or Global View**"



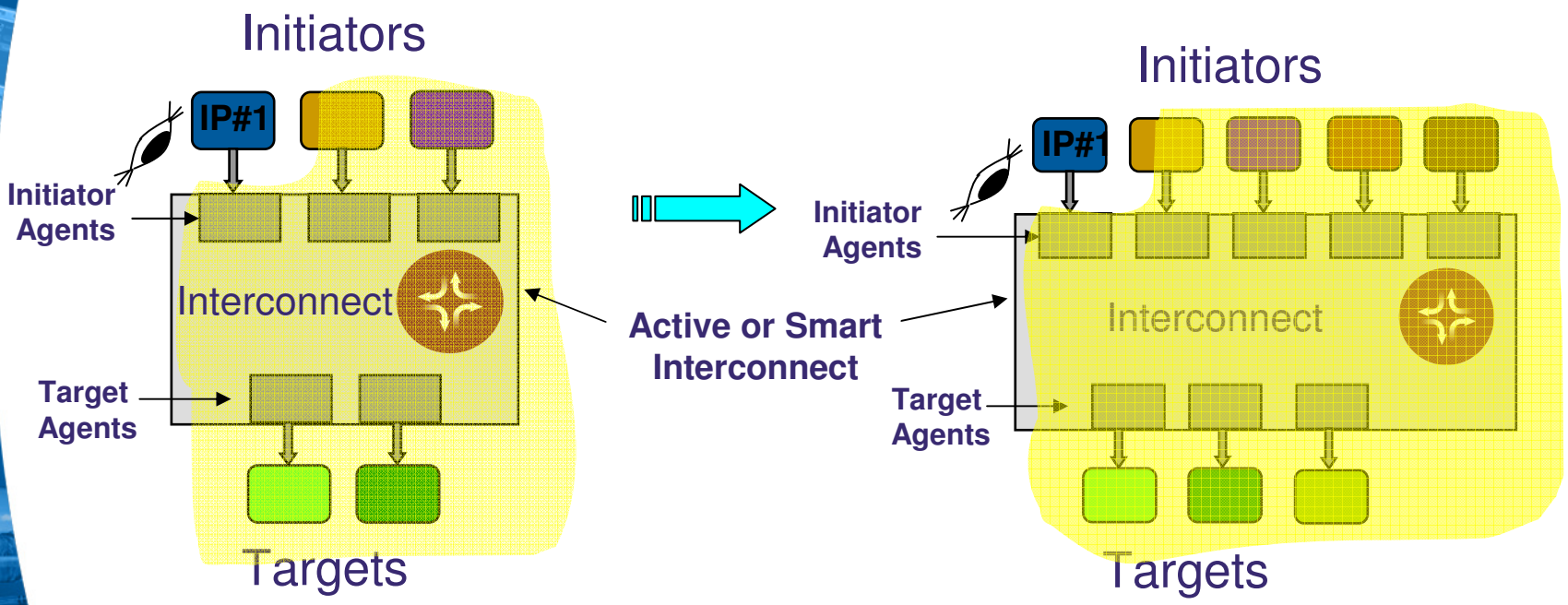
ACTIVE Interconnect - 1

- How do we make this happen?
  - Decouple communication and system services from core IP block and *transfer functionality to interconnect*
    - Passive → Active Interconnect
      - Separate IP block which can be verified separately, enhanced separately, …
- IP#1 believes that it is just communicating with one slave!
  - Agent functionality at initiator and target makes this illusion happen by taking on all system services (node ids, address map, routing)
  - In addition provides other services – QoS, …



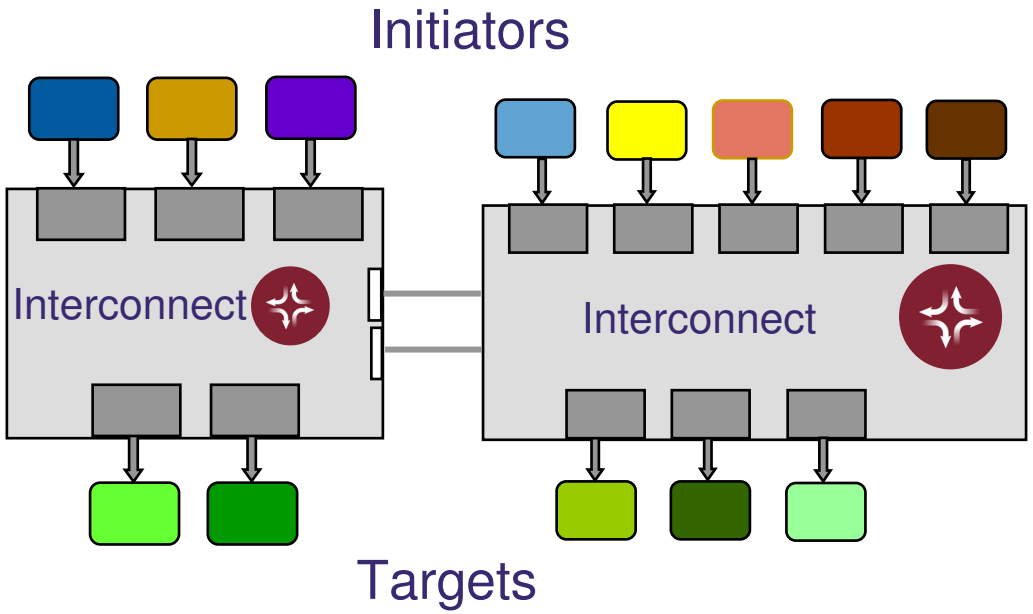
ACTIVE Interconnect - 2

- Enables platforms to be built incrementally
  - Core IPs view of system does not change - only interconnect IP needs to be enhanced

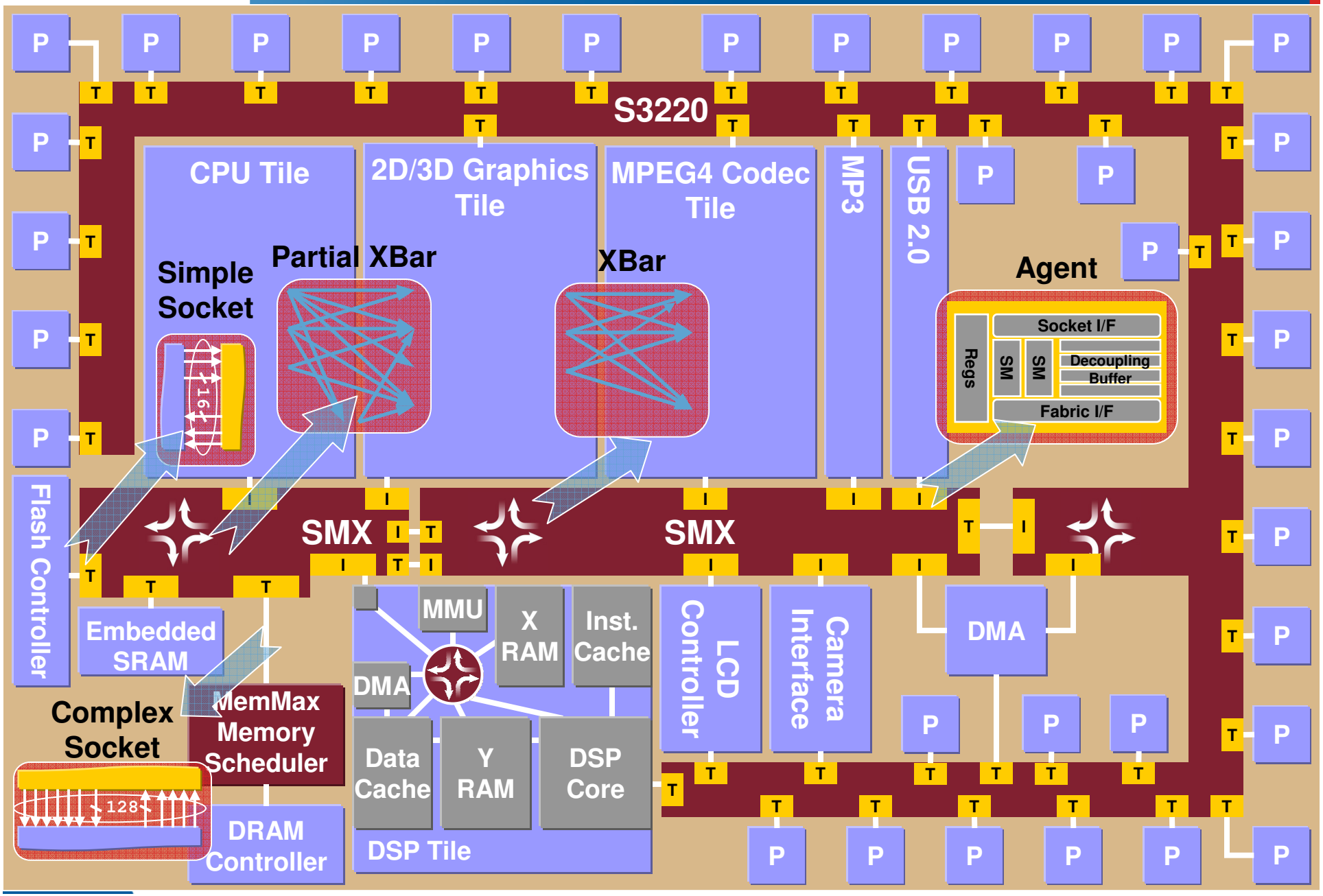


Heterogeneity → Clustered Subsystems

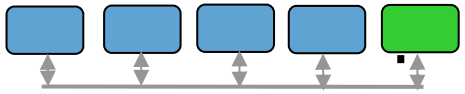
- Large number of heterogeneous blocks
  - Cluster of subsystems – each subsystem has its own active interconnect
    - Topology determined by needs of each subsystem
    - Some interconnects could be buses too!
  - Interconnects tied together through low overhead link(s)



Putting It All Together: The Sonics Way



So …

- Will we miss the 
  - **No** and we shouldn't!
- Will we miss the  ?
  - **Maybe** and we should take care NOT to
    - SoC Architectures demand new thinking
      - Eschew bus "state of mind"
      - Eschew passive interconnects
    - Core IP blocks: Design external interface with **local**, point-to-point view using standard, configurable protocol
      - REUSE is mantra
    - Interconnect block(s):
      - 1 or more - could have multiple topologies
      - Make them "active" enabling
        - System view and services to be part of interconnect
        - Simpler and incremental building of SoC platforms