Multi-Voltage Power Management Verification Issues

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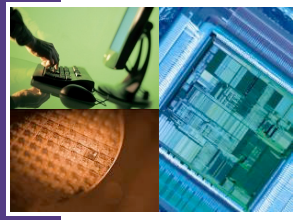

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mimasic

SYNOPSYS® Predictable Success

Power: A Critical Design Parameter

- Consumer Applications Driven Market
  - Wireless/Handheld applications dominate
  - Ever shrinking device sizes
  - Ever increasing design complexity
    - Phone, Music, Camera, PDA, Video, TV … on your palm
  - Increasing power density, design and packaging cost
- Power budgets for plugged-in devices
  - Packaging cost drives power constraint
- Power a factor for move towards multi-core
- 3 Ps of Design: Performance, Price, and Power

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Power Dissipation Factors

- Power = Dynamic + Leakage
- Dynamic power α switching activity, capacitance
- Dynamic power α V^2
- Leakage = I_{leak} * V
- Leakage = Sub-threshold and Gate-tunneling
- Leakage power α e^{-Vt}
  - Need to manage both Active and Standby Leakage
  - Standby power => power consumed even when no useful activity is taking place

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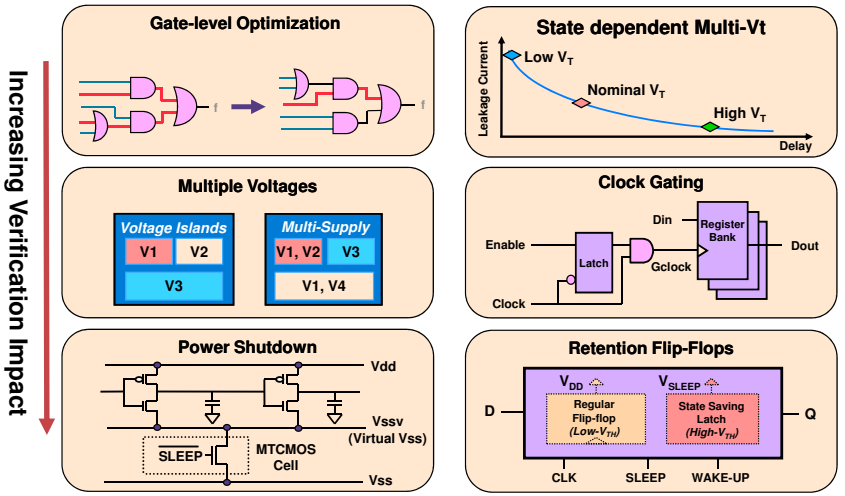
Power Reduction Methods



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Power Management Techniques

- Clock Gating (CG)
- Power Gating (PG)
- Power Gating with Retention (RPG)
- Multiple Supply Voltages (MSV)
- Dynamic Voltage Scaling (DVS)
- Adaptive Voltage Scaling (AVS)
- Multi-Threshold CMOS (MTCMOS)
- Active Body Bias (ABB)

Impact of PM Techniques

Power/Technique	PG	RPG	MSV	DVS	AVS	MTCMOS	ABB
Standby Leakage							
Active Leakage							
Dynamic							

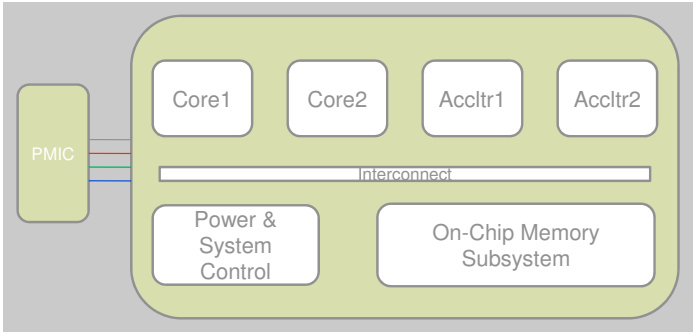
Primary

Secondary

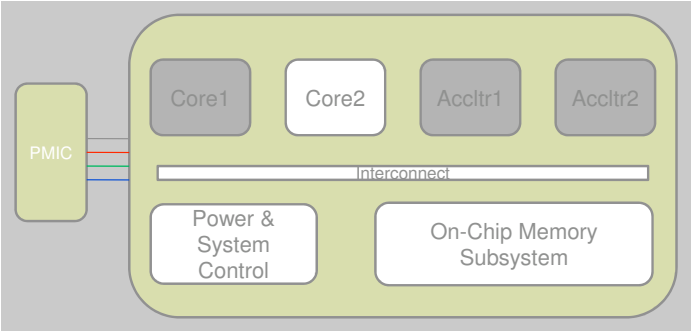
Low Power Impact on the Design Flow

Low Power Technique used	Power Reduction	Timing/Area Penalty	Design Impact	Verification Impact	Implementation Impact
Clock Gating	low	less	less	none	less
Voltage Islands	medium	less	high	Very High	medium
Power Gating	Very high	medium	high	Very high	High
Multi-Vt	low	none	none	none	none
Well Biasing	medium	less	high	none	High

Power Gating



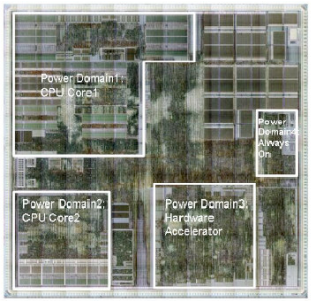
Power Gating



Power Gating

- Standby Leakage Reduction
  - Complete System or Parts of System
  - Power Switches to Implement
- Power Gating Design and Verification Implications
  - Coarse-Grain or Fine-Grain Level
  - Power Gating with Retention (RPG)
  - Isolate to avoid leakage in interfacing active parts
  - Isolate on input side of PG block for latch-up issues
- New power States in your design
  - Power Controller to manage power states and sequencing
  - Verification plan to validate power management
  - Test cases to cover plan, formal verification, rule checking

Power Gating: An Example [TI OMAP 2420 -ISSCC05]



- 5 power domains in TI OMAP SoC enabled by power gating
- Power switches gate VDD, consistsof weak and strong PMOS: Sinks low
- 2-pass power turn-on mechanism to prevent current surges
- Isolation of power down regions

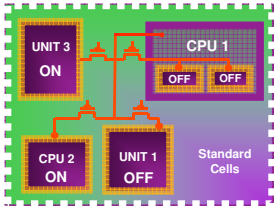
Verification Basics

- A design is characterized by its specification
  - Set of features and their intended behavior
- Verification ensures implementation matches specification
  - **Dynamic** : Simulation → Applies stimuli to exercise design
  - **Static** : Formal and Structural checks
- All methods require a reference model
  - Executable (Behavioral, TLM, C, …)
  - Assertions
  - Transformed design – Consistency across the flow
- Coverage model is used to track progress & effectiveness
  - **Explicit –** functional, assertions
  - **Implicit –** tests, code

Used by Dynamic & Static

Verifying Power Shutdown

Must verify all power modes (power-up/down) and their accompanying sequences



- **Specification:**
  - **Power Domains: Define block(s) to be powered up/down**
  - **Isolation: Isolate outputs from OFF blocks read by ON blocks**
  - **Retention: Save/Restore important registers during shutdown - Hibernation**
  - **Signal Sense: Logic of power, isolate, retention control signals**
  - **Power Distribution: Power supply network and power switches**
- **Semantics:**
  - **Power Down: Signals in OFF block become unknown (X)**
    - **Activity within OFF blocks ceases – inputs may remain '*live*'**
  - **Power Up: Activity restarts (values propagate) - like reset**
  - **Isolation: Reading OFF blocks yields correct clamp voltage**
  - **Retention: Retention registers properly save / restore state**
  - **Power Supply: Correct supply voltage delivered to corresponding blocks**

Initial blocks in power-gated blocks

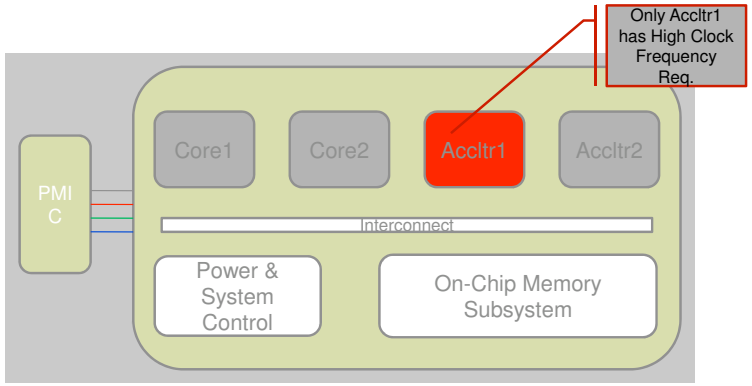
Multiple Semantics Available

- **Do not execute → error**
  - Move to the test-bench
- **Execute each time block is powered on**
  - Memory initialization
- **Execute once upon power on**
  - Open log file
- **Execute once if power on at time 0**
  - Synchronization
- **Execute once at time 0**
  - Co-simulation (Vera, Spice, Virtio)

```
initial $readmem(…)
initial $monitor(…)
initial #2ns clk=0;
initial $memory(…);
```

- Upon Power OFF
  - **Kill** process
  - **Suspend** process
  - **Keep** process alive

Multiple Supply Voltages



Multiple Supply Voltages

- Dynamic Power Reduction
  - Squared effect on dynamic power
  - Keep lower voltage of operation for most of the chip
  - Also reduces active leakage, linear effect
- Design & Verification Implications
  - Multiple Supply Voltages (MSV), Dynamic Voltage Scaling (DVS), Adaptive Voltage Scaling (AVS)
  - Level-shift paths crossing voltage islands
  - Hold and set-up issues on crossing paths
  - May need to isolate and level-shift
- Additional Power States in your Design
  - Simulation, Formal, and Rule Checking Needs
- Power Formats (UPF) for Architecture Description

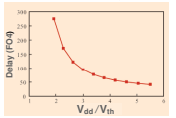
Power States Grow Quickly …

State/Island	Core1	Core2	Accltr1	Accltr2	PSC	MemSub
OFF						
POWERUP						
STANDBY1						
PMODE1						
PMODE2a						
PMODE3						
PMODE4						
PMODE2b						
PMODE2c						
PMODE5a						
PMODE5b						

- Each color represents a different voltage , gray represents power down
- Verification complexity grows quickly, upper bound is the cross-product of power and logic states

Power Aware Verification

- Gated clocks & multi-Vdd reduce dynamic power
  - Multiple Vt can reduce leakage at the expense of speed
- New designs suffer from static power (leakage)
  - Caches : 75% power is leakage
- Shutdown reduces static/dynamic power
  - Requires more up-front work by designers
- Power concerns move up in the flow
  - Design and verification teams must consider power
    - Voltages become functional
    - Cannot be relegated to the *"back-end guys"*
  - Specification and verification at the RTL level - and higher
  - Test plan and coverage model must consider power (PST)



	PN1	PN2	PN3	PD1	PD2
PS1	0.95	1.09	1.08	on	on
PS2	1.08	1.08	1.08	on	on
PS3	1.15	1.08	1.08	on	on
PS4	0.95	1.08	1.08	on	off
PS5	0.95	1.08	0.95	on	off
PS6	0.0	1.08	0.0	off	off

Verification Environment Concerns
(It is more than just the design)

- Modeling constructs
  - Assertions / Checkers
  - High-level models (memories, analog, …)
  - Initial blocks
- Assertion Behavior within powered down blocks
  - **Kill -** Most common, disable (and restart)
    - Power-down will not cause assertions to fail (design is X)
  - **Keep -** Power-aware assertions must remain active
    - up/down power sequences
      - Retain → OFF → … → ON → power_ack → Restore
  - **Suspend -** May need to retain state

```
request |=> ##[3:8] grant
```

    - Protocol violation if request → shutdown ?

Conclusions

- **New designs (< 90nm) will be power limited**
  - **Will use multi-Vdd, Multi-Vt, and power-shutdown**
- **Power awareness is moving up the flow**
  - **Must be considered by architecture, design, and verification**
- **Cost of verification is increasing**
  - **Voltages have become functional → they need to be verified**
  - **Power domains add more states**
    - **Cross coverage of all power domains (PST)**
  - **More tests exacerbate performance needs**
    - **Emulation does not model MTCMOS**
- **Power-aware flow increases productivity and predictability**
  - **Power intent captured up-front**
    - **Power constructs added post-synthesis are NOT verified**
  - **Common semantics across the flow preserve intent integrity**
  - **Enables automation**
    - **Power domain spreading, IR-drop, and rush-current analysis**