Regular Designs and Computational Lithography: Their Past, Present and Future.

J. A. Torres
Mentor Graphics Corporation, 8005 S.W. Boeckman Road, Wilsonville, OR 97070
andres_torres@mentor.com Tel. +1 (503) 685 0322

ABSTRACT

It is common knowledge that for every lithography process there is a set of layout configurations that exhibit improved robustness, meaning that their patterning performance remains relatively stable under a wide variety of process conditions. Such ideal pattern configurations are mainly implemented in two ways: By direct simulation of the process conditions (in what is becoming known as Computational Lithography) and by imposing specific layout configurations that are known to print reliably (Regular/Gridded layouts). This work emphasizes that both approaches are complementary in nature, and by no means mutually exclusive. While pattern gratings appear to be the final frontier of lithography robustness, even such patterns must be verified around their discontinuities to fully realize the benefits of layout regularity.

Keywords: Microlithography, litho-friendly, RET-compliant, process models, low k1, subwavelength, DFM, gridded layouts, computational lithography.

1. INTRODUCTION

Recently there has been a renaissance related to physical design, driven by the need to control variability and enable the reliable manufacture of 65nm features and below [1]-[2]. While the new approaches limit the number of layout configurations that circuit designers have access to, they allow the designers to continue developing the products in parallel with the manufacturing process, so the designers have accepted the restrictions.. In addition, the fear of massive increases in area or poor electrical performance appears to be unfounded, since benefits in electrical performance and limited area increase when using regular layouts have been reported [3]-[4].

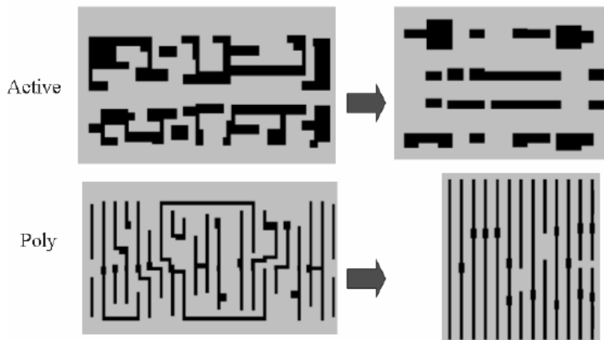

Figure 1. Evolution of layout complexity [5]. Freeform (90nm and above) to restricted (65nm and below).

Figure 1 shows a typical [5] example of how layout has become more regular, despite the initial reluctance of the design community to adopt it. While there are logic implementations that take layout regularity to its limits (Figure 2), even such layouts can be deemed two-dimensional, due to the discontinuities needed to make the necessary interconnection and define individual transistors.

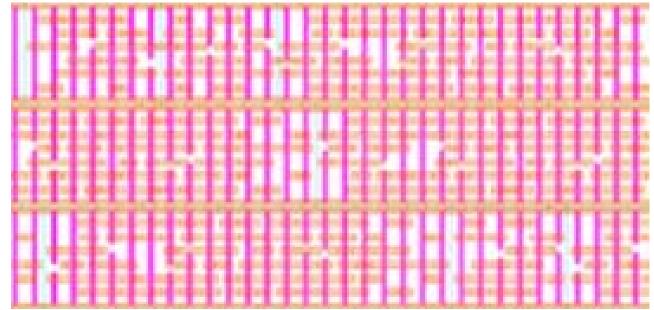

Figure 2. Logic standard cell placement with maximum regularity (Courtesy of Tela Innovation).

While the human brain can process the above layout and label it as "regular," there is no formal description of the minimum conditions needed to consider a pattern regular from the lithography point of view. Indeed, an array of lines and spaces meets the regularity definition in the geometric sense, but the challenge remains in creating a useful definition of regularity that can be used to determine the pattern transfer feasibility of a given layout.

2. REGULAR DESIGNS

Figure 3 shows three interpretations of regular layouts. Figure 3A exemplifies early attempts towards pattern regularity. The landing pads were placed in an asymmetrical fashion, mainly to reduce pinching problems at the base of landing pad. While such change was sufficient for 65nm processes, at 45nm (Figure 3B) the landing pads were again centered on the features, to reduce the necessary spacing between features and because the pinching problem at the base of the landing pad was no longer an issue (mainly due to the change in design rules, new equipment and improved OPC recipes). Figure 3C shows how landing pads can be removed altogether to achieve maximum regularity, but as can be observed, full gratings are not fully realizable because devices have a finite size, which means that discontinuities in the grid have to happen to separate devices (in the case of poly), or to allow connections only between the relevant transistors (in the case of metal).

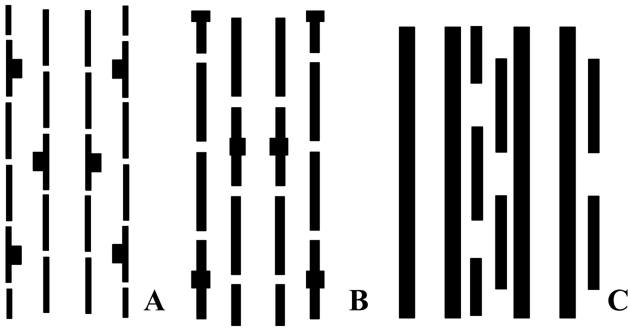

Figure 3. Polysilicon 45nm layout regularity evolution. (A) Asymmetrical landing pads. (B) Centered landing pads. (C) Removal of landing pads.

It is also important to point out that for regular layouts, the choice of pitch and width for the grating becomes critical not only from the manufacturability standpoint, but also from the economic target. The selection of the regular pitch and width is the main driver of the size of the design (keeping topology constant), which means that they need to be chosen carefully to provide the right balance between manufacturability and economics.

In addition, not only do the lithographic resolution aspects become important as to the choice of the minimum pitch and width of the layout, but also how etch, resist development, particles and electrical device requirements need to be factored in determining the optimal separation between devices.

To illustrate the need of computational tools when selecting a given regular topology, we will consider only the lithography aspects, but similar arguments can be made for etch, stress, resist collapse, and many others.

3. REGULARITY AND COMPUTATIONAL LITHOGRAPHY

In retrospect, is clear that implementing regularity means removing any bends, or corners that change the morphology of a piece of layout to any structure other than a rectangle. This was not how regularity was originally understood when layout designers considered arrays as the ultimate regular structures.

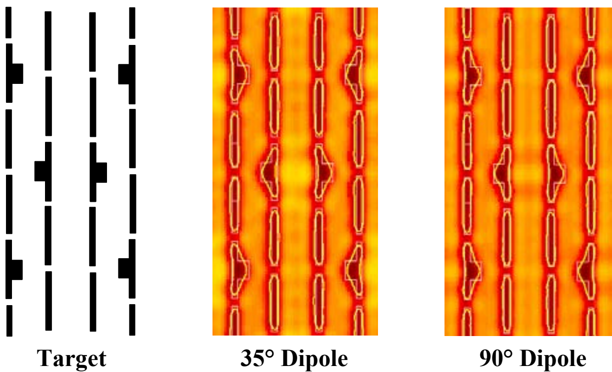

Figure 4. Asymmetrical landing pad performance for two different illumination schemes

Figure 4 shows the original target, as well as the lithography simulation of a 0.93 NA system with 35- and 90-degree dipole apertures. Only two of these aggressive illumination conditions are shown to illustrate how, despite regularity, there are pattern transfer limits even for regular structures. Of course, Figure 4 cannot truly be considered a full regular structure, since the landing pads serve as proximity wells for this layout. Because the landing pads are necessary to accommodate the square contacts, variants such as those included in Figure 5 centered the landing pads to achieve tighter pitch and control (which was obtained to a degree). However, the transistors associated with such landing pads exhibited varied performance, since the gates were not square, but distorted, due to the presence of the landing pads.

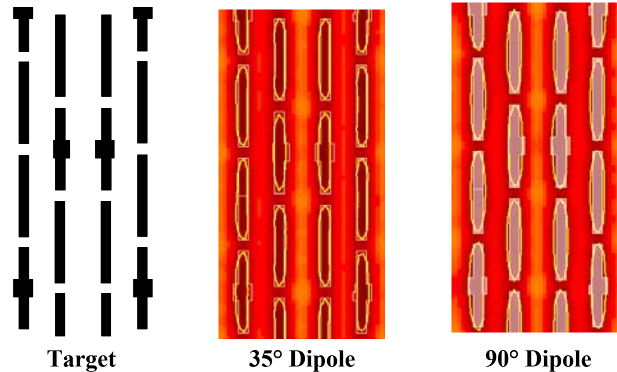

Figure 5. Symmetrical landing pad performance for two different illumination schemes

Different topologies were tried, and decisions such as using rectangular contacts (instead of square) and removing completely the need for landing pads gave rise to much more regular layouts. But even in these regular configurations, Figure 6 shows that, depending on the length, width and spacing between rectangles, the gates are not fully rectangular and there are still locations that may present challenges to pattern transfer. The same figure shows that, depending on the illumination scheme, it is possible to minimize or exacerbate such challenges.

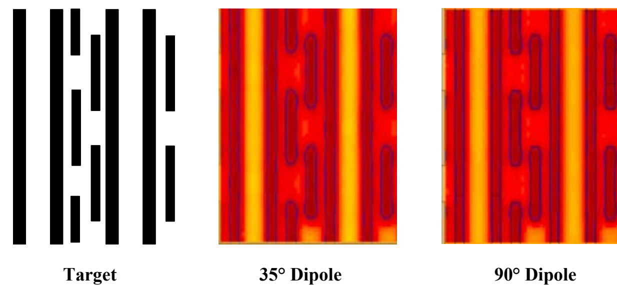

Figure 6. Landing pad removal and imaging performance for two different illumination schemes.

3.1 PROCESS MODEL REQUIREMENTS

One of the perceived limitations of computational lithography is that at the early stages of the process, the details of the final mature process are not known. Therefore, making any predictions using quasi-physical models may result in

suboptimal layout configurations. This is, in general, true, since there is a minimum of information needed to arrive at useful predictions as to the process. Recently, we presented a study [6] that highlighted the minimum modeling requirements needed to create a pattern transfer envelop around the final process. The study focused on multiple production processes, including 65-, 45- and 32nm, and three different levels: gate, contact and local interconnect.

As a way to compare the relative performance of the different processes, process variability bands (PV-bands) were calculated for all the process and layers under two conditions. The first used early estimates of the process that considered: Idealized illumination profiles, simple resist models, estimated process variations in focus, dose and mask bias, simple OPC recipes, and minimum mask constraints.

In the second condition, the actual process variability bands used the calibrated models that consider source and pupil maps, calibrated resist models, actual 3 sigma process variations in focus, dose and mask bias, and final OPC recipes under real mask constraints. Examples from such studies show how early estimates can suggest that highly bi-dimensional topologies (as is the case for interconnect layers) would fail, but after tuning the process, those same structures can be reliably manufactured (albeit compromising their pattern fidelity).

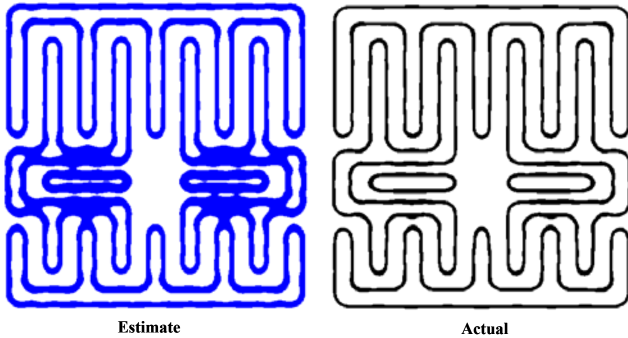

Figure 7. PV-bands for 45nm metal interconnect layer. Estimated (left), Actual (right).

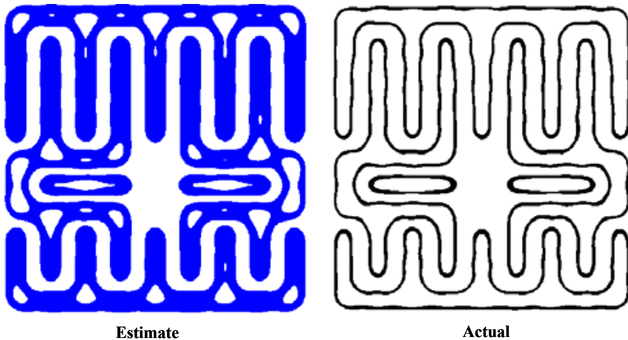

Figure 8. PV-bands for 32nm metal interconnect layer. Estimated (left), Actual (right).

To prevent the degradation in pattern fidelity (which is much more critical in gate layers), regularity has been strongly imposed in such layers, and its benefit is immediately observable in Figure 9 and Figure 10. Both figures raise interesting questions: while fully regular layouts would mean arrays of truncated lines and spaces, these two examples still have two dimensional components, which, under the geometric regularity definition, should exhibit limited manufacturability. Clearly, that is not the case.

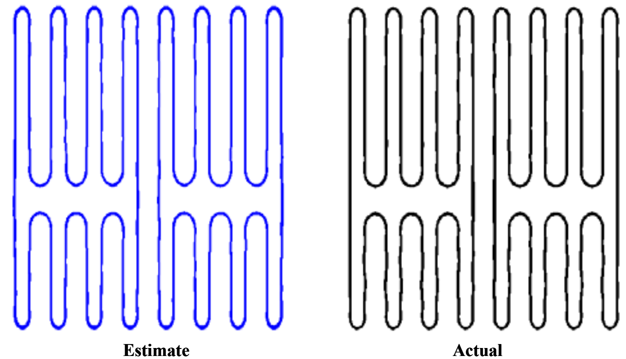

Figure 9. PV-bands for 45nm gate layer. Estimated (left), Actual (right)

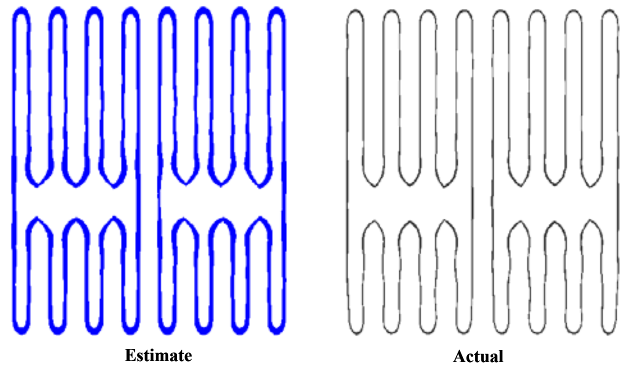

Figure 10. PV-bands for 32nm gate layer. Estimated (left), Actual (right)

This is a simple argument for having a more useful definition of regularity that should incorporate information as to how a given pattern responds to a given process.

4. CONCLUSIONS

There are undeniable benefits of regular designs—better manufacturability, and better circuit predictability at a limited area penalty cost. However, coming up with the optimal set of regular designs and process conditions remains an active area of investigation.

This work highlights how different interpretations of regularity react to different process conditions, ss well as how irregular layouts (layouts composed by features other than rectangles) are able to perform well in 45- and 32nm processes.

This work indicates that geometric regularity by itself is a limited indicator of the manufacturability of a design, mainly because even in what appear to be regular structures, the process interactions can still introduce sub-optimal imaging conditions around the grid discontinuities.

At the same time, the fastest way to arrive at manufacturable devices is to incorporate geometric regularity, which can prescribe feasible solutions in a more efficient manner. But to

come up with such prescribed layouts and to guarantee the adequate pattern transfer of the layout, computational tools must be used.

In other words, both methodologies have their own benefits and drawbacks. When used together, they reinforce each other, providing the means for more efficient circuit design flows.

While in the past there seemed to be a competition between both techniques, at present (and in the future) both techniques will be used concurrently to further optimize and make the design and manufacture of integrated circuits much more cost effective.

5. REFERENCES

[1] L.W. Liebmann, A.E. Barish, et. al. "High-performance circuit design for the RET-enabled 65nm technology node." Proc. SPIE Int. Soc. Opt. Eng. Vol. 5379 pp. 20 (2004)

[2] M.C. Smayling, H. Liu, et. al. "Low K1 logic design using gridded design rules." Proc. SPIE Int. Soc. Opt. Eng. Vol. 6925 pp. 69251E (2008)

[3] J. Wang, A.K. Wong. "Standard cell design with regularly placed contacts and gates." Proc. SPIE. Int. Soc. Opt. Eng. 5379 pp. 47 (2004)

[4] Torres J.A., Berglund C.N. "Integrated Circuit DFM Framework for Deep Sub-Wavelength Processes." Proc. SPIE Int. Soc. Opt. Eng. 5756, pp. 39 (2005).

[5] Y. Troullier, V. Farys, et.al. "32-nm SOC printing with double patterning, regular design, and 1.2NA immersion scanner." Proc. SPIE Int. Soc. Opt. Eng. 6920 pp. 65201D (2007)

[6] J.A. Torres. "Layout verification in the era of process uncertainty: target process variability bands vs. actual process variability bands." Proc. SPIE Int. Soc. Opt. Eng. 6925 pp. 692509 (2008)