Fitting DFM in Your Design Flow

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Abstract: *This paper surveys the DFM landscape across semiconductor industry. Beyond the DFM buzz, it explains what the industry is doing today and the new opportunities for 65 & 45 nm designs. However, in order to harness the new manufacturability improvement opportunities effectively, the paper describes the need for industry-wide collaboration that will allow flow of critical information between the four key stakeholders - Chip Designers (IDM and Fabless); Chip Manufacturers (Fabs, IDMs); EDA Vendors and Fab Equipment Suppliers. With increasing pressure for Time-To-Market, some design teams find it difficult to fit the new DFM methods into their design flow. Approaches are discussed that demonstrate DFM fitting very well into a chip design flow and infact improving Time-To-Market for the Deep Submicron Chips.*

1. DFM & DFY – As old as Chip Design

The areas of DFM (Design For Manufacturing) & DFY (Design For Yield) are not new. Knowingly or unknowingly, we have been practicing DFM/DFY techniques ever since we began the VLSI revolution over 25 years ago.

In order to achieve manufacturability for a Very Large Scale Integration (VLSI) of transistors on a chip, a set of Design Rules would be established for each manufacturing process. The Design Rules cover a myriad range of design layout restrictions in order to achieve commercially viable Yield for the chips. Some examples of Design Rules are: Minimum Poly Width, Minimum Spacing between metal wires, Minimum metal density, etc [1]

Adherance to the Design Rules has become an integral part of every chip design flow. The Place and Route EDA tools are guided by the Deck of Design Rules in order to place the transistors and route their connections. Before tapeout, the final layout is checked for compliance with the Design Rules using DRC tools. A violation of a Design Rule would result in visible loss of product Yield. Therefore, Design Rules can be considered as the earliest form of DFY.

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Another ubiquitous DFM/DFY technique is Memory Redundancy. Since memory is more densely packed on a chip than random logic – they are more prone to defects and hence yield/manufacturability loss. Our VLSI industry considered the idea of not packing the memory cells as densely – in order to reduce defect occurance – although this would amount to increase in chip area. The chip industry came up with a better method that took advantage of the regularity found naturally in memory structures (vs. random logic). The idea was to keep the memory structures dense – but augment with a few redundant rows and/or columns of memory that could be swapped as needed right after chip testing. A 2-10% increase in chip area (to accommodate redundant memory) has shown upto 50% increase in chip yield. [2]

The above two examples of DFM/DFY – Logic Design Rules and Memory Redundancy - help a chip avoid or recover from *Physical* defects during manufacturing. In a similar fashion our chip design community has long been using techniques that help with DFM/DFY from *Electrical* defects. An example is the offset of Voltage Control of differential amplifiers by transistor sizing in order to reduce mismatch.

2. DFM/DFY – Why the buzz now?

From Section 1, it is clear that – in a general sense – our chip design industry has been practicing DFM/DFY methods ever since we started. And we have been evolving in our DFM/DFY methods too. Therefore, why has there been a buzz around these acronyms lately ?

It turns out that there is one radical change in our design and manufacturing methods. We'll get to the radical change in a moment. That radical change – when coupled with the evolutionary changes happening with shrinking device geometries - is amplifying the manufacturability and yield problems to a point where ad-hoc approaches to DFM/DFY are not believed to stay viable. The buzz is centering around the need to create a structured approach to DFM which is integrated into the mainstream chip design flow.

The radical change happened when our industry went from a 250nm feature size (width of the gate of a CMOS transistor) down to 180nm. Well, the finest resolution of our Lithography equipment – the stuff used during manufacturing of transistors and their connecting wires – remained at 193nm ! It was clear that the shape of a transistor's poly or a metal wire, seen on a VLSI design engineer's workstation screen, would not be the

same when it got manufactured [3]. There would be some distortion. The distortions in shape could violate Design Rules on minimum width and minimum spacing. A new step was born in the VLSI design flow. It got a generic phrase – Reticle Enhancement Techniques (RET). The specific step for compensating the transistor and wire shapes in a layout to account for the expected manufacturing distortions got to be called Optical Proximity Correction (OPC) [4]

OPC worked quite well for 180nm process technology. The chips manufactured in this process went on to enjoy profitable yields and life was good. It is around the time of OPC that the acronyms DFM & DFY started to gain widespread use.

However, in order to remain faithful to Moore's Law, our industry moved on to 130nm feature size (in the stipulated 18 months). OPC tools started to find the correction process getting more and more difficult. Then came along 90nm process, then 65nm & 45nm and 32nm on the horizon. With shrinking geometries, the envelope of VLSI evolutions moves forward on all fronts. The number of transistors on a chip increases, the number of metal layers increases, the frequency and power demand increases. The emerging effects such as IR drop, Noise, Cross-Talk start to become critical. It is clear that RET/OPC alone will not be able to handle the amount of variance between what a designer draws on his/her workstations and what gets printed on the die.

A structured approach is needed in order to deal with the fundamental issue of variation in manufacturing from what is designed – which is exacerbated by the shrinking feature size.

The evolution from ad-hoc DFM to a structured DFM methodology has a parallel that is all to familiar to DFT professionals. In the 70s, in order to manage the VLSI Test problem, ad-hoc Design For Test methods were used. These included analysis of the designs and addition of appropriate control and observe points. The ad-hoc methods worked for a while until the complexity of our designs increased (and got to be called SOCs). The structured DFT approach of Scan Design gained popularity. Today Scan is ingrained in mainstream design flow – as every EDA Synthesis tool supports automatic insertion of Scan and plenty of EDA tools perform Automatic Test Pattern Generation (ATPG) on Scan designs [5]. We expect to see a similar maturity path for DFM – as DFM techniques get completely ingrained in mainstream design flow.

Here is the outline for remainder of this paper. After establishing some working definitions, we will describe the scope and context of DFM as it is being practiced today. Section 4 provides a simple business justification for the need of DFM. Section 6 details the state of the art in DFY for Physical defects – the most pervasive DFM methods in use today. Section 8 describes the inter-relation between DFY & DFT and how both functions can help each other in order to achieve competitive cost and quality for the product. Section 9 calls for an industry wide collaboration that is needed for permeating DFM into the design flow.

3. DFM/DFY – Today's Scope & Context

DFM (Design For Manufacturability): In the context of a fully manufactured chip (i.e., ready to be used on a system board), DFM encompasses any and all measures taken during the chip design flow that help improve Yield, Repair, Assembly, Test & Reliability of a chip.

DFY (Design For Yield): Design measures whose primary focus is Yield improvement.

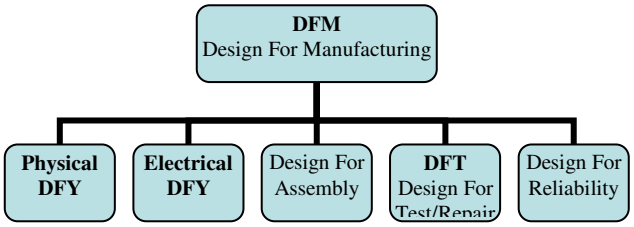


Figure 1: Taxonomy of DFM methods

The areas of Design for Repair and Design for Assembly (packaging) have a narrow scope and appear to be under control today – often handled by Design for Test (DFT) teams. Therefore, we do not hear much about these important functions. The area of Design for Reliability has traditionally covered Burnin & Soft Error support during design – again handled by DFT team. However, the area of chip reliability is of increasing concern. Yield is the biggest lever for manufacturing margin and hence profits. Interestingly, it also happens to be a big lever for improving product quality. Therefore, Design for Yield will continue to have an important place in the design flow.

Given that DFT was established decades ago and has been covering Repair, Assembly, Test and Reliability requirements in the design phase, the area of DFY is the only one that remains under the broad umbrella of DFM. Therefore, considering the importance of DFY, the terms DFM & DFY get used interchangeably. On the lighter side, since DFY has hijacked the term DFM – some industry folks have resorted to using the DFX to imply the strict context and definition of DFM !

In the rest of this paper, we will use the above definitions.

4. DFY – Why Should I Care ?

A 90nm process with 6 metal layers and 26 masks is used for a chip that produces 30,000 300mm wafers each month (running at 90% capacity). The cost of each wafer is $3030 [6]. If each wafer generates a revenue of $5000, even a 1% increase in yield will provide $1.5M of additional chips per month !

For the same test coverage (assume 99%), this 1% improvement will result in a 7% improvement in shipped product quality ! [7]

Therefore, even a small increase in yield has a significant improvement in profits and quality of the product.

5. Defects – Random & Systematic

There are two primary mechanisms of yield loss on a wafer. One is due to physical defects and deformities in the structures of the transistors, the interconnecting wires & vias. These defects are visible. Examples are open in a wire, or a short between source and gate of a transistor. The other mechanism for yield loss is due to electrical variations in the composition of transistors, wires and vias. These variations are not visible but can become significant for the chip for it to not function correctly at the operating specifications (Voltage, Frequency, Temperature). Examples are - excessive doping in the channel of a transistor or higher resistivity in a wire.

Physical defects are typically caused by dirt particles during the processing of a wafer. They are also known as *random* defects. Electrical defects are typically caused by variations in equipment and chemical mixes. They are also known as *systematic* defects.

To be sure, there is a 3rd source of potential yield loss due to defect mechanism that is not visible. These are caused by coupling and cross-talk between interconnects or timing degradation due to power droop (IR drop). Since these defect mechanisms are not introduced during manufacturing, they are identified and corrected during the design phase.

6. Fitting Physical DFY in a Design Flow

DFY for physical defects is the most pervasive kind of pro-active yield enhancement activity being practiced today. It is the most understood form of DFM.

The earliest instance of physical DFY is the RET/OPC steps taken after the completion of design layout and verification (i.e., after tapeout). The RET/OPC process makes appropriate adjustments to the shapes of the polygons representing the poly of a transistor or the metal of a wire. For 180nm (and below) process technologies, this is now an essential step between design and manufacturing. To be sure, the adjustments to the shapes of the transistors and wires are changing the RC and hence the electrical characteristics of the design. For 180 & 130 nm designs, the changes have been insignificant, or have been limited, in order to not impact the operation of the design.

The success in RET/OPC opened the doors for more aggressive adjustments to the final layout of the design. Where possible, the wires were spread, metal jogs were eliminated, vias were doubled, enclosures were put around the vias and metal fills were added to ensure uniform metal density. Again, each of these physical adjustments affects the RC and consequently the electrical characteristics of the design. These changes are significant to sometimes impact the operation of a design negatively. Therefore, after these DFY adjustments to the final layout, the RC values are re-extracted and the design is put through timing verification. In many cases, the adjusted design fails timing which prompts easing off on some of the DFY adjustments until timing verification is successful.

Modern design flows have permeated DFY considerations into virtually every step of the design flow rather than only after the layout is completed. By doing so, timing verification is conducted concurrently allowing more opportunities for yield enhancement changes than ever before.

Physical DFY is implemented in the following steps of a chip design flow:

Design Rule Manual: For every new process technology, the process and design technologists get together and develop the Design Rule Manual (DRM). The manual consists of rules related to layout width, spacing and other physical characteristics that a design must follow in order to achieve viable yield.

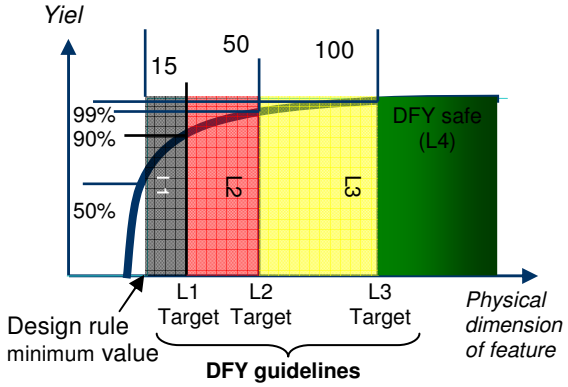


Figure 2: DFY Guidelines – Extention of Design Rules

An example of a Design Rule is a minimum spacing between two wires. When the spacing is increased the probability of defect due to a short is decreased. An example of a DFY guideline is: Achieve a minimum spacing of x units *greater* than the Design Rule minimum. Adherence to the DFY guidelines can be graded or scored by assigning levels to the amount of spacing provided between the two wires. While the example in Figure 2 shows 4 levels of DFY (L1 through L4), the future is headed towards abandoning the discrete levels in favor of simply providing the Yield vs Wire Spacing equation. Such an approach is called *Model-Based* DFY compared with *Rule-Based* approach common today.

For a 65nm process, over a hundred DFY guidelines have been developed – each having criticality and discrete levels that are based on its impact on yield. The format for DFY guidelines is typically kept to be the same as that for the DRM.

Deck Development: The DFY guidelines – just like the Design Rules – must be translated into a language that EDA tools can parse and interpret. This process is called *Deck* development and is a manual process today.

DFY Scoring: Specialized tools have been developed to score or grade yield-related indices such as Manufacturability and Improvability for a given layout. A DFY scoring tool uses the DFY Deck developed for the process technology and then reads in the layout of the library cell that is being scored. The scoring formula is weighted based on the criticality of a DFY guideline and the level of adherence to it. Scoring helps determine how far a given library cell is from the target and when the improvement activities can be considered completed. In future, scoring

formulas will be enhanced to include Electrical DFY considerations as well.

More and more semiconductor companies are setting a minimum DFY score that a library must achieve before it can be qualified for use on their SOC products.

6.1 DFY for Libraries

The manufacturing weak-spots and defect mechanisms are different for fabrication steps that are required for the transistors (Front End Of Line), versus those for the metal wires (Back End Of Line). The library cells are manufactured during Front End Of Line since they contain the transistors. The interconnection between the transistors in a library cell is often done with the use of a Local Interconnect.

The following eight techniques are the most common DFY corrections made during the design of the library cells:

(1) Adding Redundant Poly Contacts
(2) Adding Contact to Metal-1 Extensions
(3) Removal of Jogs in Poly or Metal
(4) Increasing Poly width over junctions
(5) Adding Redundant Active
(6) Increasing spacing between Active & Poly
(7) Adding Extensions to Poly Endcaps
(8) Adding Enclosures to Active Contacts

EDA tools are available that can modify a library cell in two modes. One mode modifies opportunistically, without increasing the area of the cell. The other mode uses DFY guidelines aggressively even if the cell area increases by a reasonable amount.

The latter – also known as Stretch-DFY cells, can increase the area of the cell by as much as 25%. For example, a stretch-DFY cell that uses 25 tracks (versus 20 tracks used by a normal cell) can reduce the probability of defect by 2/3rd and a cell that is increased to 27 tracks reduces the probability of defect by 4/5th [8]. Such an increase in library cell size may appear to negate any yield improvements – but it will be described how Stretch-DFY cells are used during the Floorplanning and Placement stages of SOC development (Section 6).

Lithography Simulation: The DFY guidelines related to Lithography equipment are also used by specialized tools that are able to analyze Litho variations in the layout. Layout adjustments can be made during library development in order to compensate for Litho variations.

Figure 3, shows a portion of layout of a library cell. The white borders show the layout as drawn and which passed all the Design Rule Checks (DRC). The structure shaded in green is what would actually be manufactured due to lithography limitations. The manufactured structure would not pass DRC. Finally the structure with blue border indicates the compensated drawn shapes so that the original (DRC clean) structure with the white border is printed during manufacturing.

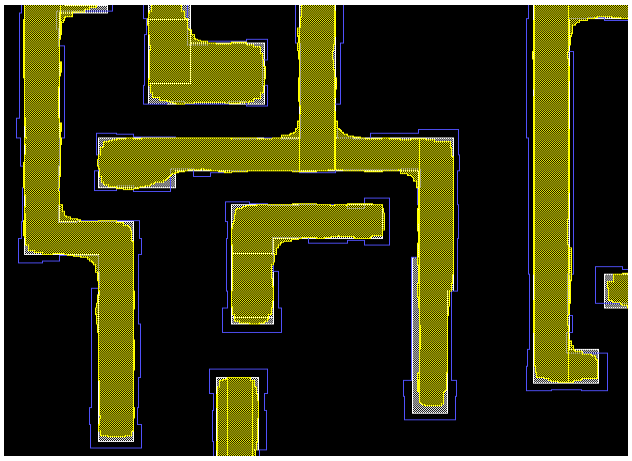


Figure 3: Lithography Variation. White - Original Drawn. Green - Manufactured. Blue – Corrected Drawn

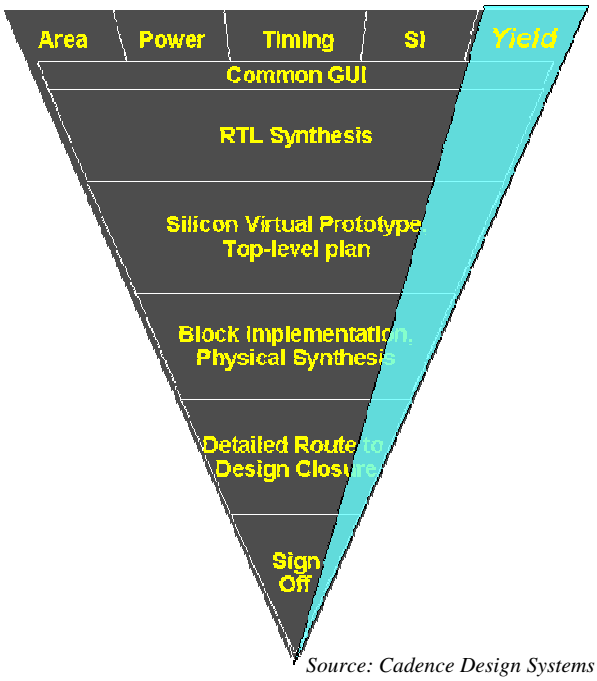
While correction for Lithography variation is commonly done during Mask Preparation stage (RET/OPC) [9], the advantages, of doing this during library development (i.e., concurrent timing closure), are leading EDA vendors to integrate this capability into the library development and migration tools [10].

6.2 DFY during SOC Design

A generic SOC design flow is shown in Figure 4. In the past, the process of SOC design involved finding the right optimization between Area, Power, Timing and SI - in order to meet the design objectives of the SOC. The fifth cost function element – Yield has been added recently and the EDA industry is integrating Yield considerations into every step of the SOC design flow.

Architecture: DFY considerations begin at the architecture stage of a chip development. Some common forms of ad-hoc DFY enhancements are – Adding Redundancy in embedded memory and adding ECC to major buses. More recently, chip architects are factoring yield consideration into deciding if a new product will be implemented with the use of microprocessor/memory alon with software algorithms, or dedicated hardware.

RTL Synthesis: In this SOC design step, the Register Transfer Level (RTL) representation of a design is synthesized into gate level using the corresponding gate-level library of the standard cells. Timing, Area, Power & Signal Integrity (SI) have been the four important cost functions that the tool's algorithms have considered during the synthesis process. Now Yield has been added as a cost function that a user can dial in for appropriate yield optimization as well. Each library cell has a DFY score associated with it. Whenever a choice is available to the tool during the synthesis process, the DFY score is used as the arbiter rather than a random pick.



Source: Cadence Design Systems

Figure 4: Yield – the fifth element of Cost Function

Silicon Virtual Prototyping: In this SOC design step, the library cells are placed within the design blocks and the blocks are placed within the SOC. Industry observations are that the area of a design block is set by the area required for routing wires between the library cells and not by the library cells themselves. In other words, as the congested metal layers set the area required by a design block, there is empty area at the library cell level. This observation has been harnessed into an important DFY opportunity. The library cells can be replaced, with bigger library cells that are very high yielding, to the extent that the total area required by the library cells still is within the area required by the metal layers. This step is called "cell swapping". The floorplanning tool is "aware" of this opportunity and attempts to maximize the use of high-yielding bigger cells where possible.

Detailed Routing: There is particular difficulty in manufacturing via structures. As a result, a significant percentage of defects are traced to via failures. DFY to reduce via failures has the following components:

Via Reduction: The routing tool is made aware of Via issues. The algorithms utilize this information to minimize the number of vias.

Via Redundancy: The Routing, Chip Optimization & Physical Verification tools attempt to insert an additional via without increasing the area of the chip. The tools are sophisticated and are able to move neighboring wires around and creatively find room for the additional via.
Via Enclosure/Extention: Inserting an additional via is not always possible without increasing the chip area or impacting the timing negatively. In such cases, the tools attempt to put an enclosure or/and extension around the via. These methods are known to reduce via failures.

Due to the visibility caused by the via failures, this is the most popular DFY technique in use today.

Shorts between adjacent wires and *Opens* in wires are other leading cause of chip failures. The specific methods used in the EDA flow are:

Wire Spreading: As the term implies, the tools attempt to spread wires around without increasing chip area. This step is performed during Routing, Chip Optimization and Physical Verification stages. The wire spreading tool is usually provided a list of critical nets. The wires around a critical net are prevented from coming closer to the critical net even if there is an opportunity to do so.

Wire Thickening: The tool attempts to increase the thickness of wires where possible. A thicker wire has reduced possibility of an open defect. A user can provide the tool a list of wires that must not be processed. These may be wires whose speed-up may result in hold time violations.

Wire Straightening (or Jog Elimination): Bent wires are particularly prone to greater lithography variations. Therefore, the tool attempts to eliminate bent wires where possible.

Industry observations are that wire spreading is providing marginal yield improvement benefit. Early speculation is that the defect density for shorts is much less than for opens in Copper Damascene process technologies [11].

Chip Optimization & Sign Off: After the detailed routing is completed, the impact on timing due to RC (also known as extraction), due to Noise and due to IR-Drop can be accurately assessed. Indeed, several set-up and hold violations are reported after the Extract/Noise/IR-Drop steps. Instead of going back to the synthesis step in order to make compensatory adjustments – these small adjustments are made to the routed design database. This process is also called Post-route optimization, Chip Finishing, or In-place Optimization. The turn-around time for each loop of timing iteration is reduced to hours from days.

The chip optimization step also turns out be ideal for making DFY guided enhancements to the layout of the design. The major DFY enhancements during this step are: Via Optimization, Wire Optimization, Metal Density Uniformity and several miscellaneous DFY fixes (such as antenna corrections).

While there is overlap between the DFY functions carried out in the Detailed Routing stage and the Chip Optimization stage, industry experience has found that a prudent use of DFY in both steps results in maximizing DFY improvements on the design. As an example, the router may be able to optimize 60% of the Vias in a design without increasing the chip routing time unreasonably. The chip optimizer then optimizes 25-35% of the remaining Vias that may have been difficult to optimize during the routing stage. Leaving all of Via optimization for the chip optimization stage does not allow much time in the design flow for another synthesis run should re-timing be required after Via optimization. On the other hand, during the detailed routing stage, re-synthesis is quite possible should it be required.

The variation in density of metal, that is used for wires in the chip, causes issues during the CMP process (Chemical Mechanical Polishing) [12]. On a given metal layer, when there is a dense set of metal wires with open spaces around it, the CMP process applies uneven pressure during polishing. This can result in an uneven polish and/or higher quantities of leftover abrasive material causing defective manufacturing. In order to compensate for this, dummy metal structures are added in the open spaces during the design phase in order to create an even density of metal. This step is called Tiling or Metal Density correction. Older DFY tools performed this step after the layout was completed. Lately, the capacitive coupling effects between the added dummy metal tiles and the real wires, have known to cause timing issues and chip failure. Therefore, today this step is performed during the Chip Optimization step prior to final timing signoff – thus allowing adjustments to the shape and location of the metal tiles – as needed. In addition, the routing tools are now beginning to add "awareness" of desiring a uniform metal density in their routing algorithms. The routing tools try to arrange the layout with an attempt to maintain a uniform metal density – thereby reducing the need for dummy metal structures.

Physical Verification (LVS/DRC): After chip optimization, the Layout Versus Schematic (LVS) comparison is performed and Design Rules are Checked (DRC) on a flattened layout of the design. Earliest DFY methods were deployed during this stage. The two common techniques – doubling vias & metal density uniformity – are still common at this stage of the design flow.

While doubling vias has been successful in 180 and 130 nm technologies. The technologies below 90 nm require more than via-doubling and even via doubling is now having an impact on chip timing because of the capacitive effects of the added via. At this late stage of a design flow, it is difficult to make timing corrections. Similar issues are being experienced with Metal Density Uniformity which is now done in Chip Optimization stage along with "density" aware capabilities in the Router.

There are advantages in performing DFY corrections during the Physical Verification stage - when a flattened layout for the full chip becomes available. One example is illustrated in Figure 5. Litho Simulation for the library cell located a potential short in the circled area.

However, when the EDA tool analyzed the entire layout, it turned out that the metal structures close to each other belonged to the same electrical net (Figure 6). A short between these metal structures would not result in chip failure. Therefore, no DFY correction was necessary.

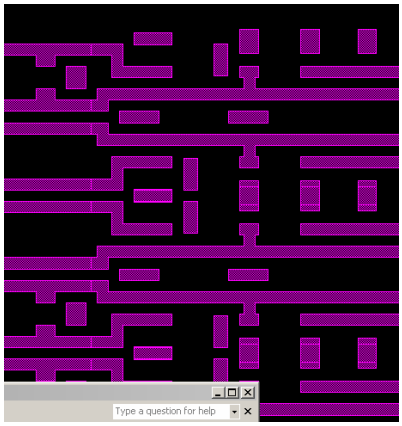


Figure 5: Local Litho Simulation locates a potential short *(courtesy: Mask Services, Freescale Semiconductor)*

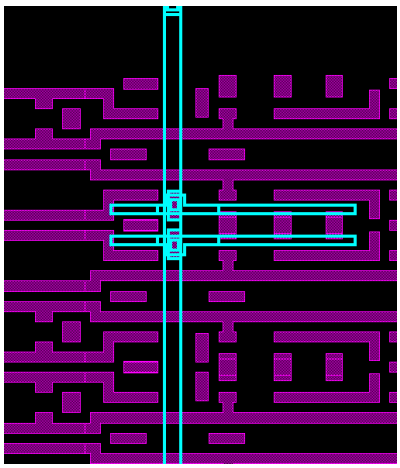


Figure 6: Full chip analysis reveals same electrical net

It turns out that such instances are frequent. Global signals and clocks have large fanouts. Electrical connectivity analysis – which is done most effectively at full-chip level can detect such false alarms and prevent unnecessary modifications to a design.

While, DFY enhancements will continue to be made at this late stage of the design, the industry direction is moving towards addressing DFY opportunities as early in the design flow as possible.

7. Electrical DFY

As described in Section 3, variations in equipment and chemical mixes, that are used during the manufacturing process, can result in corresponding variations in the composition of transistors, vias and wires – leading to chip failure at operating conditions. Since the defects are not visible but do affect the electrical operation of the chip – these are now being referred to as electrical defects.

Electrical DFY has been practiced by the design teams on an ad-hoc basis for a long time. One example is the correction in transistor sizing in order to reduce the mismatch in the offset voltage control of differential amplifier designs.

The need for an organized DFY effort is now being felt. The following early methods are being practiced in the area of Electrical DFY.

- The P/N ratio of the transistors in a gate are adjusted in order to improve electrical performance and hence margin against the defects.
- The use of M2 metal layer for clock signal inside a Flip Flop cell improves the signal integrity and lowers the power consumption.

- Multiple vertical tracks are made available in a library cell for connection to output. This step improves the electrical performance & margin.
- Using the M1 metal layer for routing power supply – in addition to using M2 for power and ground – reduces coupling cap thereby improving the power grid.
- Selectively replacing library cells with longer gate length transistors (slower but with less leakage variability) along non-critical timing paths of a design. Chip frequency remains intact while leakage variability & hence yield improves.

Electrical sources for defects will continue to increase. Therfore, in addition to physical DFY (Section 6), Electrical DFY is also expected to become a standard consideration during the chip design flow.

8. Relation between DFY & DFT

Figure 7 shows the design and test flow for a chip. The design flow is guided by DFY guidelines. As explained in Section 6, the Design Rule Manual (DRM) is the basis for DFY guidelines. The DRM, in turn, is developed through carefully designed Test Chips. Additional inputs for the initial DFY models are obatined through (a) interviews with Process/Device engineering experts, through Yield Models and (d) Critical Area Analysis (CAA). Despite the various sources of inputs, the initial DFY models still represents only the best guess at the time a new process is deployed. Test results can help refine the DRM & DFY guidelines. The improved DFY guidelines can thus be deployed for use on subsequent chips designed in the same process technology. It may be noted that chip designs, for various reasons, may not be able to implement all the DFY guidelines.

On the test generation front, our industry started off with gate-level netlist-based stuck-at fault model. The stuck-at tests are still used, but now they are being supplemented with tests that are based on (a) Timing (i.e., Path Delay and TrueTime) and on (b) Layout (i.e., Bridging). The DFY guidelines that remain unimplemented or incompletely implemented, will become an effective source for generating and prioritizing the tests.

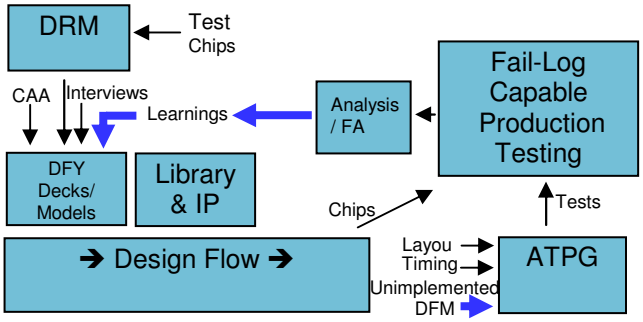


Figure 7: The relationship between DFY & DFT

A complete loop of the Process, Design, Test & Diagnosis flow will work as follows - For a new process technology, the initial DFY models may well be developed through ad-hoc methods, but the corrections and refinements will happen using the diagnostic results obtained from production testing of the earliest chips using this process. The diagnostics results will also update the Yield score for the library cells. With the updated DFY guidelines and enhanced library cells, along with accurate DFY scores for each cell , the subsequent designs will use DFY and IP maturity guidelines more accurately, thus producing higher yielding chips. The ATPG process will use unimplemented DFY as another source of input for test generation and prioritization.

When the DFT and DFY efforts are harmonized, it is possible to improve product quality and yield at the same time. Several chip design houses are using portions of the DFY-DFT loop, however an integrated DFY-DFT flow is not available from commercial EDA vendors yet – although several are working towards it.

9. Future Challenges – Gaining Adoption

DFM/DFY, though practiced ad-hoc for decades, is now becoming recognized as an organized and accountable activity in the chip design flow. However, it needs to become an integral part of a chip design flow just like frequency (timing) and die-size is. There are several challenges that we must deal with:

- There is no consistency in the industry on what the acronyms DFM and DFY should cover. Standardization of the terms and their scope will help us make progress faster. Standard bodies such as IEEE and ACM can provide help.

- There continues to be resistance from the chip design community to accommodate DFY considerations at every step of the design flow. The main reason is that the design teams are not resourced and scheduled well for the extra people/time/compute that the DFY steps require. The extra resources need to be driven from business considerations. At the same time, EDA vendors can play an important role by integrating DFY steps completely and seamlessly into the mainstream chip design flow. In this context, the use of Open Access (OA) standards is expected to gain acceptance [13].

- Rule based approach towards Design Rules and DFY guidelines is running out of steam. A model based approach is more accurate and efficient. However the EDA infrastructure is not available today and its deployment logistics is not well-understood.

- Yield loss due to electrical variations is becoming significant. Therefore, the electrical DFY flow must be developed and integrated into the mainstream EDA flow just like what has been accomplished for physical DFY.

- Design Rules must be updated using Diagnostic results from production runs for a given process technology.

Test Generation must be guided by unimplemented DFY. EDA help is needed in making the Process, Design, Test & Diagnosis loop seamless.

The challenges listed above are not easy to resolve. In order to make faster progress an industry-wide DFY coalition is needed [14]. This coalition is comprised of 4 groups: (1) Chip makers; (2) Foundries; (3) EDA Vendors (4) Foundry Equipment Suppliers. The coalition is establishing terminology, standard formats for information exchange and common infrastructure that is required to facilitate development of DFY methods and their use on chip designs – while not stifling innovation from each of the competing parties.

10. Conclusions

Design For Yield has now been recognized as an activity that must be well integrated in the mainstream design flow. Several of the DFY elements have already been integrated into the various steps of a design flow. The key areas that are integrated today are all under Physical DFY – Via and Wire Optimization, Metal Density Uniformity and Cell Swapping. However, the usage of existing elements is not widespread and DFY integration into the design flow is not complete yet. Key areas that need to be integrated are Electrical DFM, Model-based Guidelines and DFY/DFT interlock. Especially, the area of DFY/DFT interlock, when fully harnessed, can bring very tangible advantages to the semiconductor industry and could become instrumental in sustaining Moore's Law. On the positive side, DFY is an area that allows incremental benefits from incremental efforts. It is not a *must do it all or else get nothing* situation. Therefore, a chip design team can begin practicing even a single element of the multi-faceted DFY universe and realize improved quality and yield for their chips starting today.

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