Fitting DFM in Your Design Flow

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Purpose

- Clarify the buzz words – DFM & DFY
  - The origins of DFM
  - Relationship between DFM & DFY
- Explain the business significance
- DFM Methods in use today
  - Where the methods are used
  - How the methods are used
- Future DFM Challenges & Opportunities

Outline

- DFM Origins
- How DFM is understood today
  - Taxonomy & Terminology
- DFY in Practice
  - DRM, Metrics, Measurement
  - DFY in Libraries
  - DFY in SOC – RTL Synthesis, Place & Route
  - DFY in SOC – Chip Optimization, LVS/DRC
- Future DFM Methods
- Conclusions

Acknowledgements

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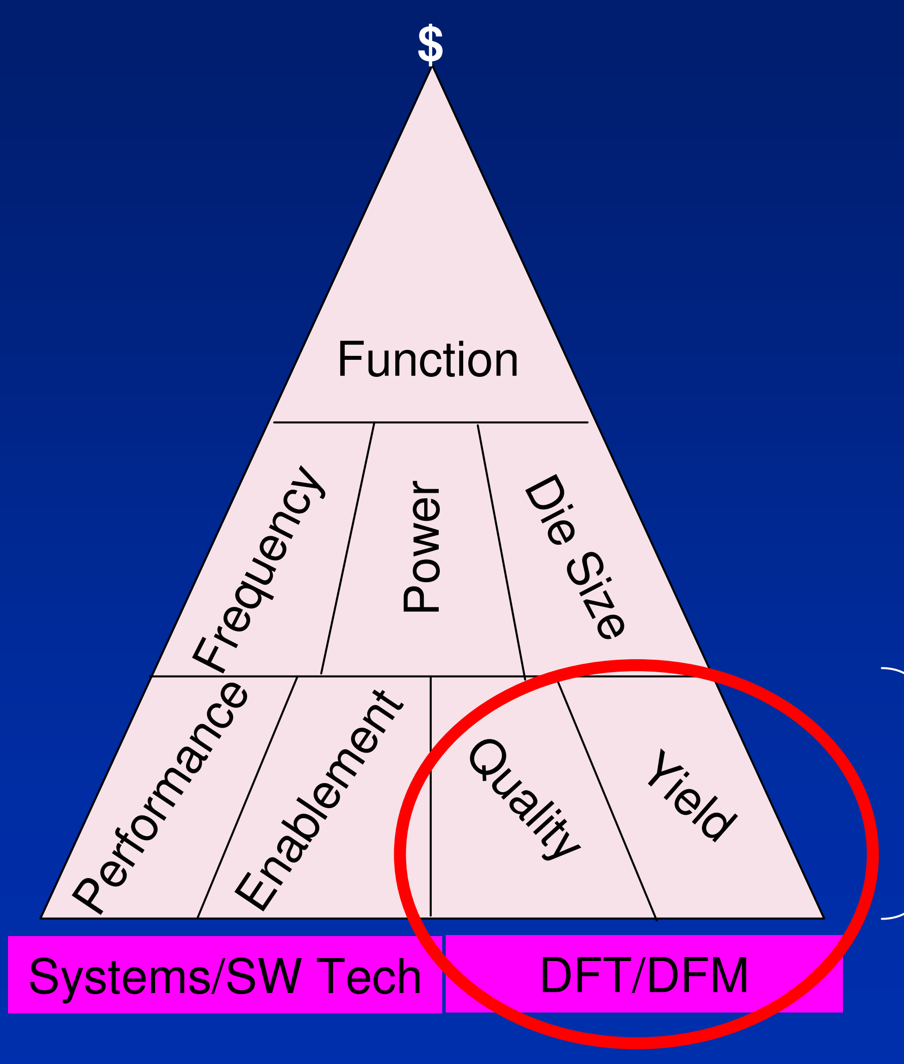
- Business Groups: Chris Ahrens, Ezra Baruch, Mahboob Rashed, Tom Thomas, Ravi Vaidyanathan, Jeff Warner, Michael Zimin
- Mask/Mfg/Libraries/Fabs: Jonathan Ellis, Andy Espenscheid, Claude Moughanni, Kyle Patterson, Brad Smith
- Management: Joe Pumo, Ross Hirschi, Suresh Venkatesan, Dirk Wristers
- EDA Vendors: Cadence Design Systems, Mentor Graphics Corporation

Selling a Chip – What to consider during design



1. ELIMINATE Defects by Design (DFM)
2. DETECT Defects by Design (DFT)

Design Technology Differentiators

Timing	Power	Die Size
Pass gate Muxes	HVT Cells	High Density Cells
Pipelined Architecture	Power Domains	Common Fuse Processor
Lookahead Adder	Gray code Counters	Scan Reset
Timing-Aware Placement	Clk Gating	Logic Optimization

Library Dev

SOC Arch

Logic Design

Physical Design

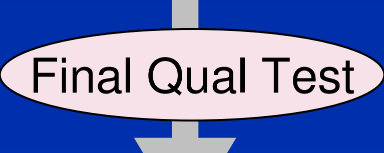
Mask Prep

Fabrication

Probe Test

Package

Final Qual Test

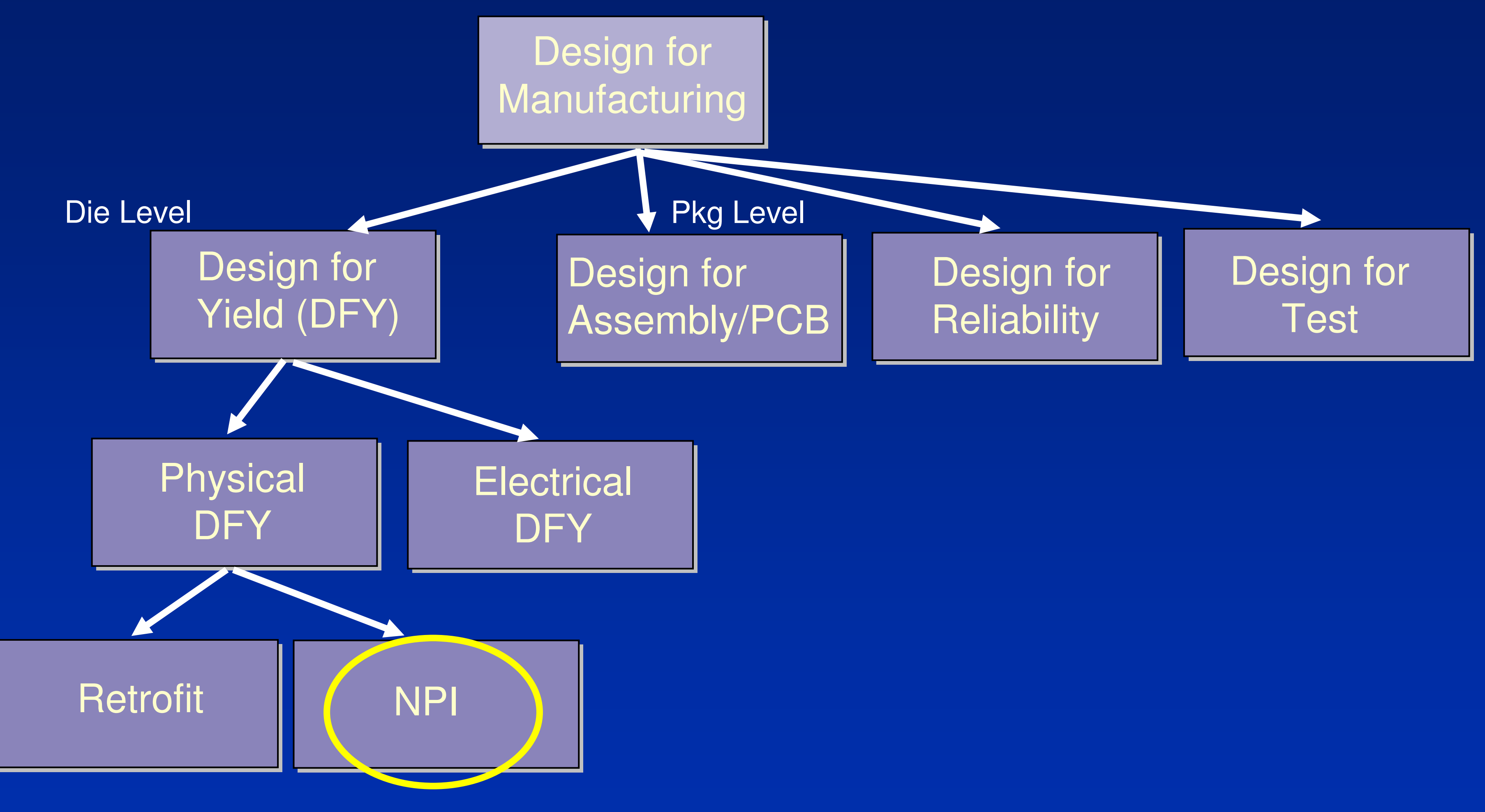


Perf	DevTech	Quality	Yield
Complex Gates		Test Pulldown	DFM guidelines Litho Sim
Multi-Core	HW/SW Co-design	IEEE 1500	Memory Redundancy
Multi Threading	JTAG	MBIST	IPmaturity
	Logical to Physical Map	Scan	Via/Wire Optimization
			RET/OPC
		DFT	DFY

Points to note:

1. No single magic DFM bullet !
2. DFM opportunities in every step of design
3. Each opportunity provides incremental return

Performance, Quality, Cost
Must be permeated in Design Flow

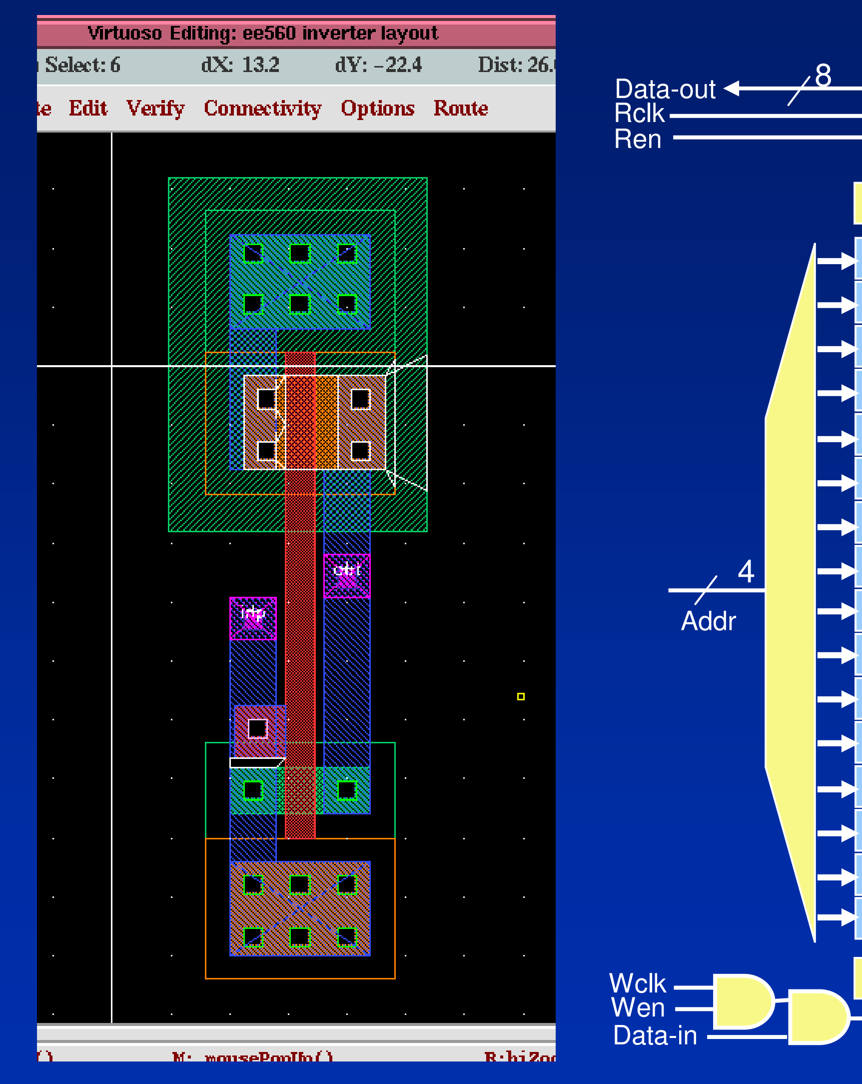

The World of DFM
Design for Manufacturing
Die Level
Pkg Level
Design for Yield (DFY)
Design for Assembly/PCB
Design for Reliability
Design for Test
Physical DFY
Electrical DFY
Retrofit
NPI

Techniques for Improving Yield

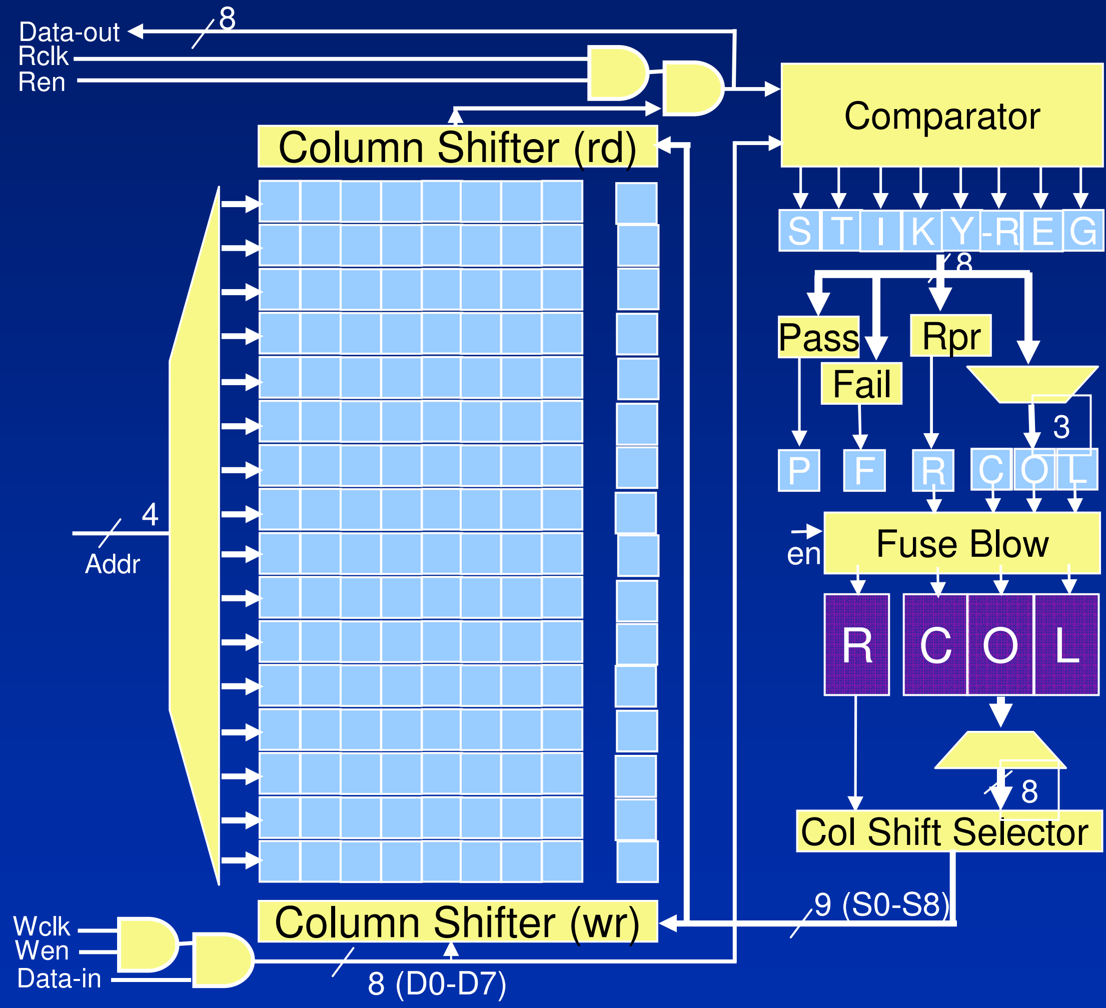
Defect source	Description	DFY Countermeasures
Random Physical	• Metal/poly shorts and opens • Contact/via voids • Missing or extra pattern • Stress cracks	• Increase poly pitch and spacing to contacts • Contact/via redundancy and reduction • Wire widening and spreading • ↑ area of metal/active islands
Device variation	• L_{eff} variation (gate length, dopants, oxide thickness) • Devices not matching models due to local layout (stress, well and pattern proximity)	• Rule-based changes to layout to mitigate proximity effects (poly and active corners, poly pitch, contact spacing to gate) • Statistical device & timing models
Lithography capability & variation	• Small focus/exposure window • Bridging and pinching • Corner rounding and pullback • Overlay errors	• Lithography simulation (using OPC model) to find & remove hot spots • Jog elimination • Via enclosure optimization
Topography due to CMP	• Non-planar topography due to pattern density variation • Dishing & erosion • Oxide thickness	• Rule-based tiling • CMP–model-driven tiling and extraction

Source: Scott Hector

DFM is not new

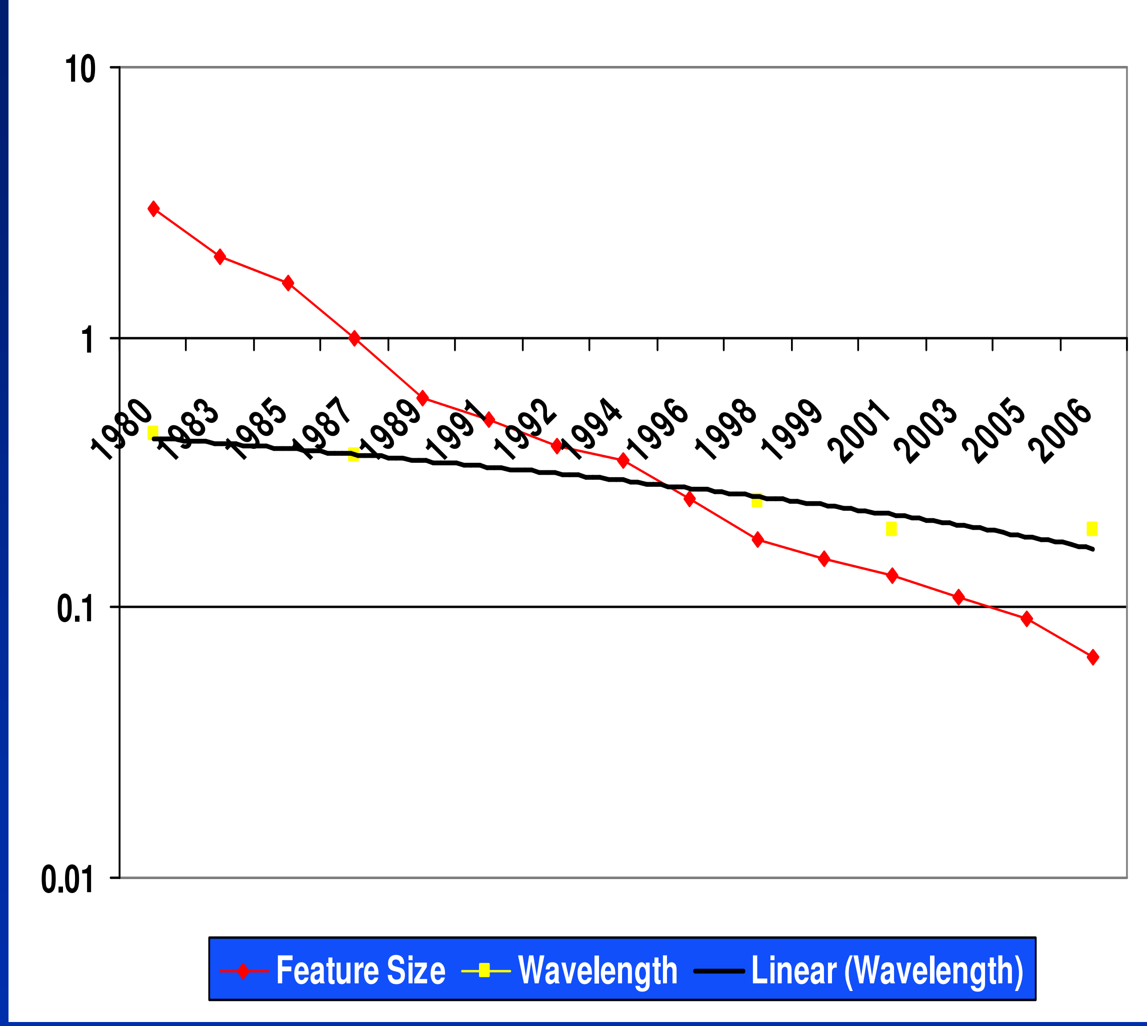


DRC



Column Redundancy

DFM – Why the *Buzz* now ?

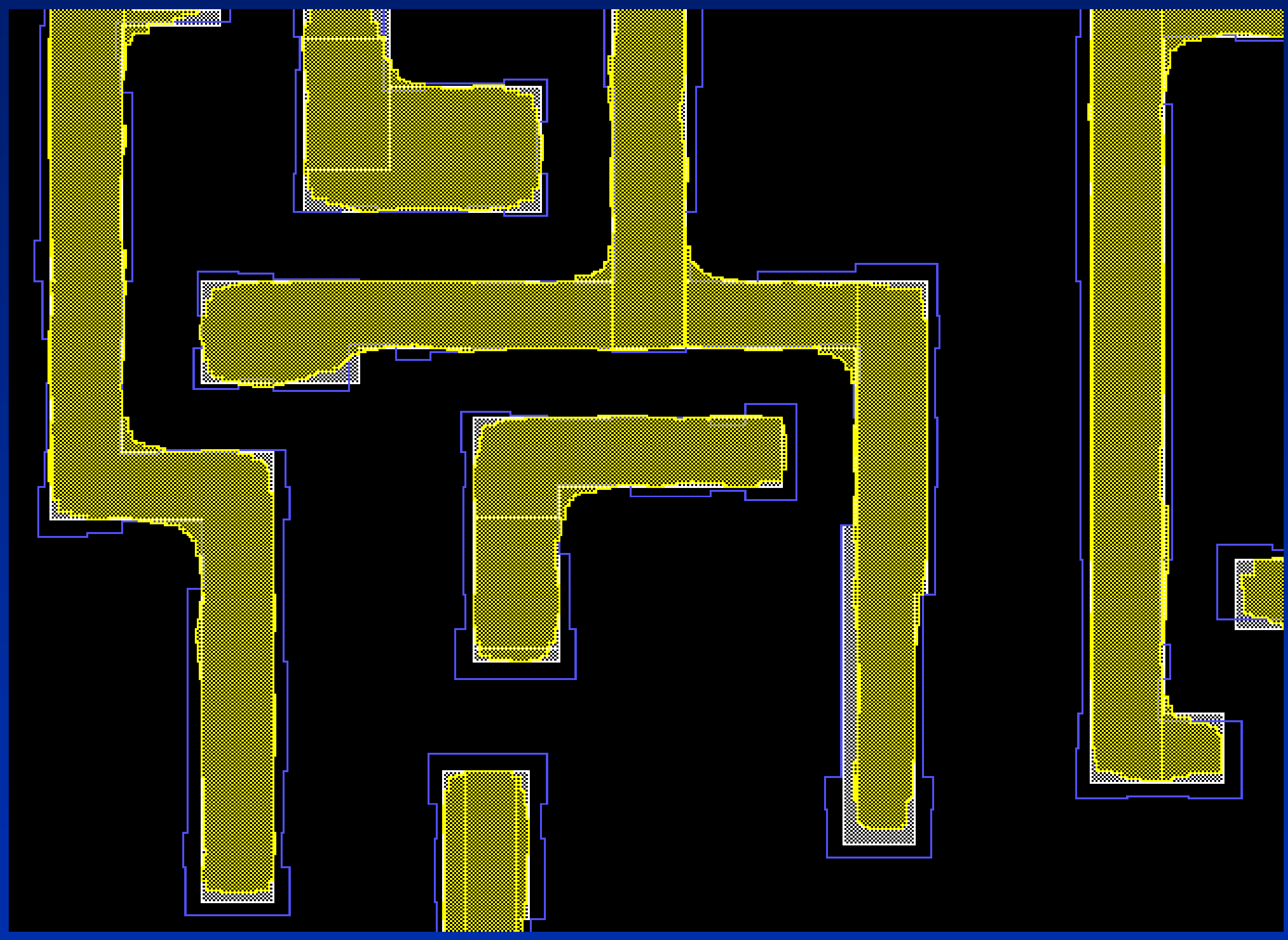


193nm Stepper

Courtesy: ASML

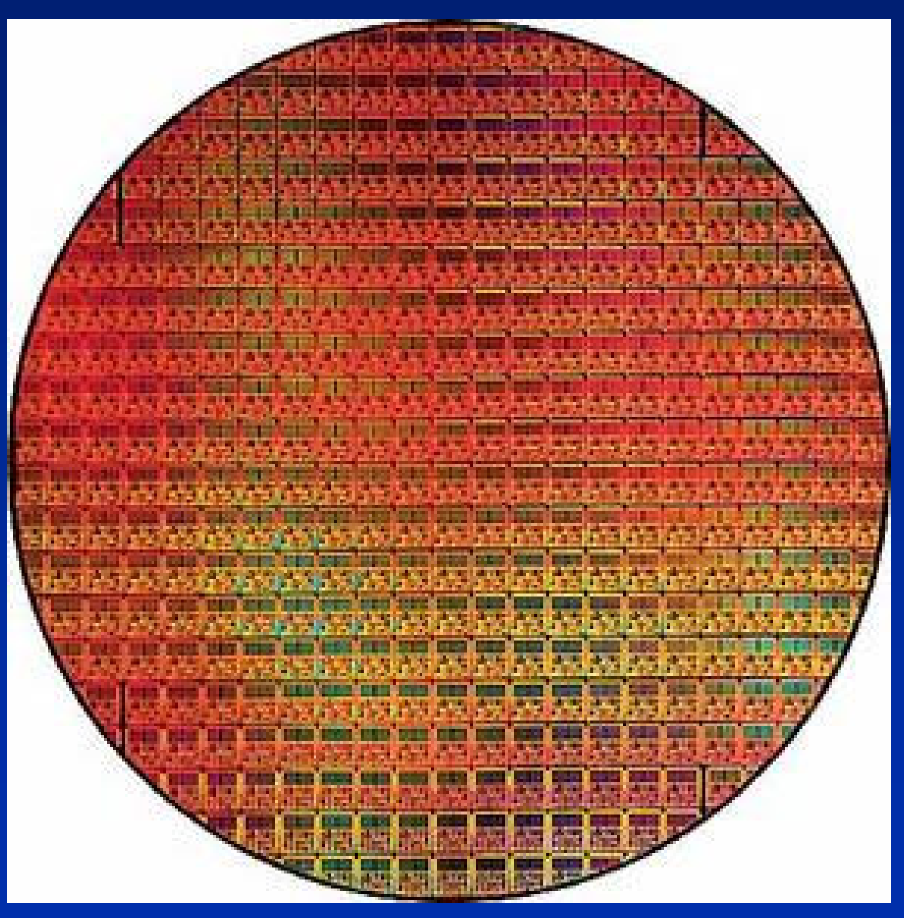
Feature Size Smaller Than Wavelength

DFM – Lithography Variation



White - Original Drawn. Green - Manufactured. Blue – Corrected Drawn

DFM – Business Case



Process: 90nm Bulk
Layers: 6
Masks: 26
Wafer Size: 300 mm

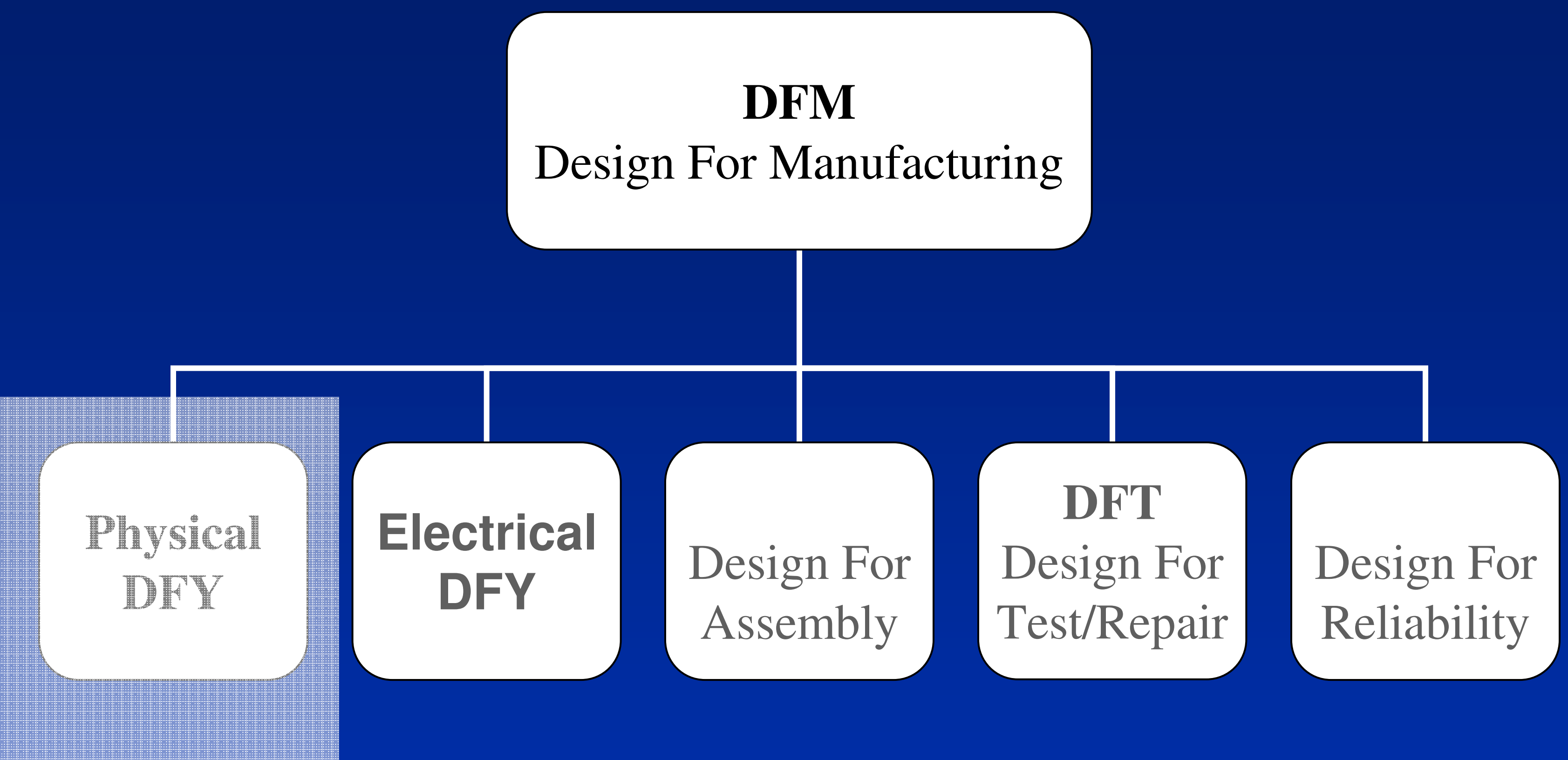
Wafer Cost: $3030
Wafer Sold: $5000

Volume: 30K/month
Yield Increase: 1%

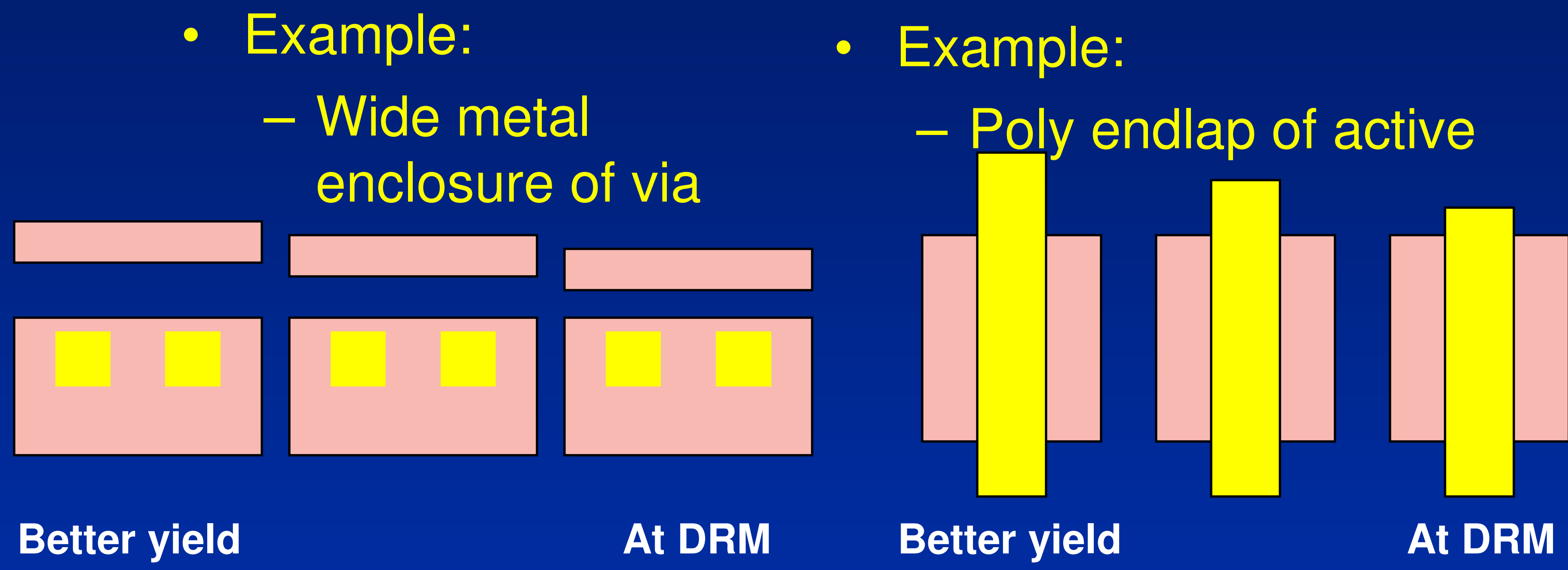
Revenue increase:
$1.5M/month

Test Coverage: 99%
DPM improvement: 7%

DFM and Physical DFY



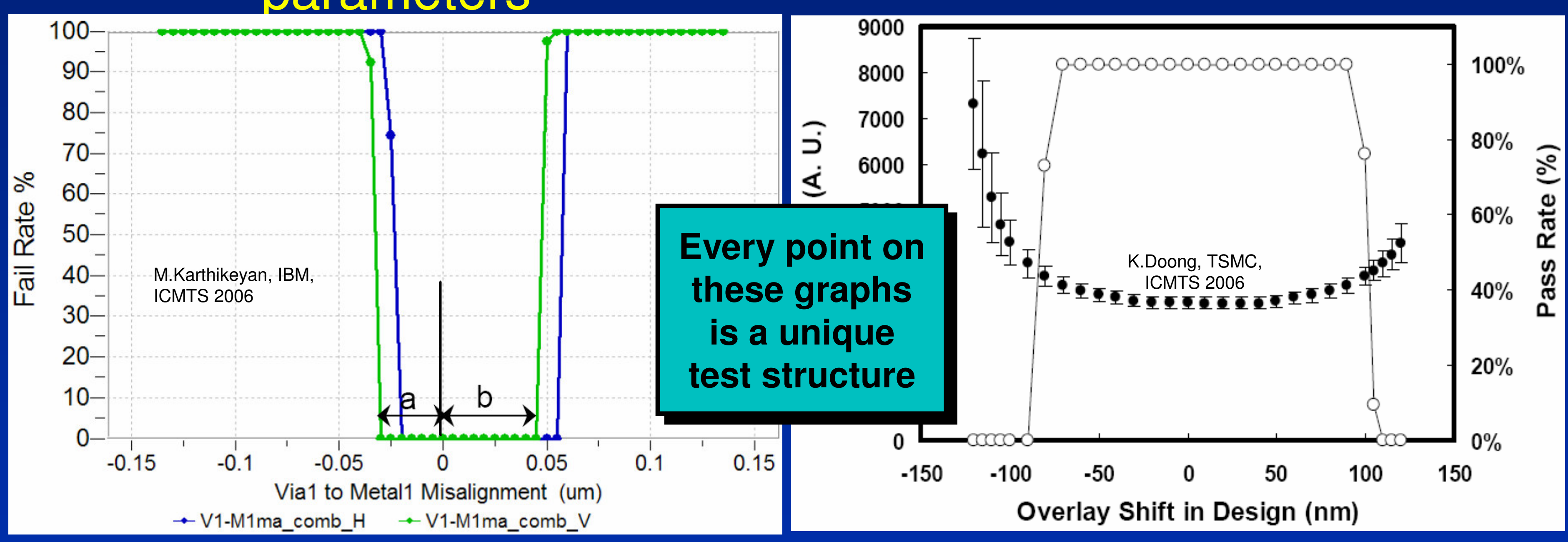
DFY Test Vehicles – Examples



Courtesy: Technology Validation Group, Brad Smith

DFY Test Vehicles – Reporting

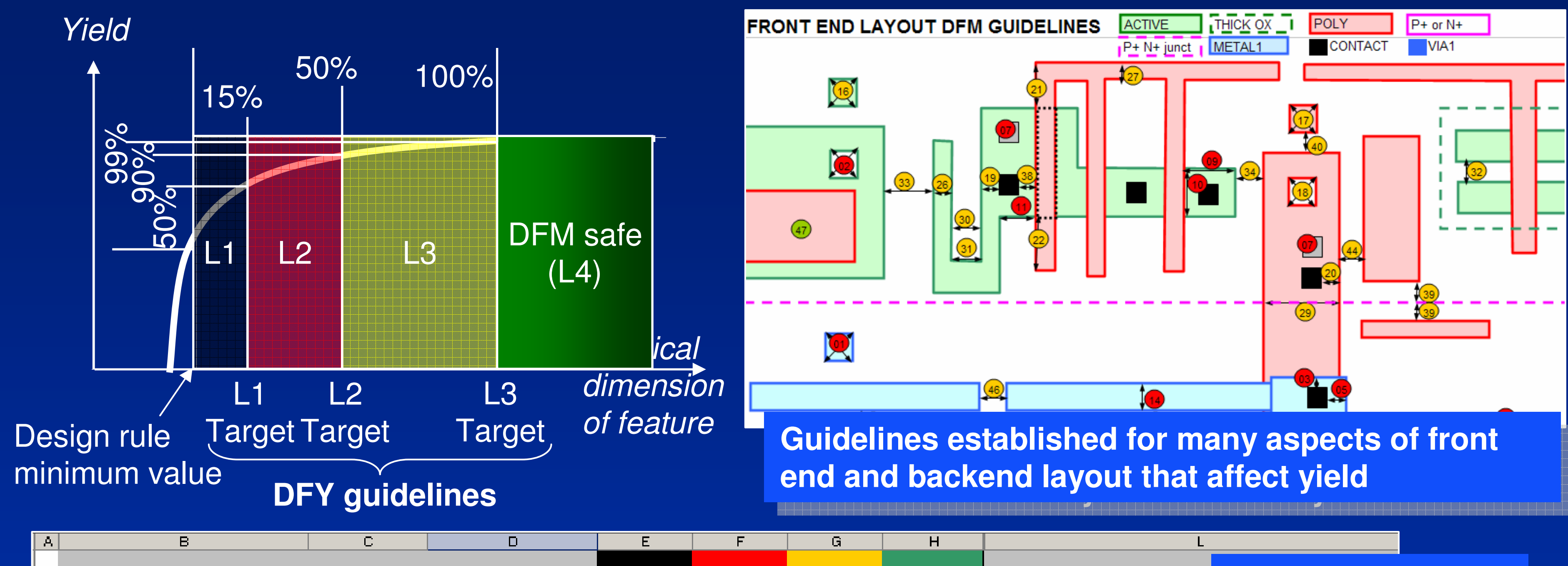
- Manual reports
  - Graphs showing yield as a function of one or more parameters



- Yield modeling
  - Table to feed yield models

Courtesy: Technology Validation Group, Brad Smith

DFY in Practice – DRM, Metrics

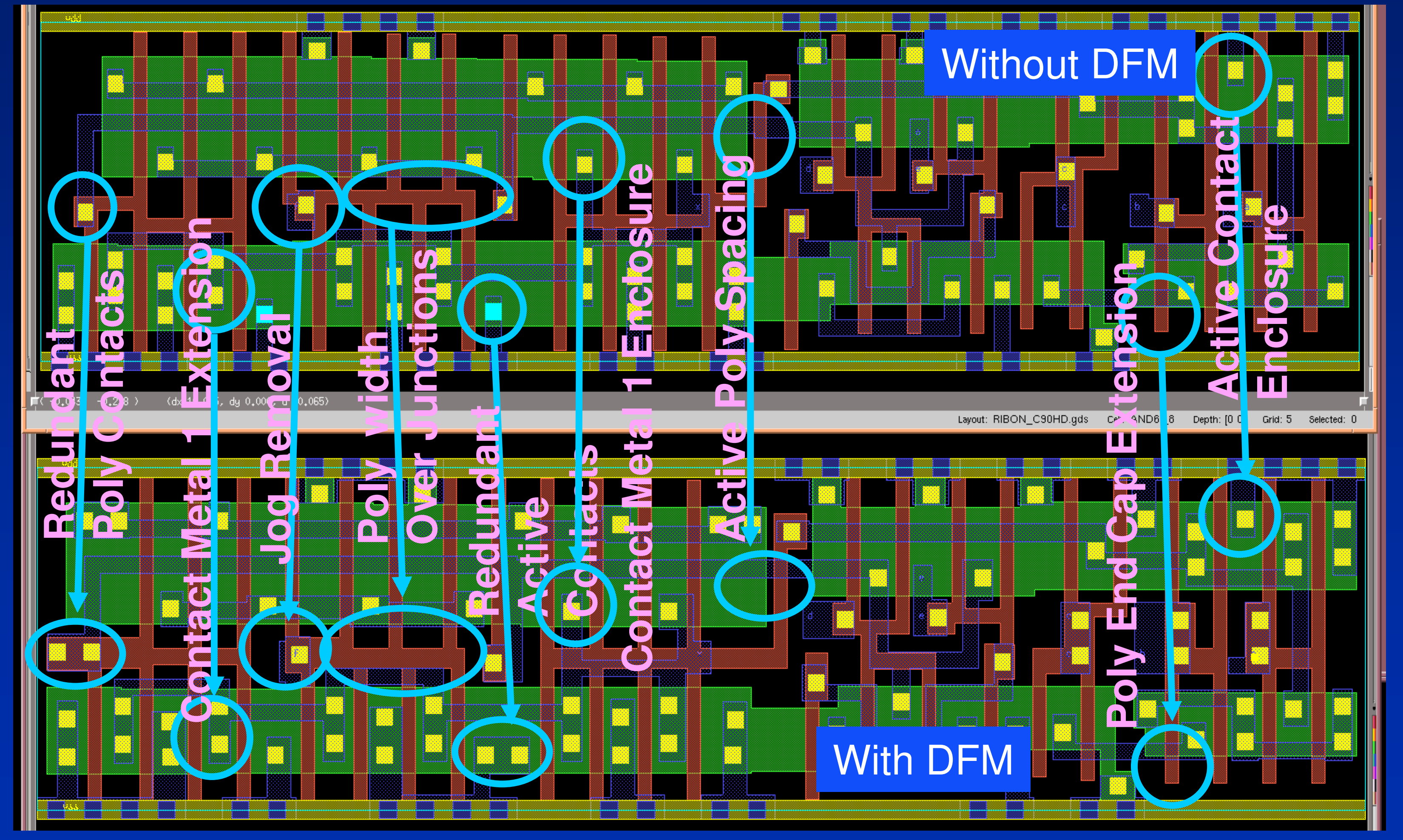


Re	Naming	Rules Criticality	DRM reference rules	L1	L2	L3		Comments
			Min Area					
1	AR1_M1	1 HC	M1.A.1	0.042	0.046	0.050	0.060	
			Min enclosedArea					
2	AR3_OD	1 HC	OD.A.2	0.085	0.093	0.107	0.200	
			Via/Contact Min enclos					
3	EN1_M1.CO	1 HC	M1.EN.1	0	0.005	na	0.01	Applies only on single transitions
4	EN1_M1.VIA1	1 HC	VIA1.EN.1	0	0.005	na	0.01	Applies only on single transitions
			Via/Contact Min enclos					
5	EX1_M1.CO	1 HC	M1.EX.1	0.04	0.045	0.05	0.06	Applies only on single transitions with Enclosure M1.Co < 10nm
6	EX1_M1.VIA1	1 HC	VIA1.EX.1	0.04	0.045	0.05	0.06	Applies only on single transitions with Enclosure M1.V1 < 10nm
			Redundability					
7	RE1_CO.OD	1 HC	Double if possible, with back up as far as possible	1x	na	na	2x	
7	RE1_CO.PO	1 HC		1x	na	na	2x	
8	RE1_VIA1	1 HC		1x	na	na	2x	

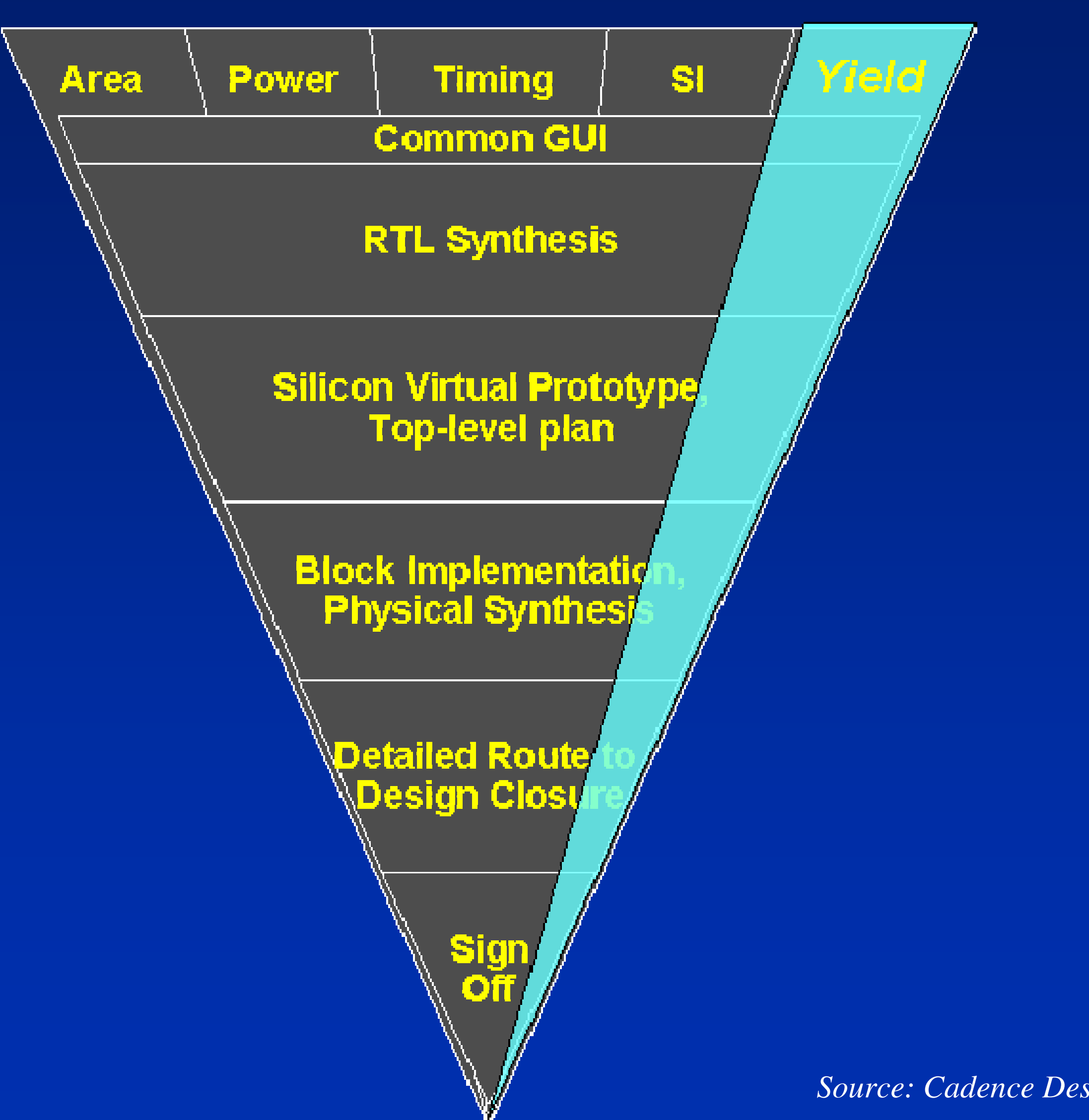
Example of guidelines values

Source: Lionel Riviere-Cazaux

DFY in Practice - Libraries



DFY in Practice - SOC

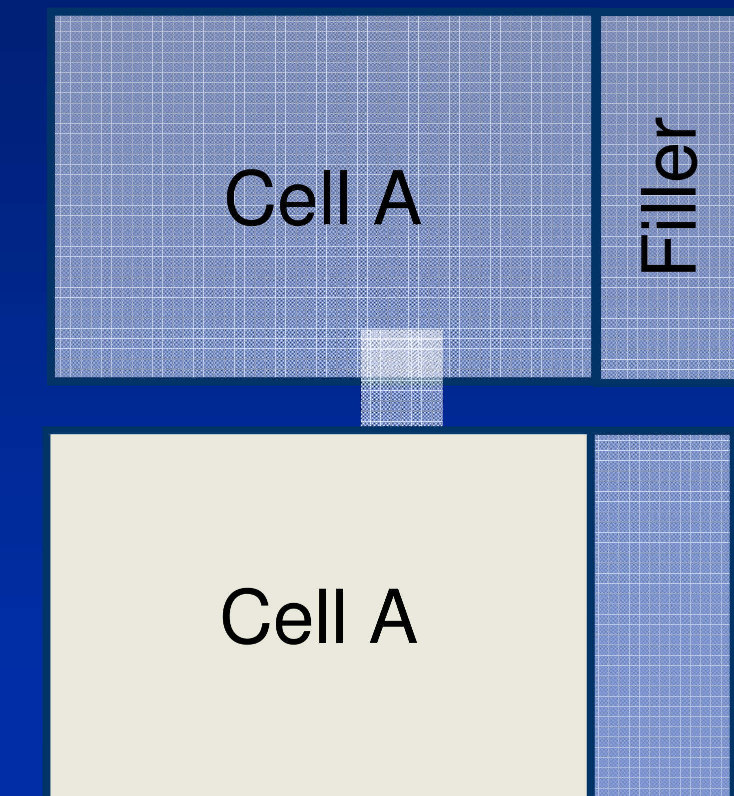


Source: Cadence Design Systems

DFY in Practice - Stretched StdCells

Place & Route blocks use up to 30% filler cells

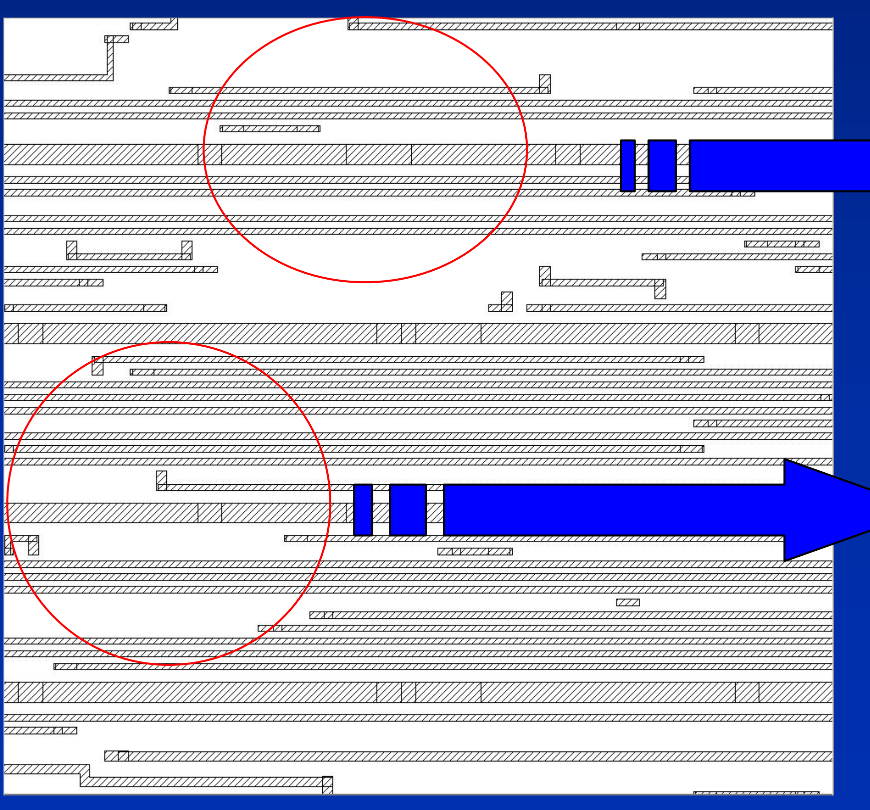
Swap regular cells…

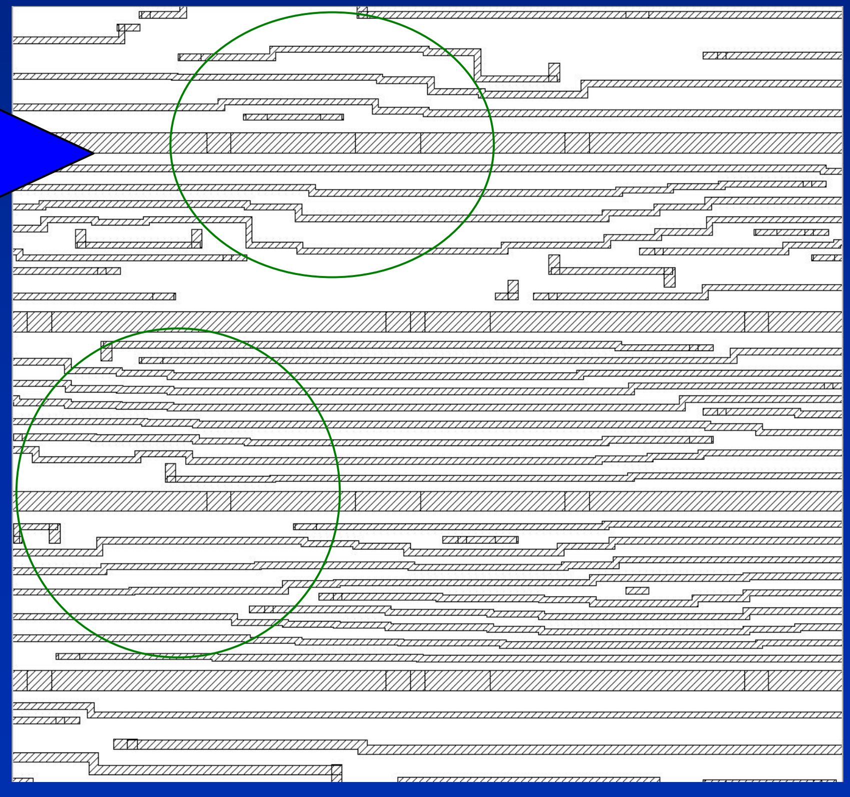


…by stretched cells

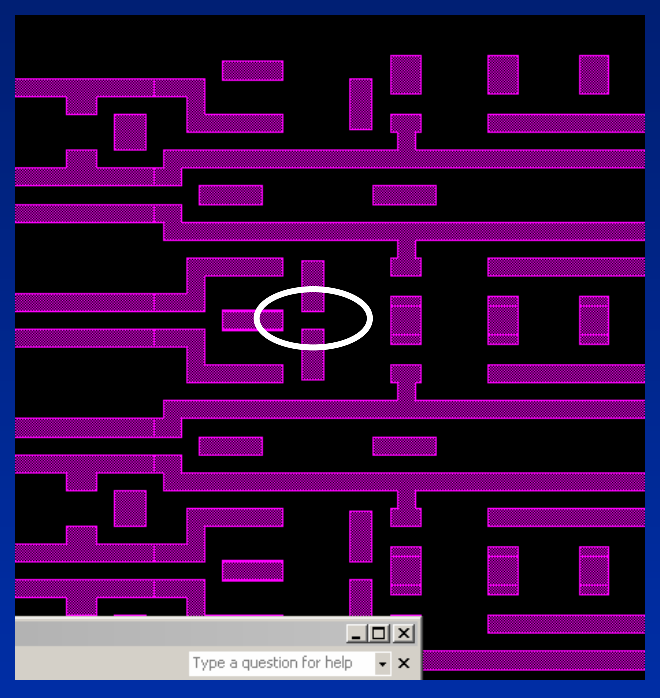
DFY in Practice - Wire Spreading

- Wire spreading goal is to seek congested minimum space areas and spread the wires to reduce shorts.





DFY in Practice – Avoiding Overkill

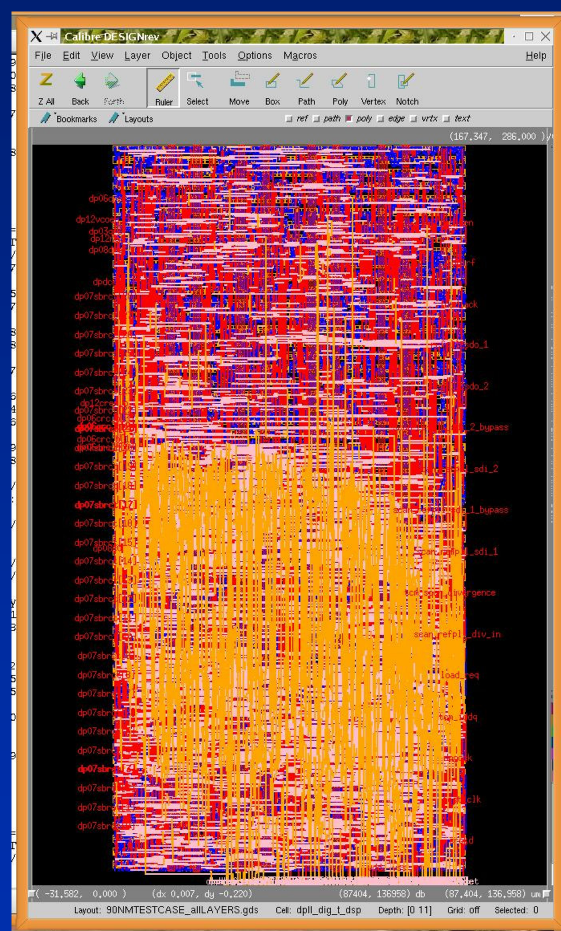


Potential Bridging?

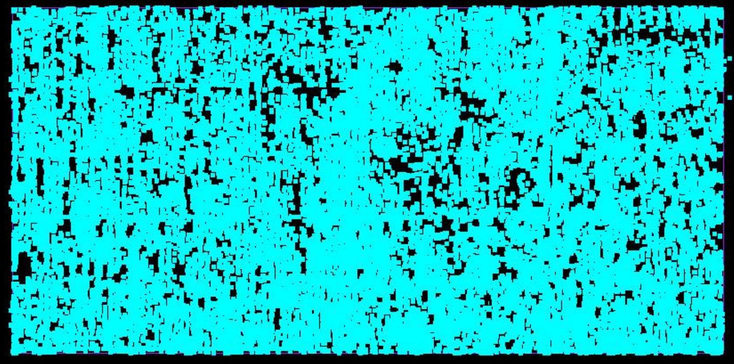
Same Electrical Net

Source: Andy Espensceid

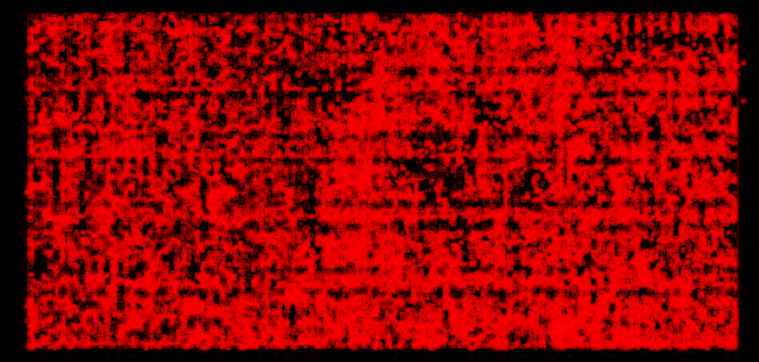
DFY - Results



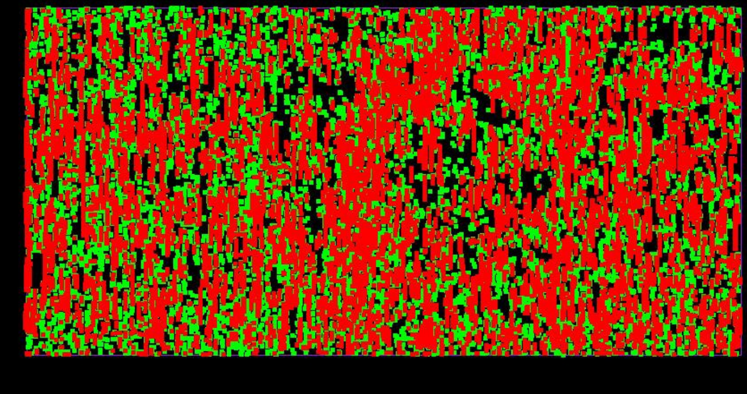
90nm, 6 layer Process



DRC Clean

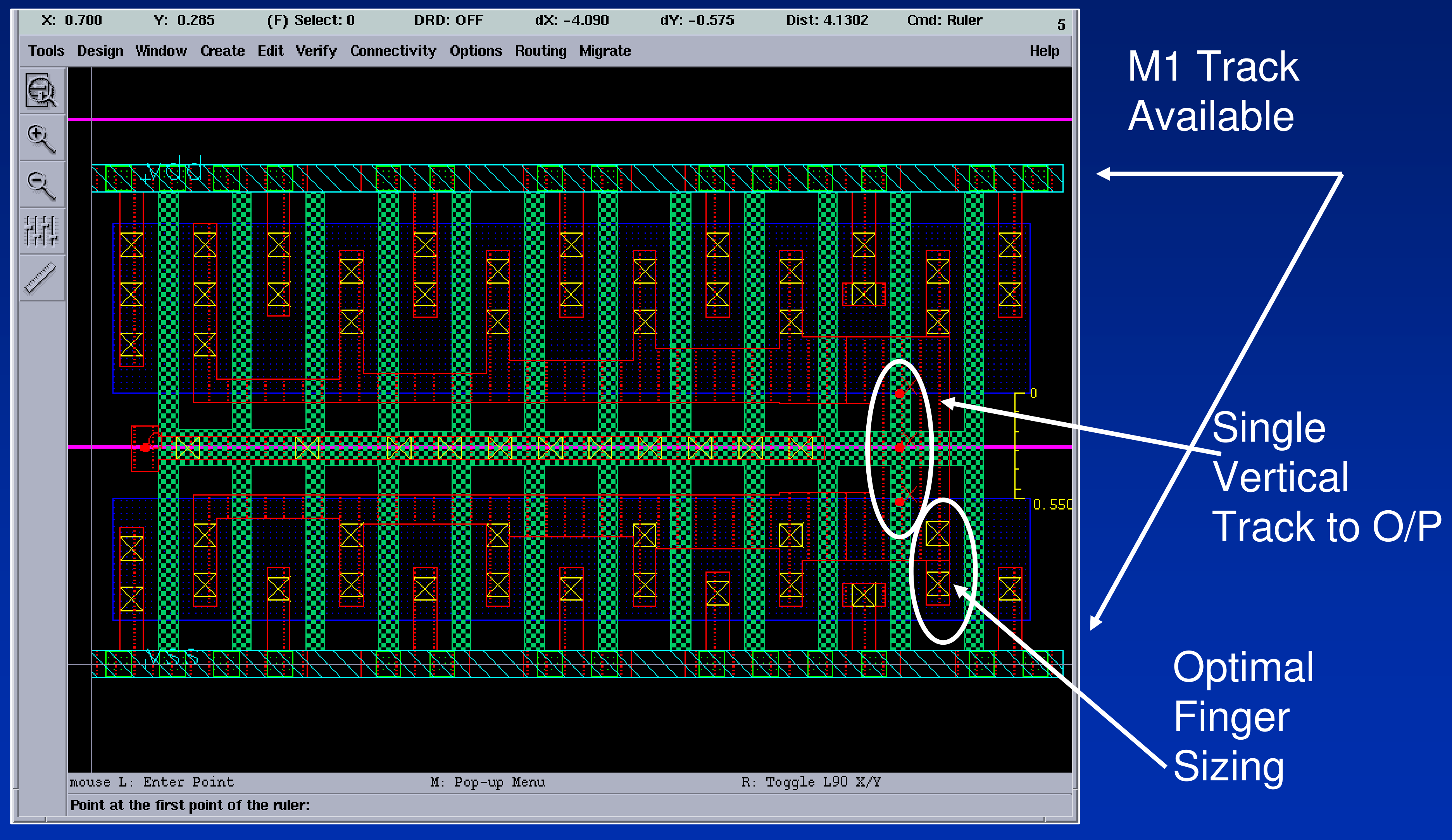


DFM Check



DFM Fix
Area Neutral

Electrical DFY

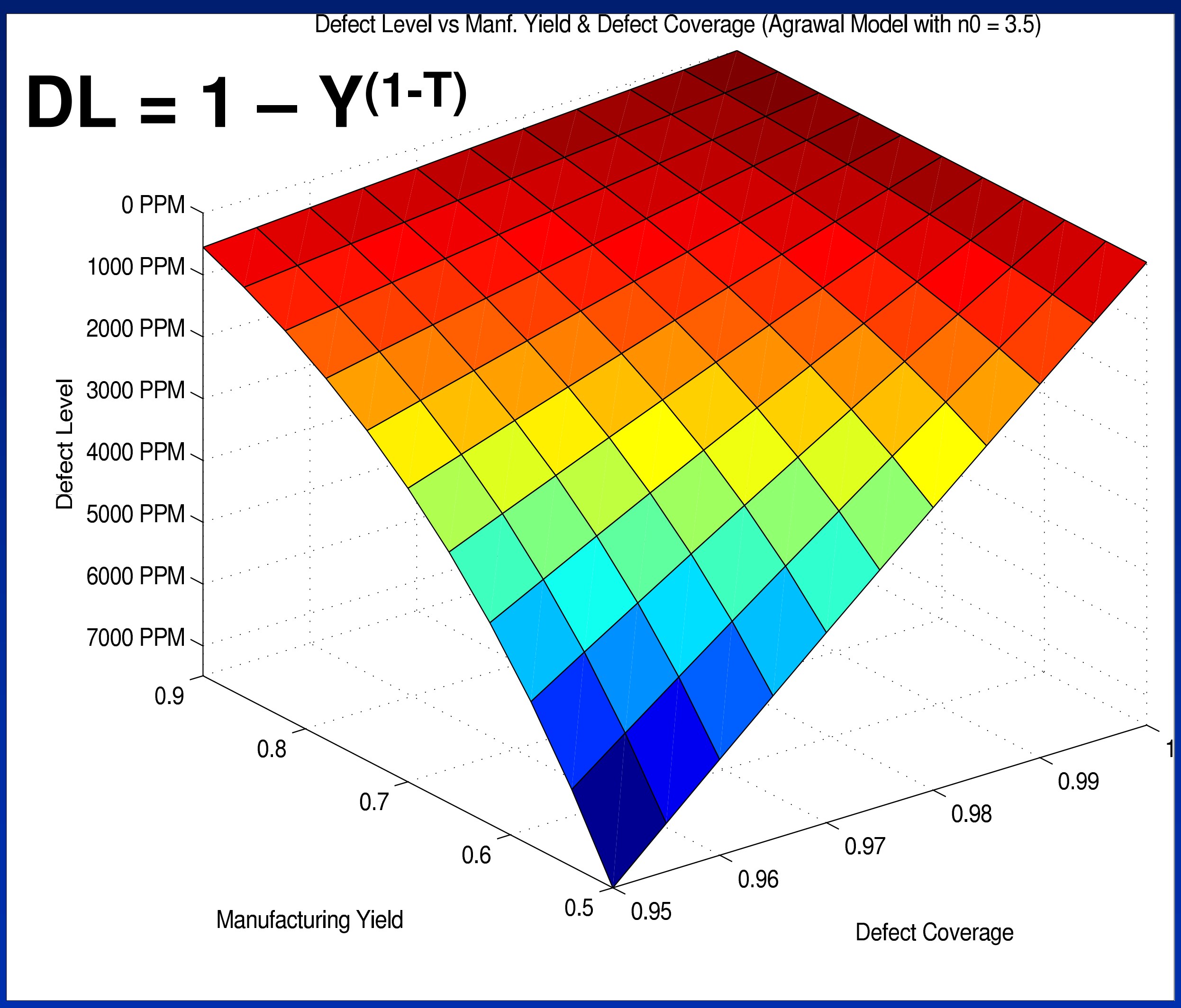


Source: Michael Zimin

Electrical DFY

- **Physical defects can be seen. Electrical defects cannot be seen.**
- **However Electrical Operation is affected which leads to Yield loss**
- **Electrical DFY Opportunities**
  - P/N Ratios
  - Using M2 for Clock inside FF
  - Making multiple vertical tracks available
  - Using M1 for power (in addition to M2)

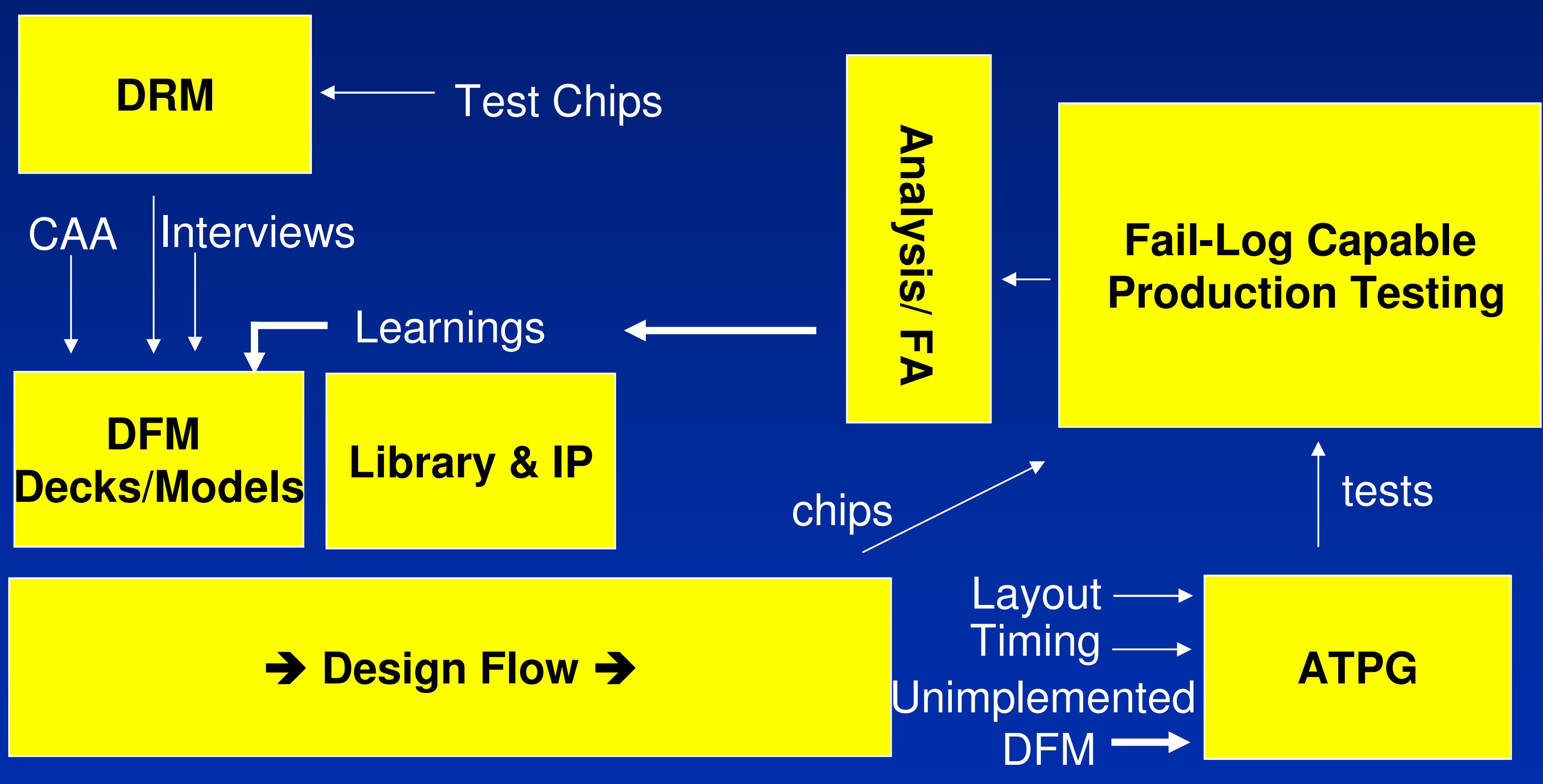
DFY & DFT Nexus



Y = Yield
T = Test Cov
DL = Defect Level

Source: Williams & Brown '81

DFY & DFT Nexus



DFM – Future Opportunities

- Standard Definitions
- Integrating into Design Flow
- Model Based vs Rule Based
- Electrical DFY
- DFY and DFT helping each other

Conclusions

- DFM is an extension of DRC
- Physical DFY is the most common form of DFM – Essential for 90nm & below
- Physical DFY is being integrated in a modern design flow
- Electrical DFY is the next opportunity
- DFY & DFT complement each other
- DFM is incremental

Conclusions

- DFM is an extension of DF

Fixing Antenna and using Double cut vias in a single run:

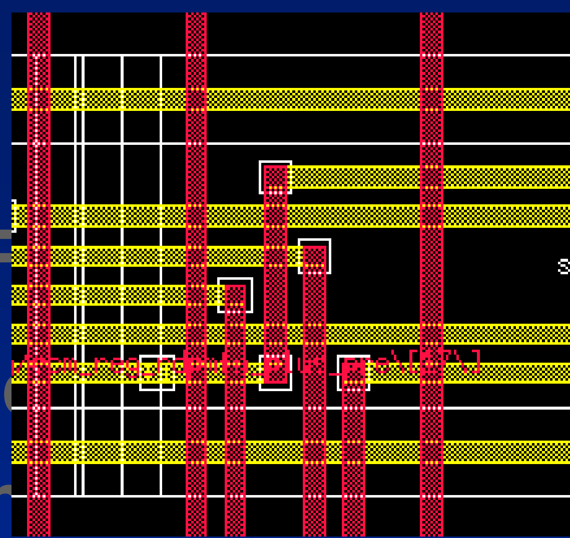
The following commands repair process antenna violations by inserting diodes and insert fi
left when the diodes replace large filler cells:

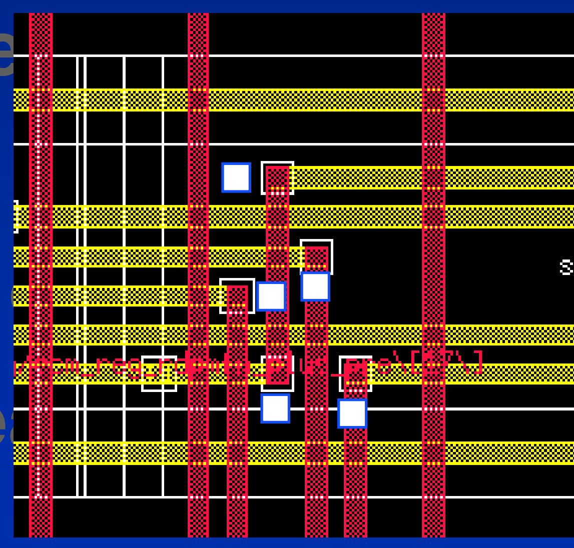
```
setNanoRouteMode routeInsertAntennaDiode true
setNanoRouteMode routeAntennaCellName cell_A
setNanoRouteMode routeReInsertFillerCellList my_fillers
globalDetailRoute
```

The following commands replace single-cut vias with double-cut vias. Run these command

```
setNanoRouteMode drouteOptimizeUseMultiCutVia true
setNanoRouteMode drouteStartIteration 20
setNanoRouteMode drouteEndIteration default
detailRoute
setNanoRouteMode drouteOptimizeUseMultiCutVia false
setNanoRouteMode drouteStartIteration 16
setNanoRouteMode drouteEndIteration 20
detailRoute
```

- DFY & DFT complement e
- **DFM is incremental**





+1.7% Yield !