DFM

The path toward maturity through innovation and consistent added value

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DFM "ecosystem" evolution from 90nm to 45nm

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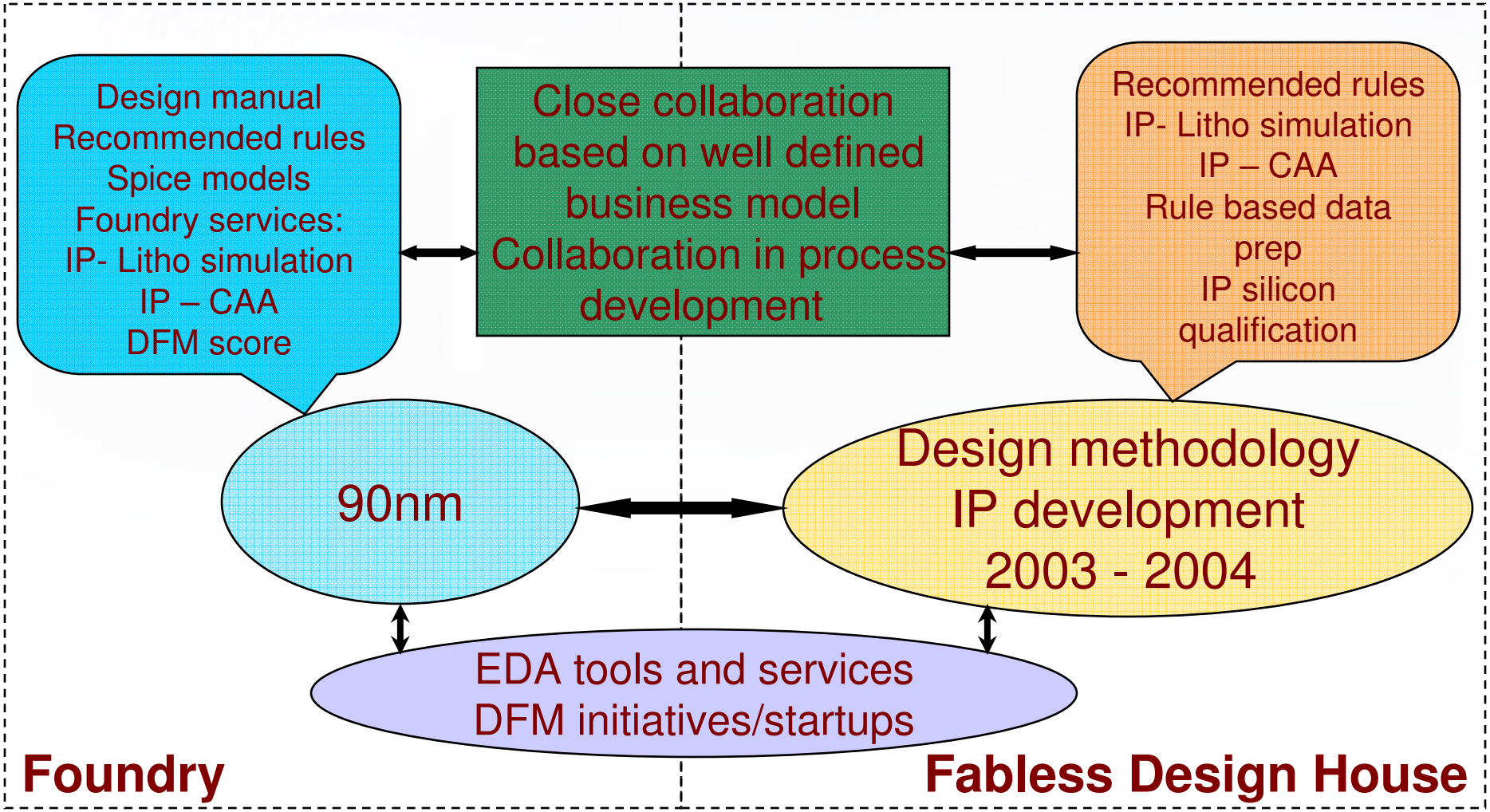
- **Process evolution && Design methodology evolution:90nm**



DFM "ecosystem" evolution from 90nm to 45nm

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- **DFM methodology impact: 90nm**
  - Biggest impact in IP development
  - Major impact in physical design data prep:
    - Via redundancy insertion
    - Dummy fill generation
  - Limited impact in block/chip level physical implementation and timing closure
  - Limited impact in timing/power optimization

- **"DFM Design Cost" vs. "Impact in Quality of Design" relative comparison:**
  - Using a scale from 1 to 20
    - DFM cost: 2
    - DFM impact (yield, time to market, performance): 5

DFM "ecosystem" evolution from 90nm to 45nm

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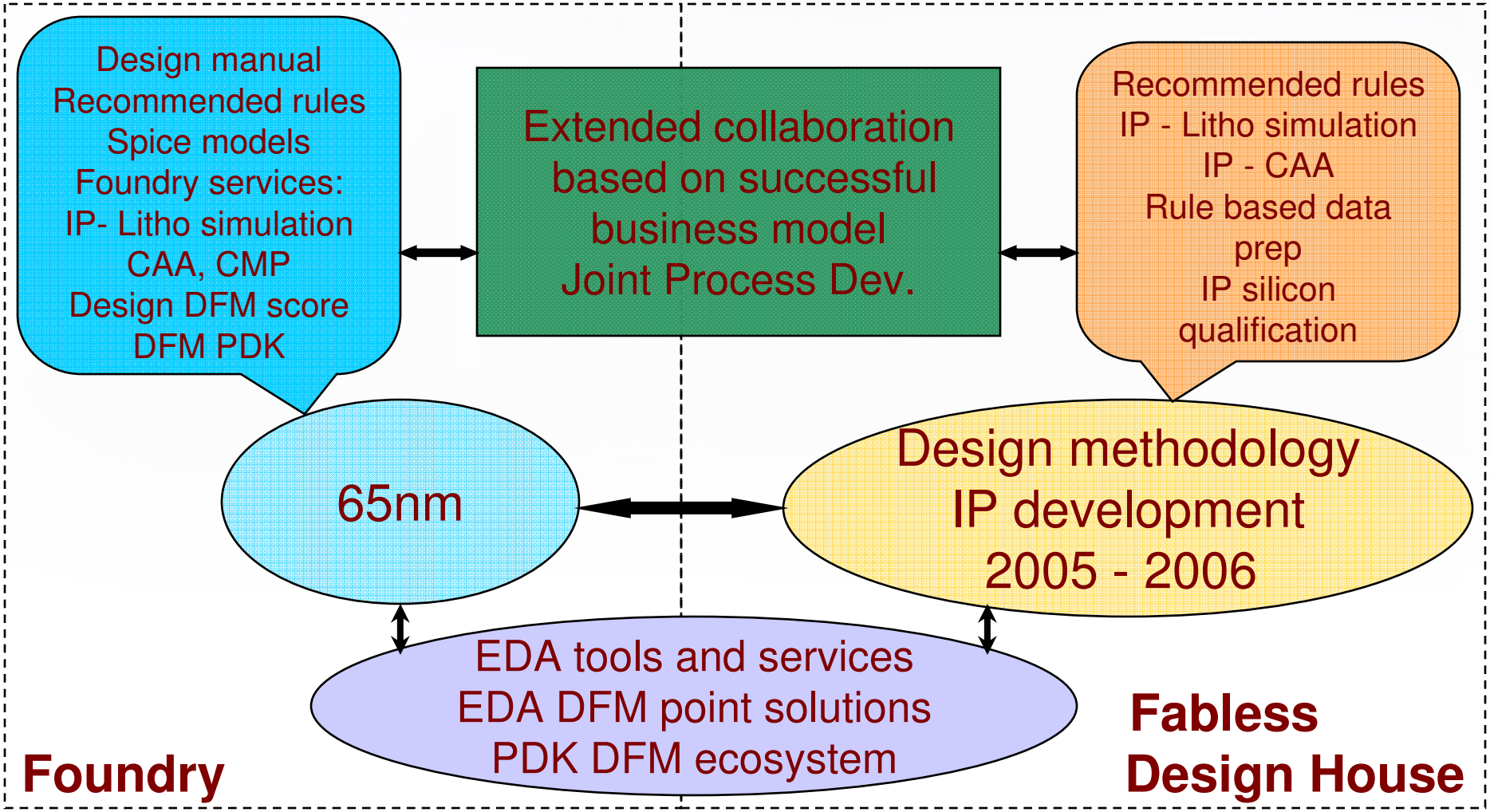
- **Process evolution && Design methodology evolution: 65nm**



DFM "ecosystem" evolution from 90nm to 45nm

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- **DFM methodology impact: 65nm**
  - Biggest impact in IP development
  - Major impact in physical design data prep:
    - Via redundancy insertion
    - Dummy fill generation
    - OPC driven layout optimization
  - Limited impact in block/chip level physical implementation and timing/power closure
  - Limited impact in timing/power optimization

- **"DFM Design Cost" vs. "Impact in Quality of Design" relative comparison:**
  - Using a scale from 1 to 20
    - DFM cost: 4
    - DFM impact (yield, time to market, performance): ?

DFM "ecosystem" evolution from 90nm to 45nm

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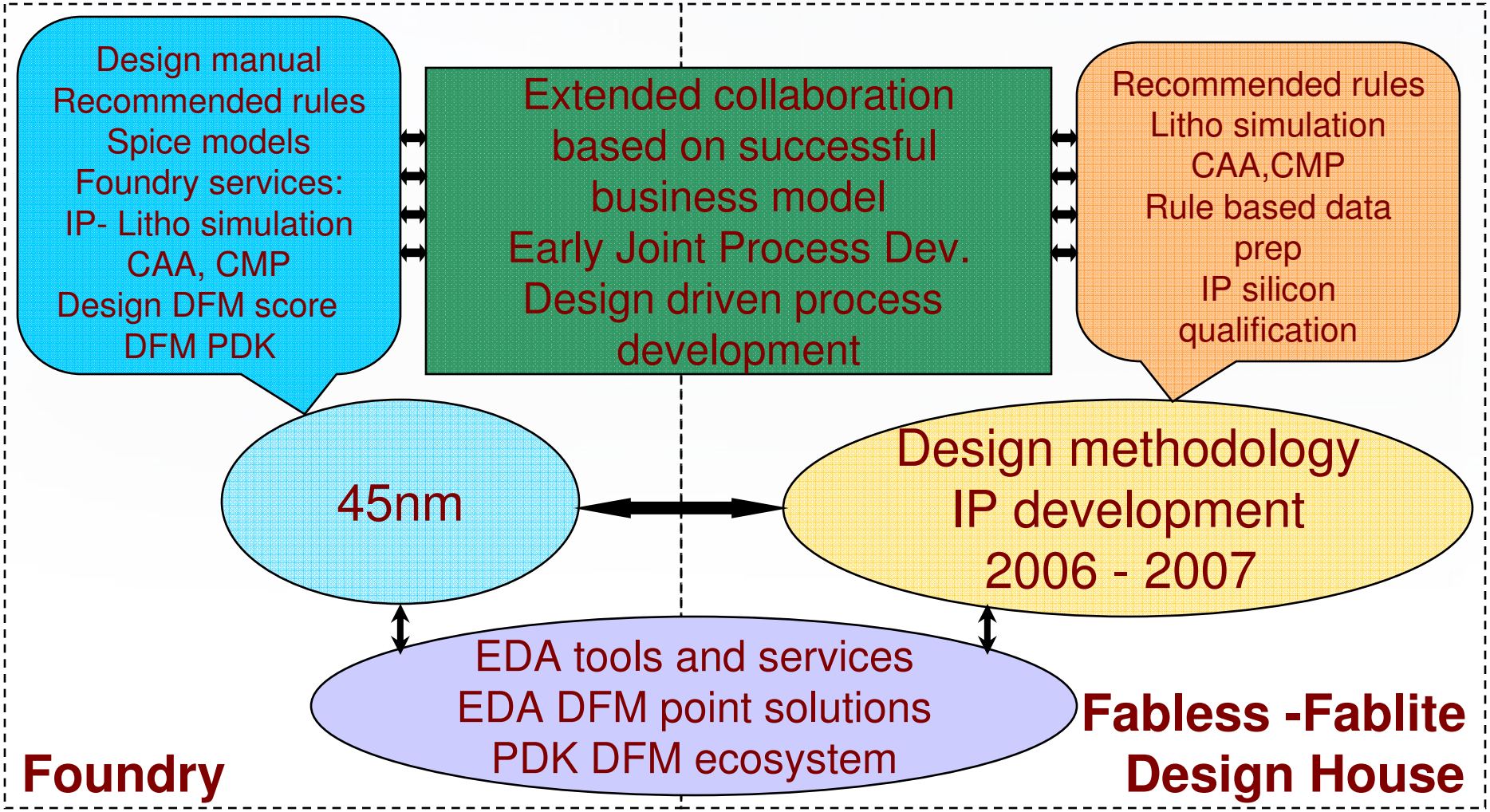
- **Process evolution && Design methodology evolution: 45nm**



DFM "ecosystem" evolution from 90nm to 45nm

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- **DFM methodology impact: 45nm**
  - Biggest impact in IP development
  - Major impact in physical design data prep:
    - Via redundancy insertion
    - Dummy fill generation
    - OPC driven layout optimization
  - Limited impact in block/chip level physical implementation and timing/power closure
  - Limited impact in timing/power optimization

- **"DFM Design Cost" vs. "Impact in Quality of Design" relative comparison:**
  - Using a scale from 1 to 20
    - DFM cost: 8
    - DFM impact (yield, time to market, performance): ?

DFM "ecosystem" evolution from 90nm to 45nm

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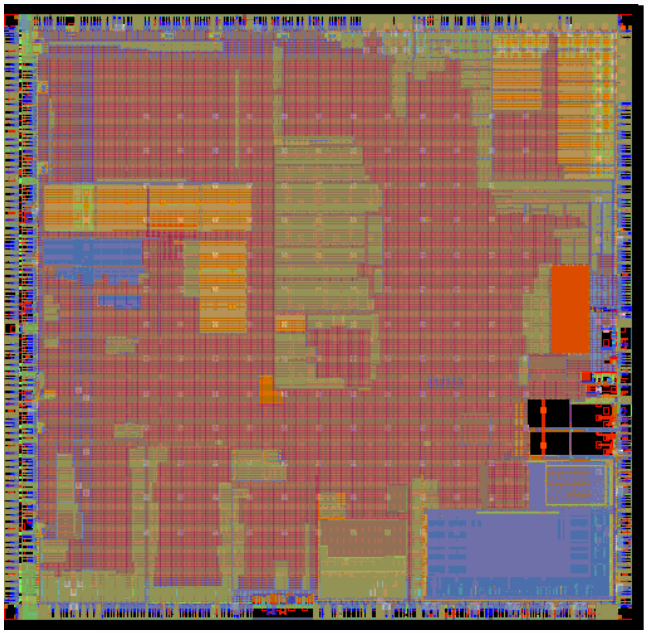
- When are we going to see a similar slope for the "design benefits" associated with DFM, to the slope of the cost associated with the enablement of the new DFM tools and methodologies ?

- What is the "key" element which will contribute significantly to the added value of the design which will make DFM mandatory or highly desirable ?

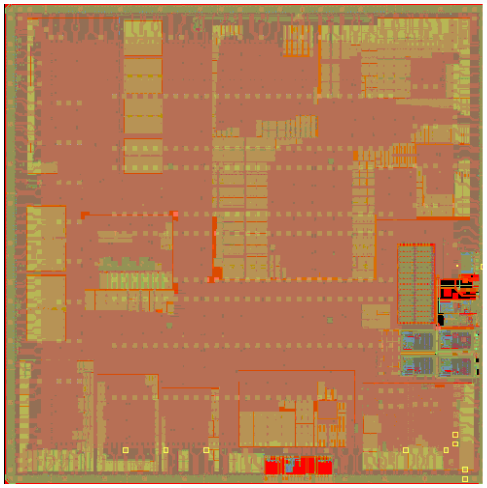
- In which process node a design start-up can not live without DFM ?

90nm vs. 65nm vs. 45nm DFM impact

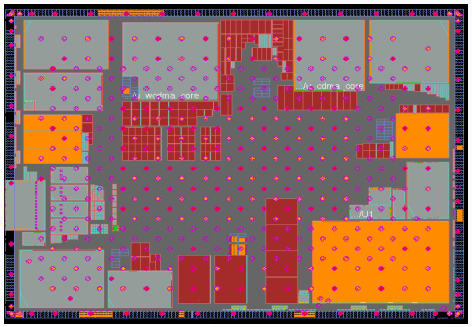
90nm design



65nm design



45nm design



DFM90 >= DFM65 >= DFM45

No DFM models | Inaccurate DFM models | No DFM models

The PDK DFM enablement is behind the process and design ramp-up curve !!!

90nm vs. 65nm vs. 45nm DFM impact

- **DFM should be part of the SOLUTION for fast ramp-up not part of the PROBLEM (Extra Cost):**
  - In order to reduce the gap between process ramp-up and DFM enablement, relatively easy to generate and calibrate DFM models should be developed.
  - It is beneficial for the DFM companies to work together with the foundries, IDM's and academia to generate these models and to standardize the test vehicles used for extraction and calibration.
- **DFM should be part of the SOLUTION for higher yield products and faster time to market in new immature processes:**
  - Building IP's with less variability using restricted design rules is a good option for faster time to market, higher parametric yield and design predictability (smaller variation across process window). Also it provides a very competitive COST alternative for process development relative to other solutions.

Design challenges for DFM

- Lack of integration in the existing COT/ASIC Design Flows.
- Immature (in development) use models.
- Highly dependent on proprietary process models:
  - Late arrivals
  - Lack of qualification methodology in the design space
  - Immature procedure for model updates
  - Questionable portability/scalability across technology process nodes
- Major developments in the design space (new EDA tools and design flows) which have major impact in timing/power optimization competing with EDA E- DFM solutions.
- Design driven process development and optimization
- Advancements in device engineering, device optimization and process integration.
- Less process variability driven by restricted design rules in advanced process nodes (65nm/45nm).

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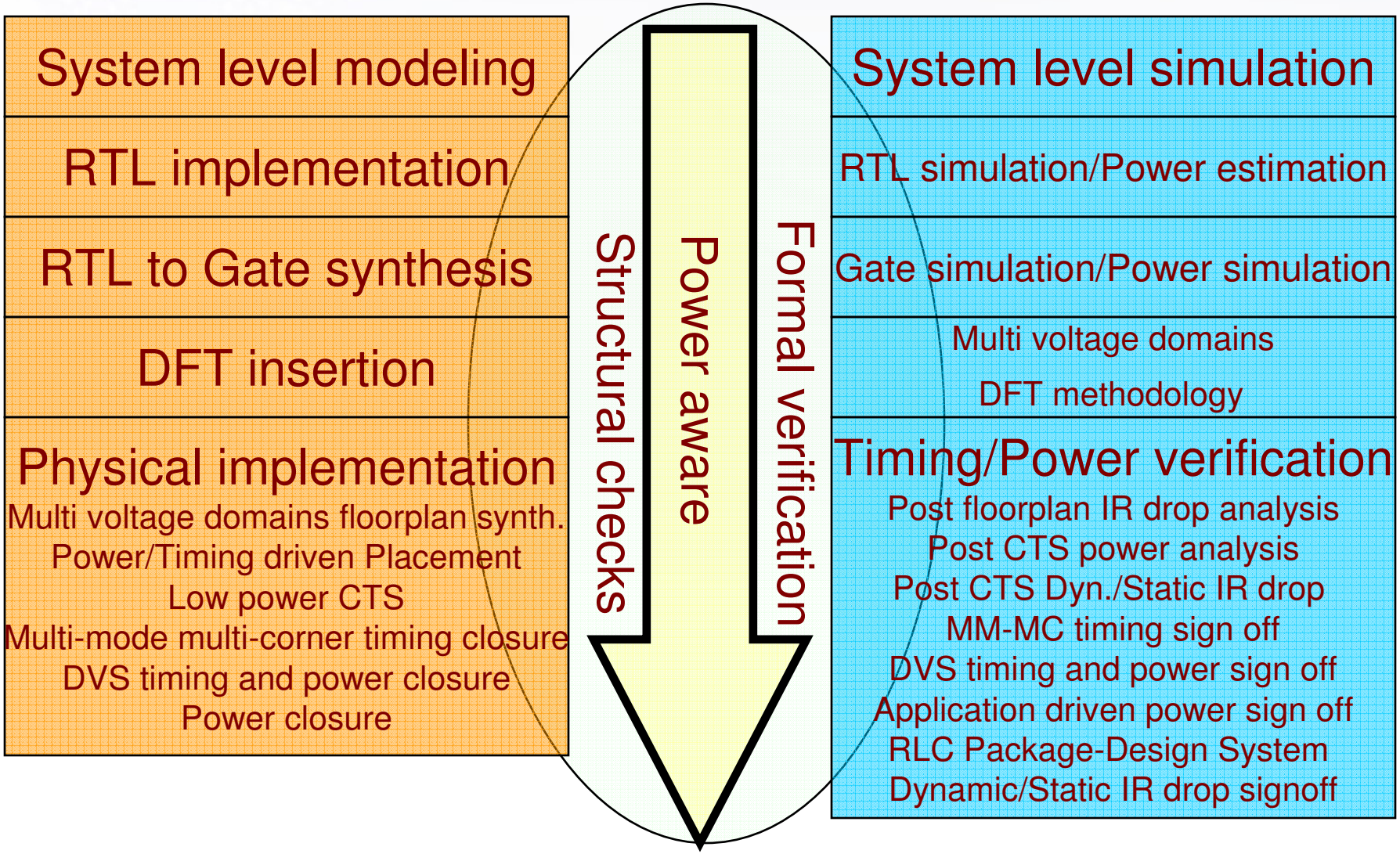
➢ Power aware integrated design "ecosystem":



E- DFM solution scalability across process nodes

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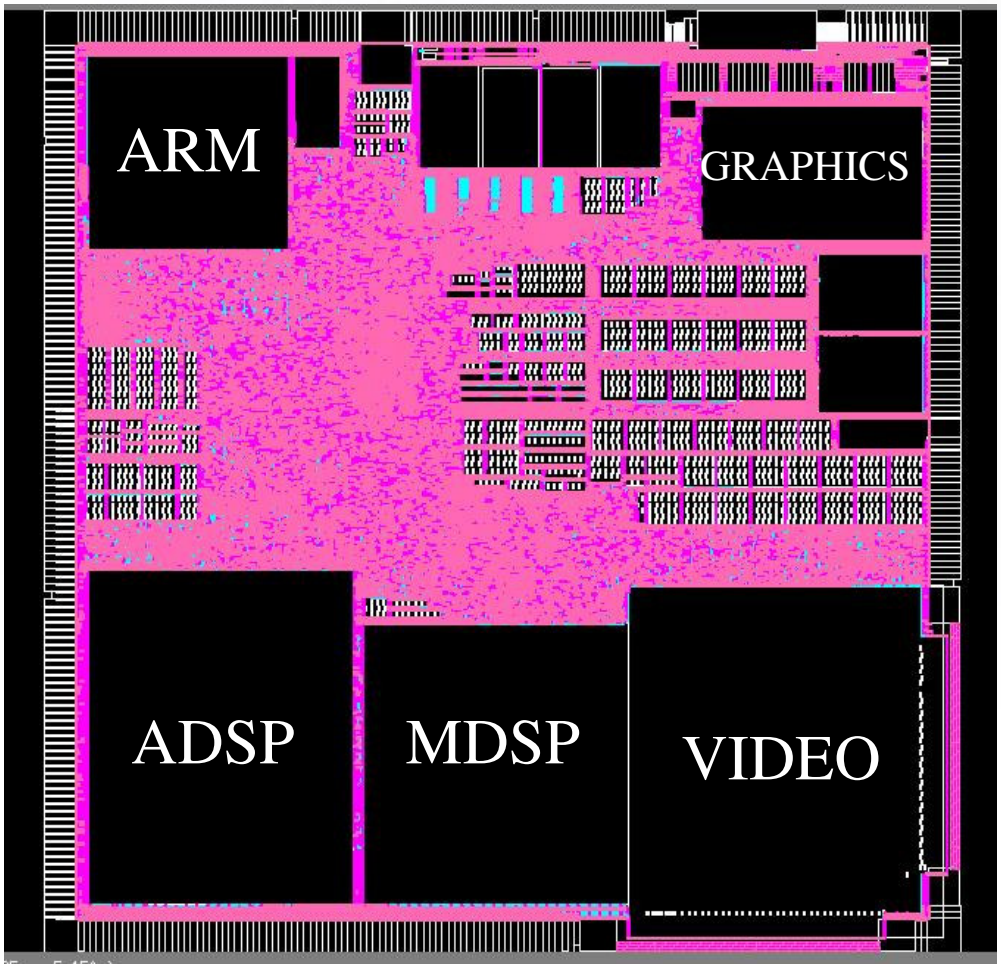
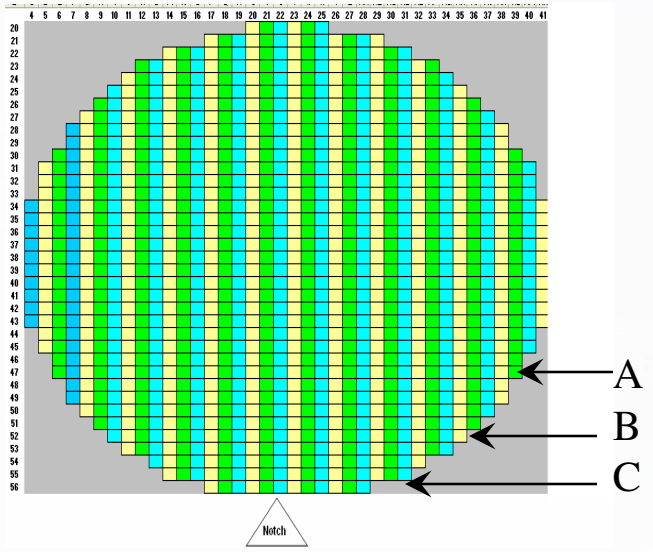
➢Leakage optimization using channel length modulation in 90nm





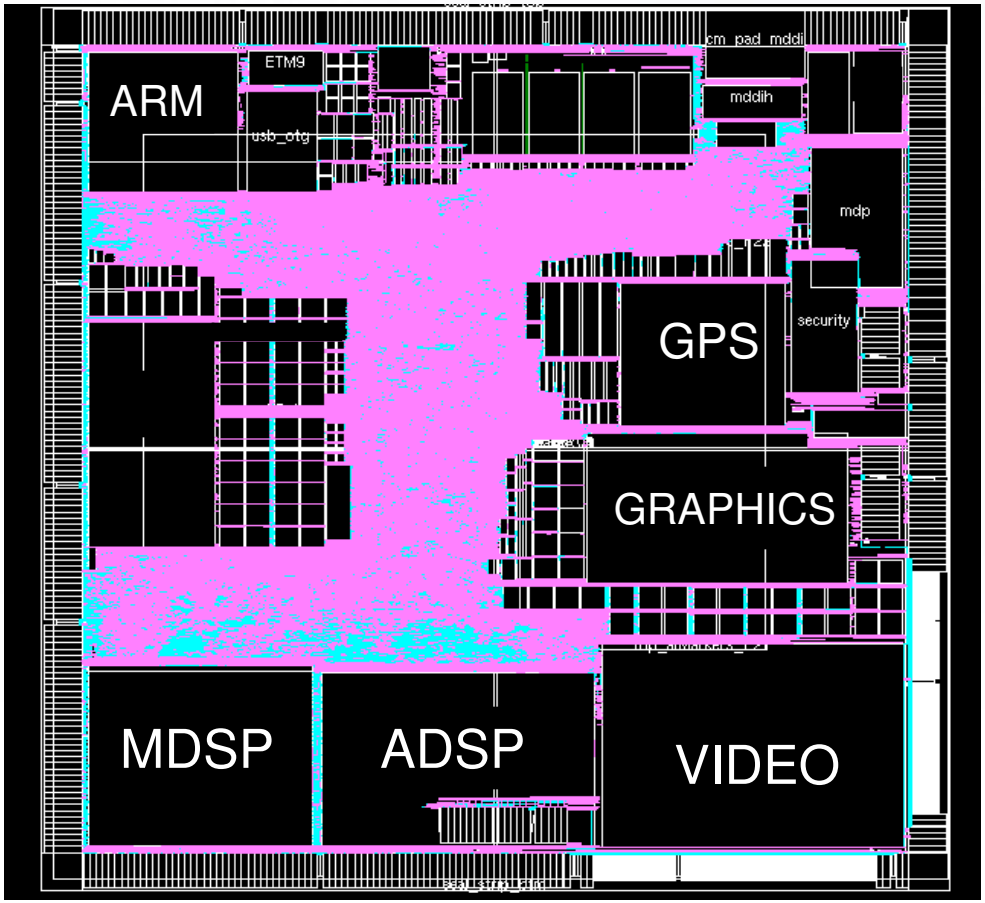
Silicon validation of DFM optimization:
A vs. B vs. C side by side comparison

A: Plan of record
B: DFM optimized design
C: Foundry design variant

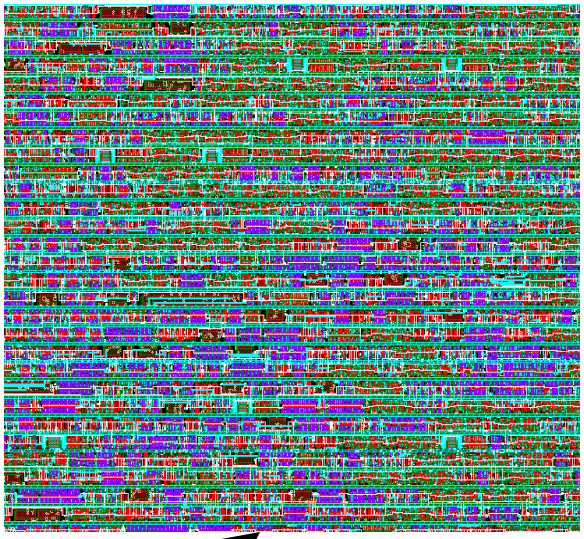
20% leakage current improvement

E- DFM solution scalability across process nodes

- Leakage optimization using channel length modulation in 65nm



65nm WCDMA MSM design



Sample area of gates:

- Biased gates in magenta

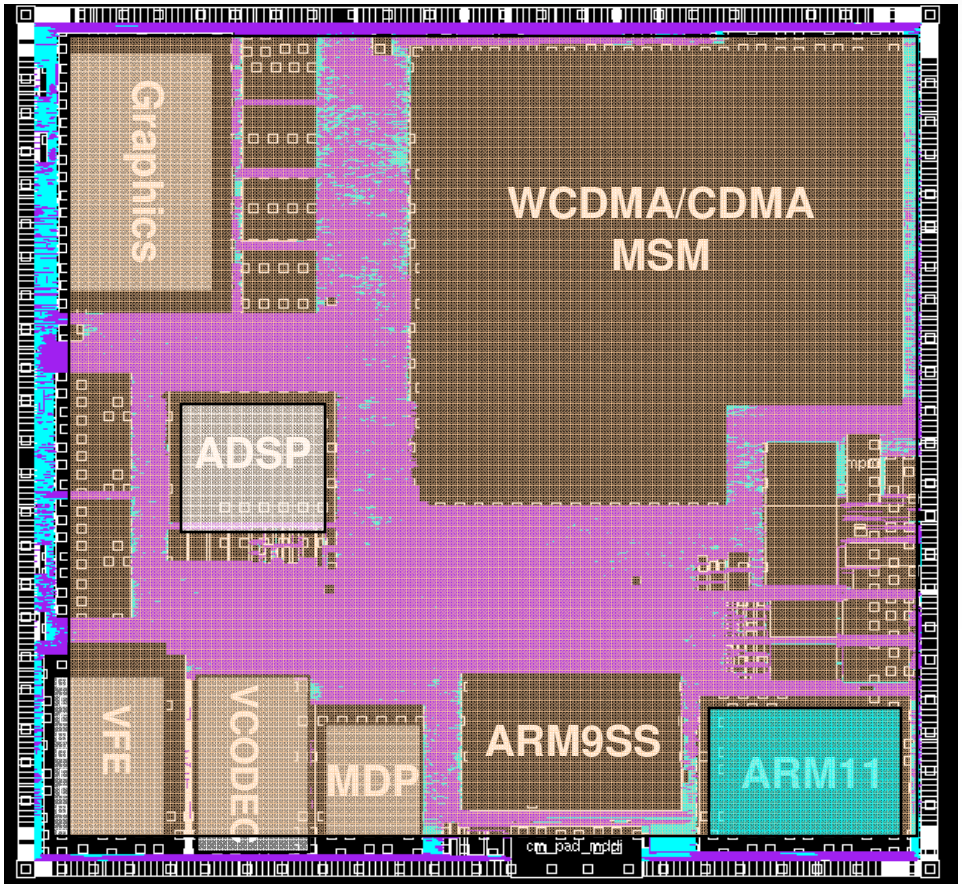
Optimization:

- CD biasing
- Vt swapping

20% leakage reduction on the optimized design

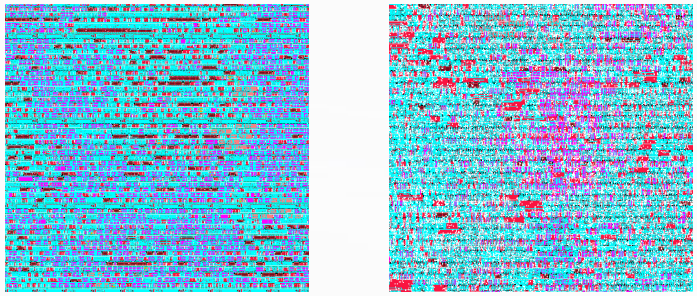
E- DFM solution scalability across process nodes

- Leakage optimization using channel length modulation in 65nm design which is using POWER/GROUND gating and MULTI Voltage Domains



65nm convergence platform

Low speed High speed



Sample area of gates:
- Biased gates in magenta

Optimization:
- CD biasing
- Vt swapping

Leakage saving depends on the state of the blocks:
- All the blocks on: 15%
- Sleep mode: 5%

E- DFM solution scalability across process nodes

- Leakage optimization using channel length modulation in 45nm design:
  - Major changes in timing and power corners methodology due to reverse temperature effects
  - Dual vt process versus triple vt process in 65nm:
    - NVT cells
    - Longer channel length cells NVT, LVT
    - LVT cells
  - Most of the blocks will be POWER/GROUND collapsible
  - Major challenges in 45nm designs:
    - Low voltage functionality
    - AC noise associated with dynamic voltage drop.
    - Vt variability
    - DVS sign off.
    - Process immaturity

What we expect from DFM moving forward

- **Model based DRC:**
  - We would like to see the model based DRC becoming reality for physical signoff.
  - We would like to see the litho and CAA DFM tools integrated in the design flow.
  - We need to see a consistent verification methodology based on silicon data. (rule based + model based)
- **SSTA:**
  - What is the business value of SSTA (ROI) ?
  - When SSTA is going to be ready for real designs ?
  - Can we use SSTA to do silicon to design correlation ?
- **E-DFM:**
  - Has to take in consideration the reality of current EDA landscape : LOW POWER INITIATIVES
  - Take in the consideration the advancements in process development (low power optimized process, new set of design constraints).

What we expect from DFM moving forward

- We would like DFM "ecosystem" and solutions to provide a step function jump in the value added for the designs.

DFM IS PART OF THE SOLUTON FOR THE DESIGNERS

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What we expect from DFM moving forward

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- **What DFM should provide for the design house:**
  - Real impact in faster time to market for designs implemented in new process nodes
  - Real impact in shorter design cycle and higher parametric yield
  - A flexible and integrated solution in the design flows which scales well across process technology nodes

- **What DFM should NOT be:**
  - An exotic solution which does not help the designer and disregards the design methodology
  - An exotic solution which does not help the manufacturing of the product and the yield ramp-up process.
  - A costly solution which does not produce measurable benefits