DFM: It's all about *Flexibility*

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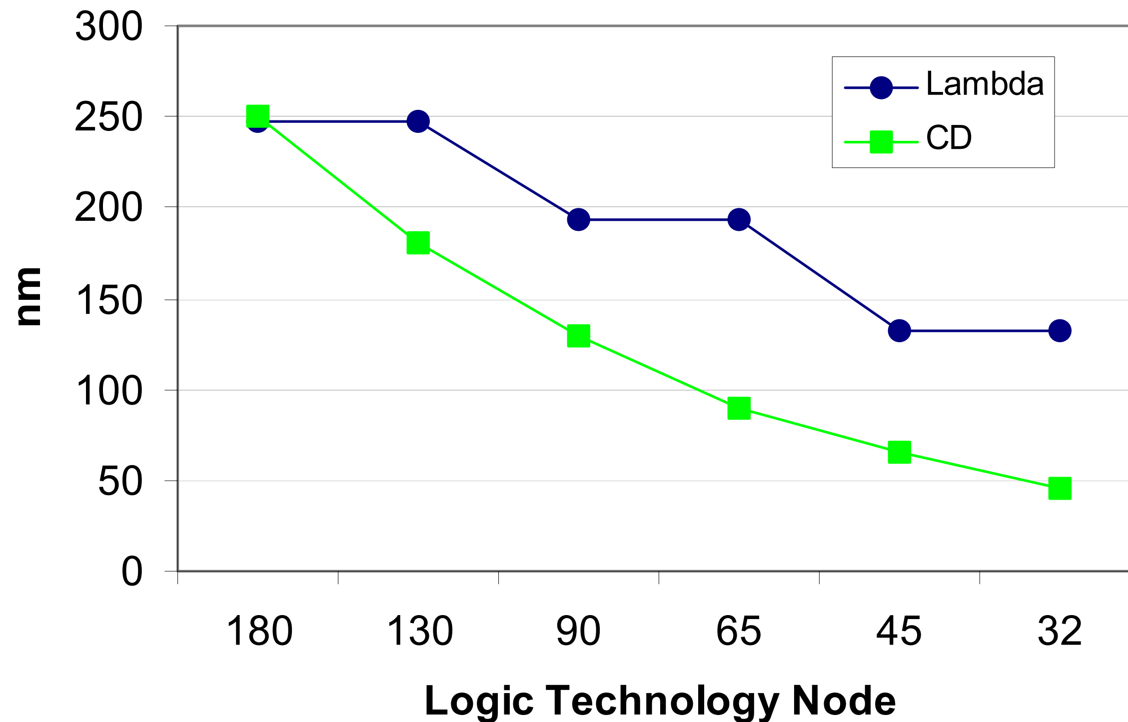
Topics

- Introduction
  - Moore's law, scaling, the end of scaling
  - Photolithography, the subwavelength era
  - Resolution, knobs to turn
- Cost
  - Scanner cost trends; dry, wet, hyper
- Design style
  - Need to consider design and technology
  - 2D versus 1D design styles
  - RDR's and an additional k_1* factor
- Conclusions

Integrated Circuit Scaling

- **Moore's law**
  - Density of transistors doubles every n years (n=1, 1.5, 2, 3)
- **Scaling benefits**
  - Scaling laterally by 70% each generation (technology node) cuts the die area by 50%
  - Circuit frequency can increase, or power decrease
- **The end of scaling**
  - Transistor gate oxide thickness is limited by atomic spacing (we now count atomic layers in the dielectric)
  - Electrons can directly tunnel through thin barriers
  - These two factors are responsible for the power dissipation crisis we face today

Photolithography: the subwavelength era

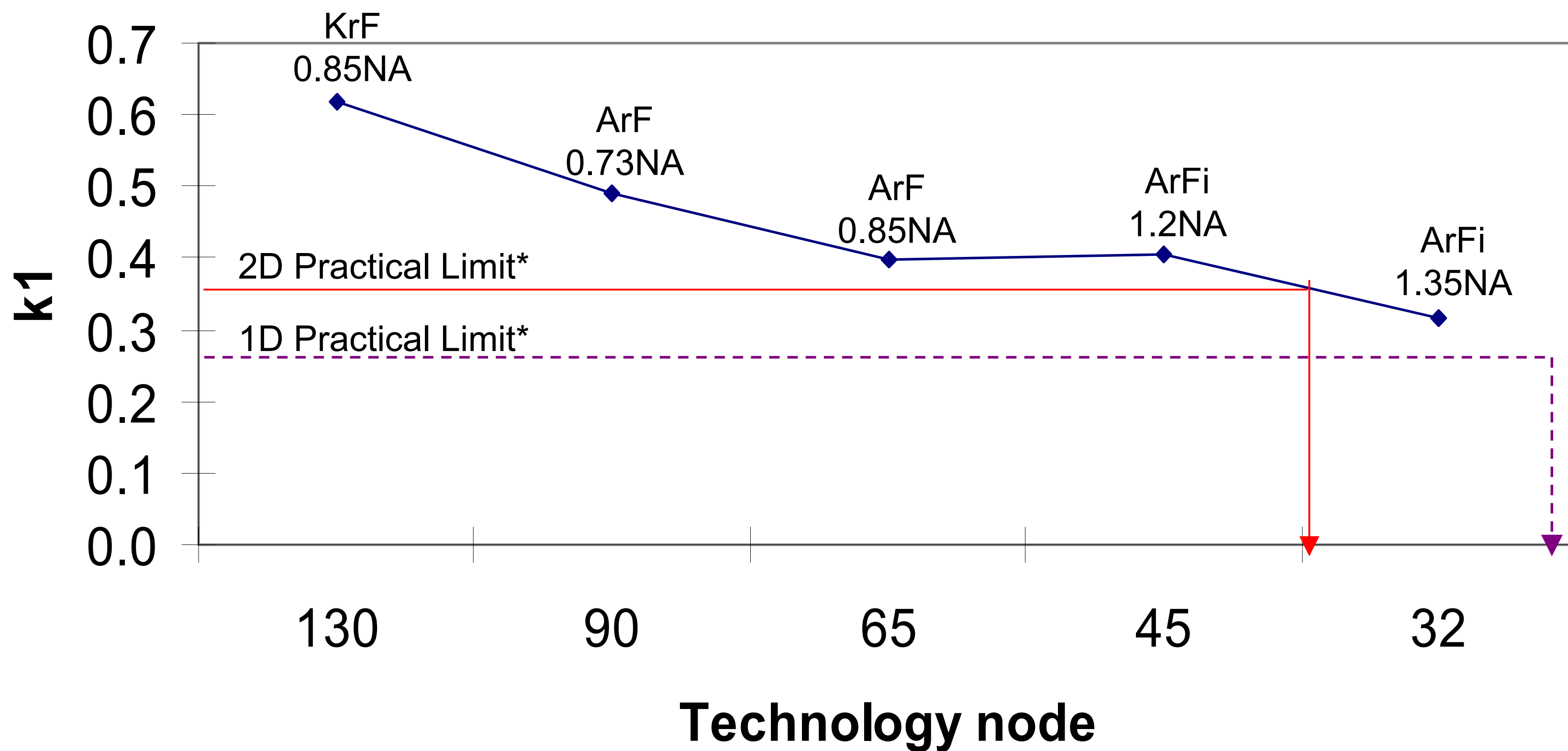


Patterning with λ less than the critical dimension creates a fidelity problem

Optical Resolution

- **Rayleigh's equation**
  - **$CD = k_1 \lambda/NA$**
    - **k_1 is the difficulty factor, lower is more difficult**
    - **λ is the illumination wavelength; 193nm for ArF excimer laser**
    - **NA is the numerical aperture of the optical system**
- **Knobs to turn**
  - **Patterning with lower k_1 essentially means lower fidelity in the stepper requires higher capability in the resist process; in general, the contrast is lower so "chemically amplified" resists are needed**
  - **λ is expensive to reduce, and nature gives few choices (the next choice, the F_2 excimer at 157 nm, was dropped from the roadmap)**
  - **NA has steadily increased, but the size and cost of the lens grows quickly with higher NA**

k_1 trend



For each successive technology node in the subwavelength era, the difficulty factor has been approaching the practical limits.

* Bill Arnold (ASML), IEDM 2006 32nm Short Course

Patterning cost

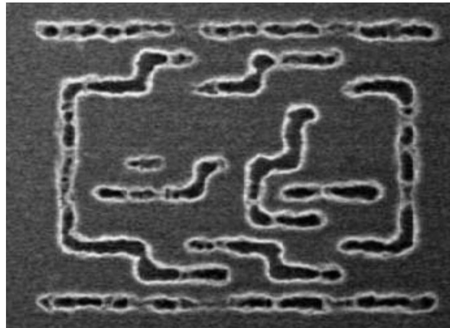
- **Stepper / scanner cost**
  - **~$1M in 1986**
  - **~25M in 2005**

  - **The decrease in λ and increase in NA have come at a cost, but until now the increase in cost has been offset by a decrease in die size**
  - **It is not clear that next generation steppers with NA>1.3 are feasible and can be cost effective**
- **Impact of reduced fidelity**
  - **Even with improved steppers, k_1 has decreased steadily from $k_1 > 0.6$ to $k_1 < 0.4$.**
  - **OPC (optical proximity correction) has been used to try to improve pattern fidelity**
  - **Unfortunately, even with OPC, low k_1 results in "hot spots" in the design which may not be correctable**

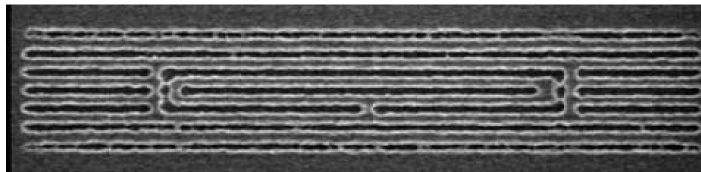
Design – Technology interaction

- **Morris Chang, founder of TSMC, at ISSCC 2007: "deeper and broader relationships with customers are needed, covering both design and technology engineering to allow for increasing demands for product-cost performance and reduced time-to-market"**
- **The traditional approach of using binary (pass/fail) design rules to communicate patterning capability from a fab to a design team is no longer enough to ensure a yieldable design**
- **An emerging factor is design style, in which how rules are used becomes important**

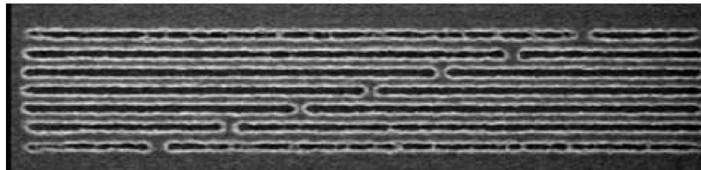
Design styles



- Traditional 2D layout with bends, bi-directional shapes



- 2D layout with restrictions (RDR)



- 1D layout

Even though k1 = 0.31 in all cases, the fidelity of the 1D layout is better. Note that the 2D layout with restrictions still had problems at the bends.

SEMs from Applied Materials SPIE 2007 poster.

Conclusions

- Chip yield depends on the fidelity of the design layout replicated on wafers.
- The industry is clearly at a cross-roads, where the cost of photolithography is limiting lateral scaling; major players have dropped out of the race at 32nm.
- Even with RDR's, the needed patterning fidelity may be beyond economic limits at 45nm and below.
- Design style, for example more use of 1D patterns, is an important factor to consider to allow further scaling.

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