Should Power Management Govern Design Hierarchy?

EDP, April 2007, Ed Huijbregts

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- Logic Hierarchy
- Domain definition
- Floorplans and supply styles
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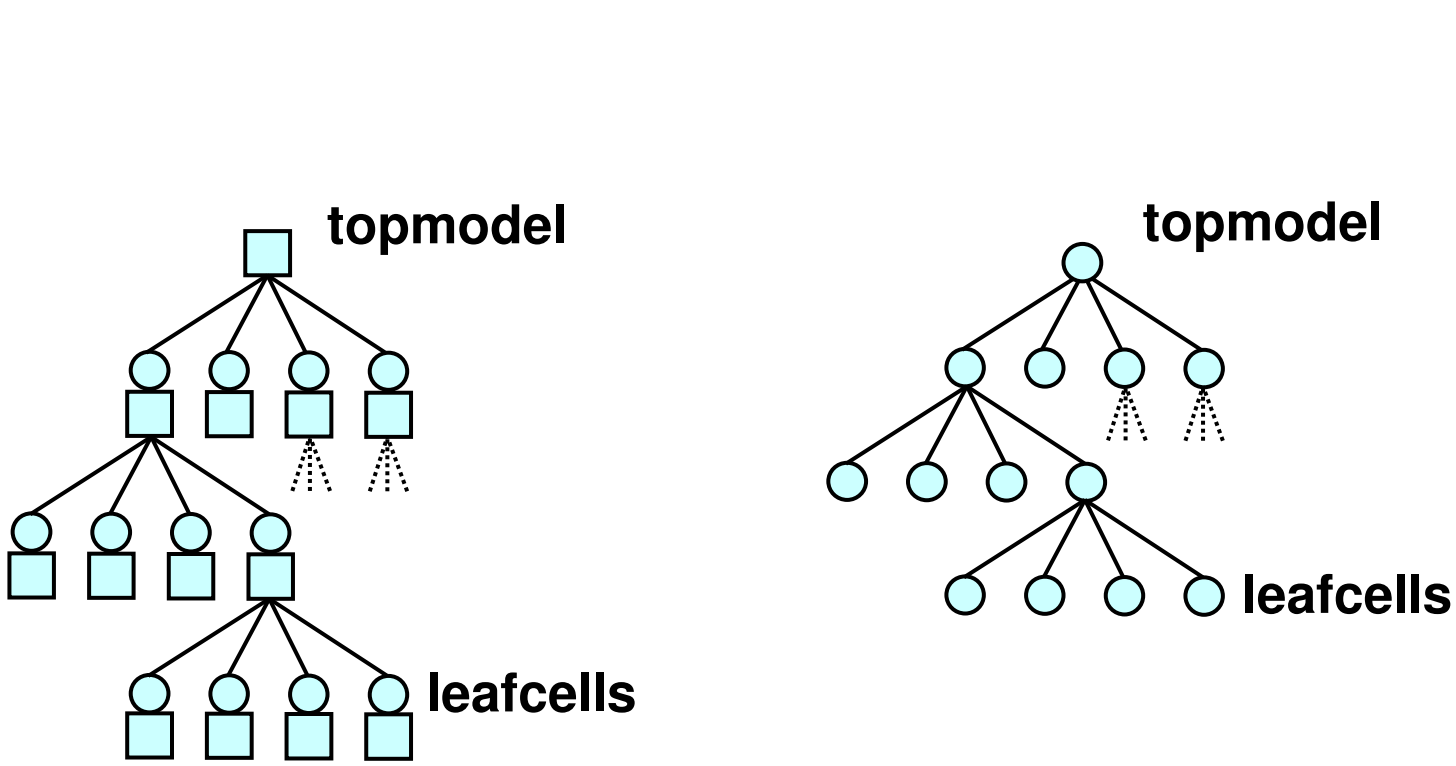
Logical Hierarchy



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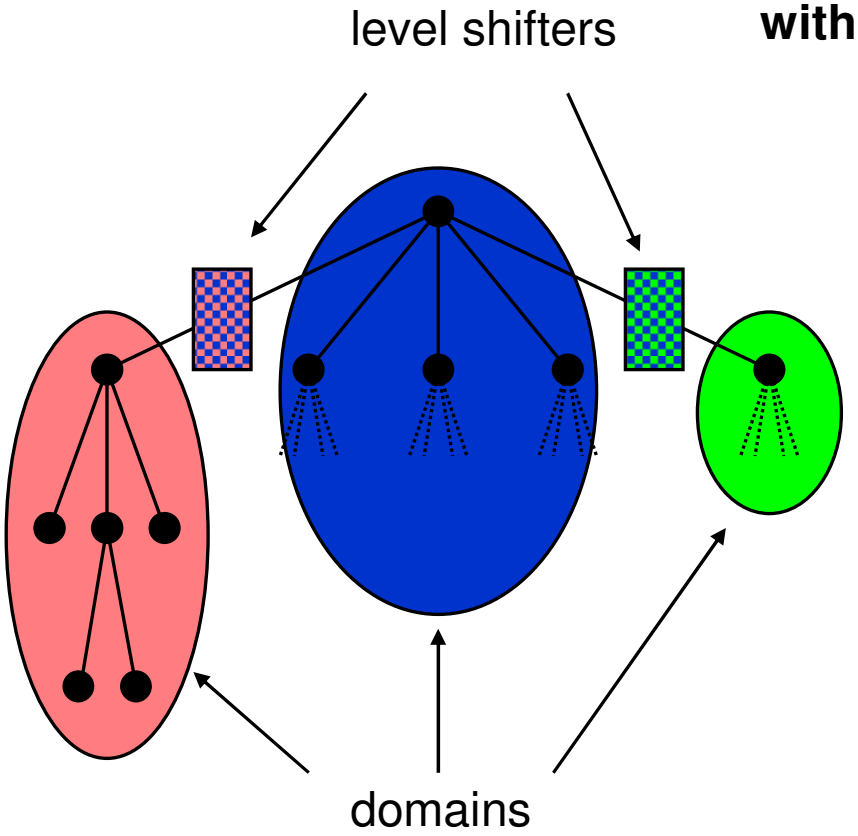
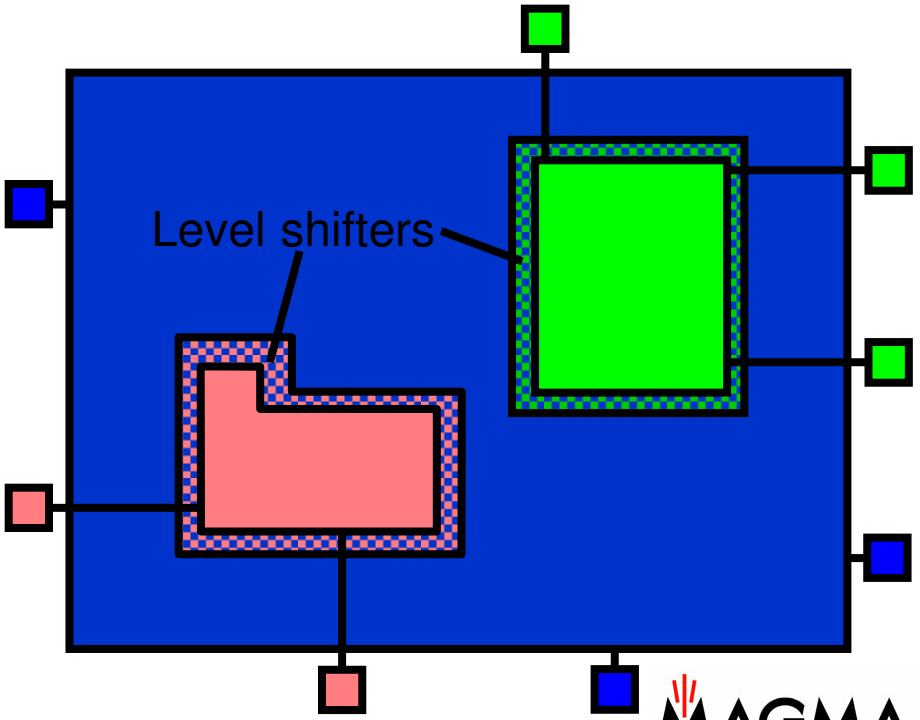
Logical - Electrical - Physical

Today, for optimization to work correctly domains and floorplans need to coincide with logical hierarchy throughout the flow





Domains

A domain specifies for a group of related cells

- **The supply nets for these cells**
- **The recipe to connect these nets to the cells**
- **The operating conditions, P V^n T for best and worst**

Typically domains are aligned with logical hierarchy

- **The logical boundaries are required to understand the electrical qualities of the inferred logic**
  - What domain does it belong?
  - What voltage do they run on?
  - What timing characteristics do they have?

- **Is this alignment really required?**

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E.g. Domains in UPF

- UPF creates domains on a model, called the scope of the domain
- The supply nets of the domain are visible in the extent of the domain, i.e. all hierarchical cells that are in this domain

- Draw figure to explain….

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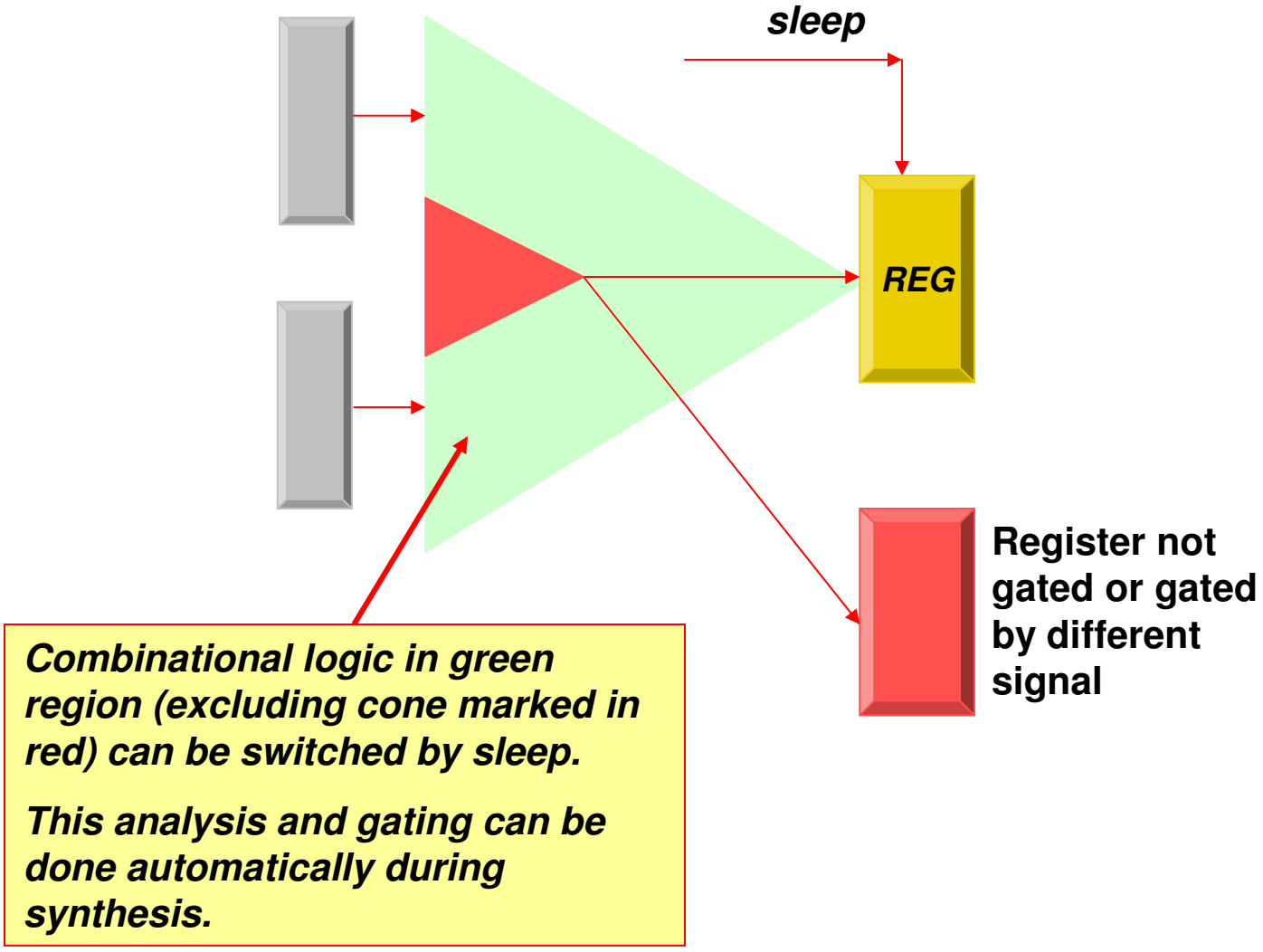
Automatic Power Gating – Not limited to hierarchy



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Floorplans

A floorplan specifies for a group of related cells

- Rectilinear shape
- Cell row definition

- Floorplans are not allowed to have partial overlap
- Floorplans behave as exclusive placement regions
- Floorplans behave as boundaries for global routing
- A floorplan has exactly one domain
- A domain may have multiple floorplans

Power distribution styles in floorplans are diverse, e.g.

- One set of supply nets homogenously available
- Occasional sparse supply connections routed as single-connections
- Multiple sets of supply nets, uniformly available in the floorplan
- Many small homogeneous floorplans, a.k.a. gas-stations
- Hybrid forms…..

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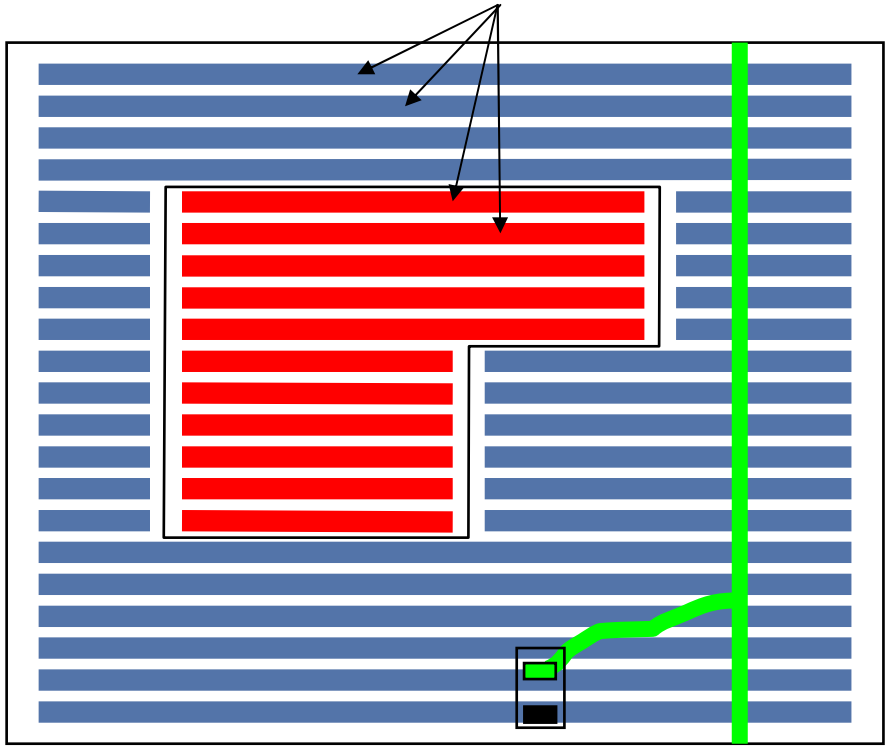
Floorplans and supply styles

- **Floorplans are used to create blocks in a building block style**
- **Floorplans are used to concentrate logic with similar supply requirements**
  - Different voltage levels
  - Switched supplies

Cellrows (color indicate supply sets)



Homogeneous floorplans, each cellrow has same rails

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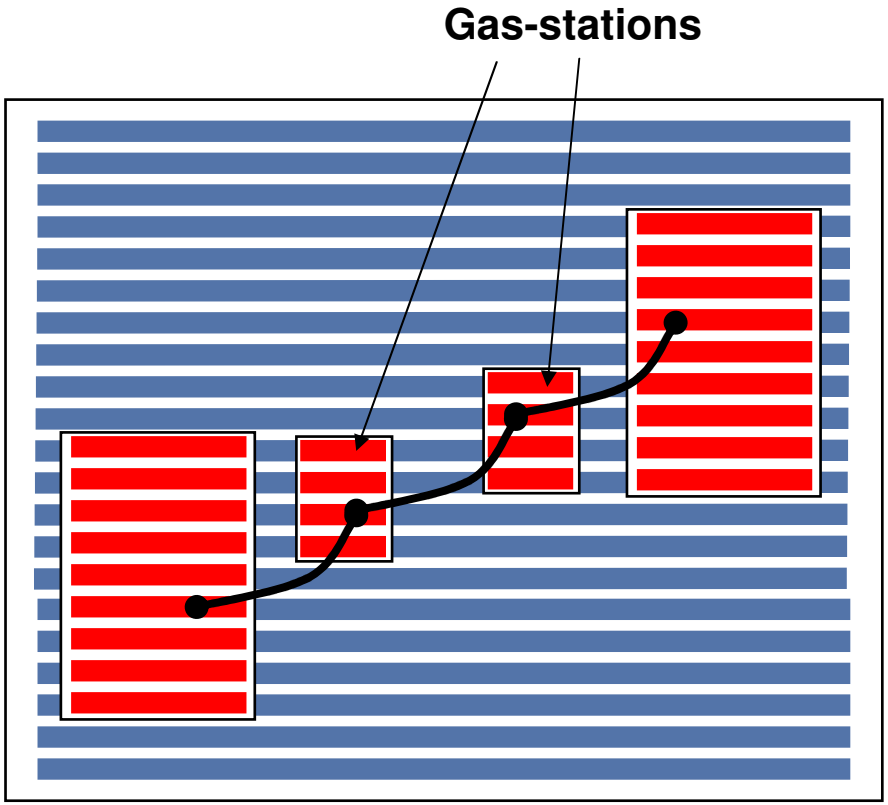
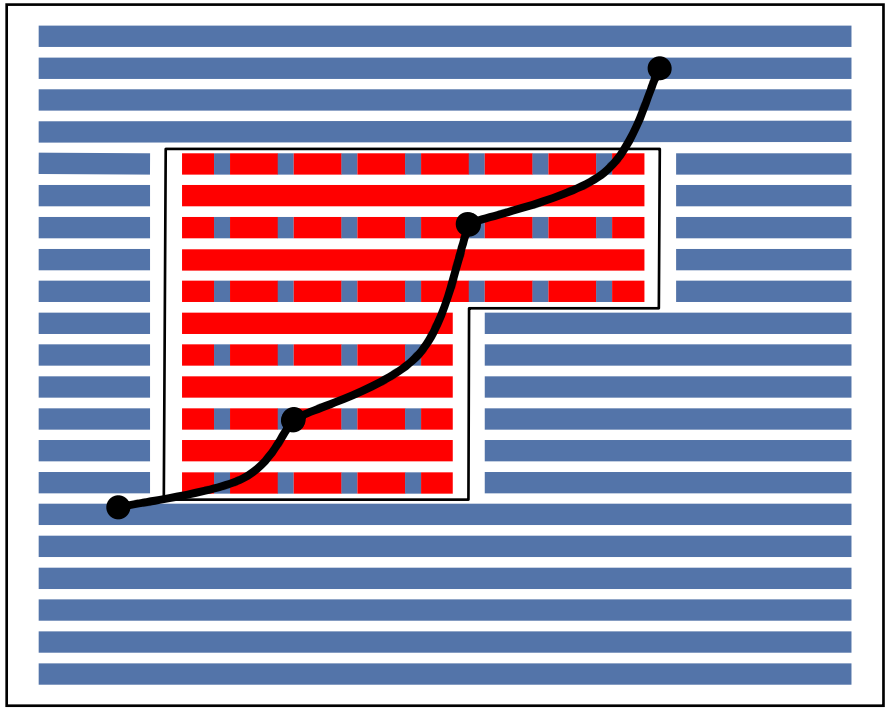
Floorplans and supply styles



Long-wire buffering in homogenous floorplans: gas-stations



Long-wire buffering in porous floorplans: parts of the cellrow have different rails

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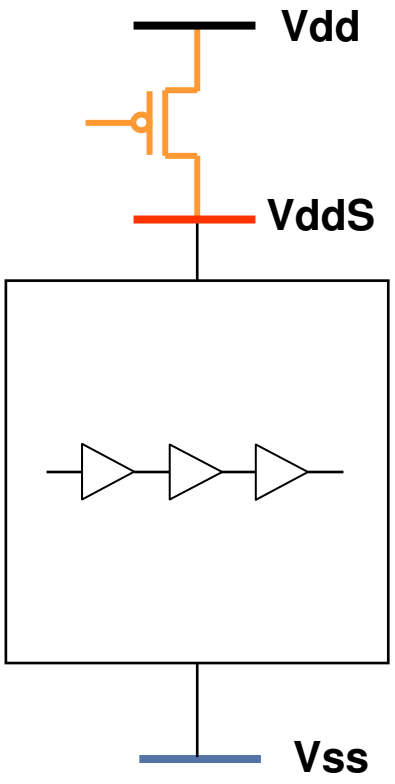
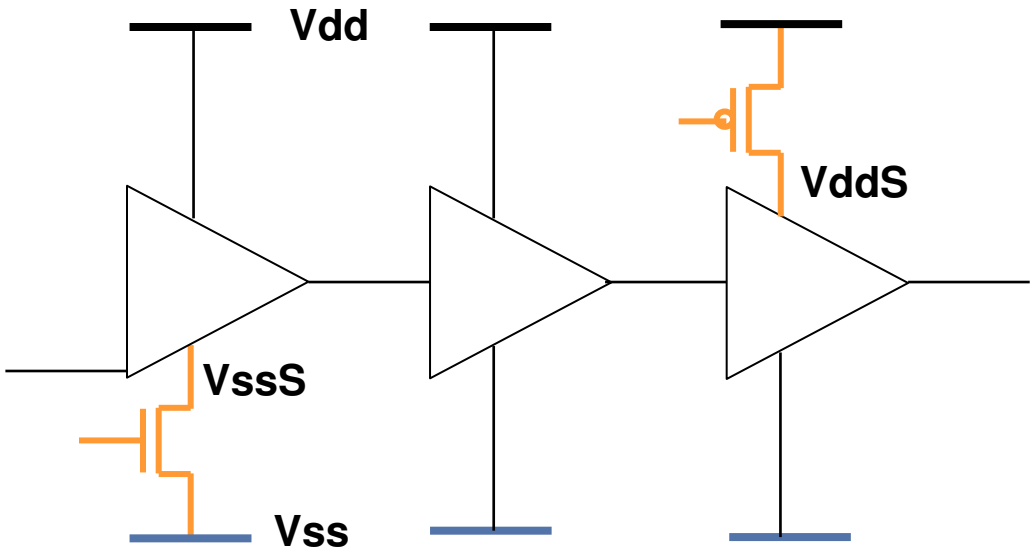
MTCMOS variants



Coarse grain MTCMOS



Fine grain MTCMOS

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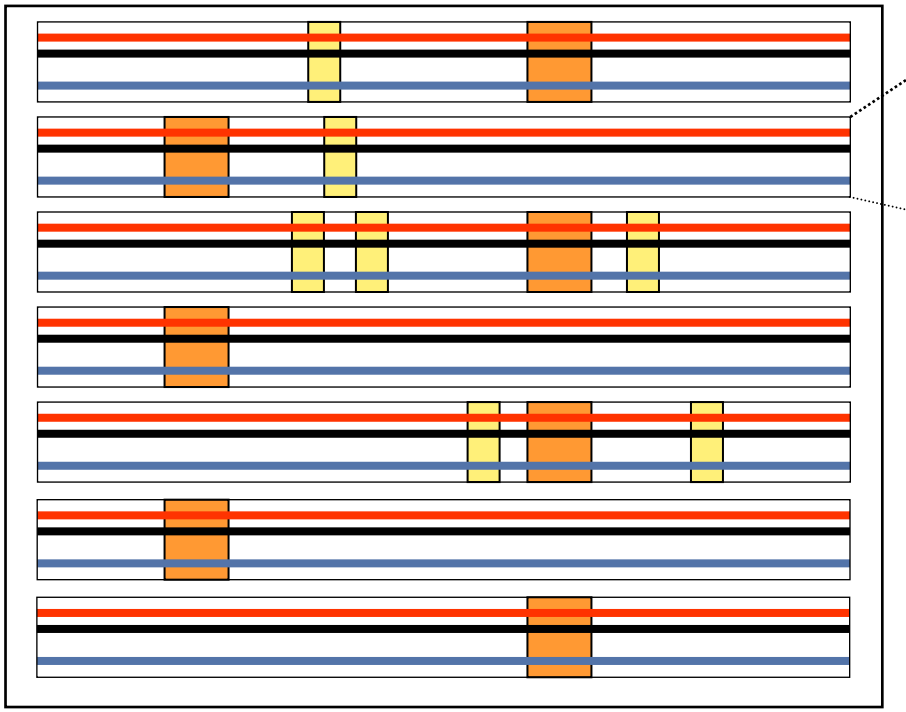
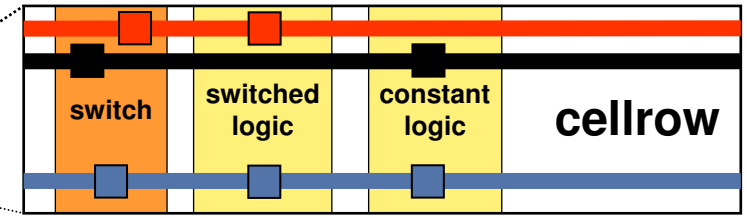
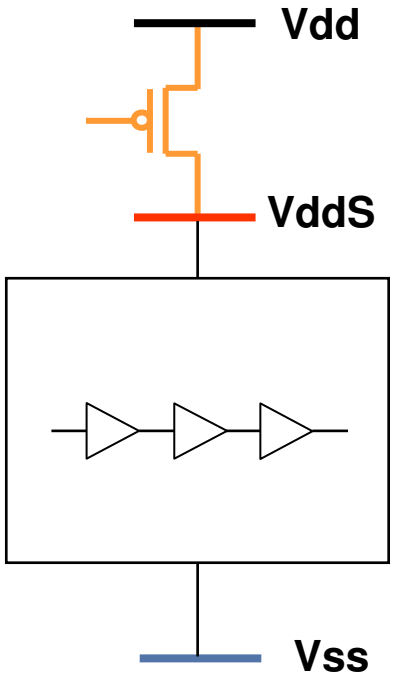
Floorplans and supply styles







Coarse grain MTCMOS

- **Constant and switched rails**
- **Regular logic**

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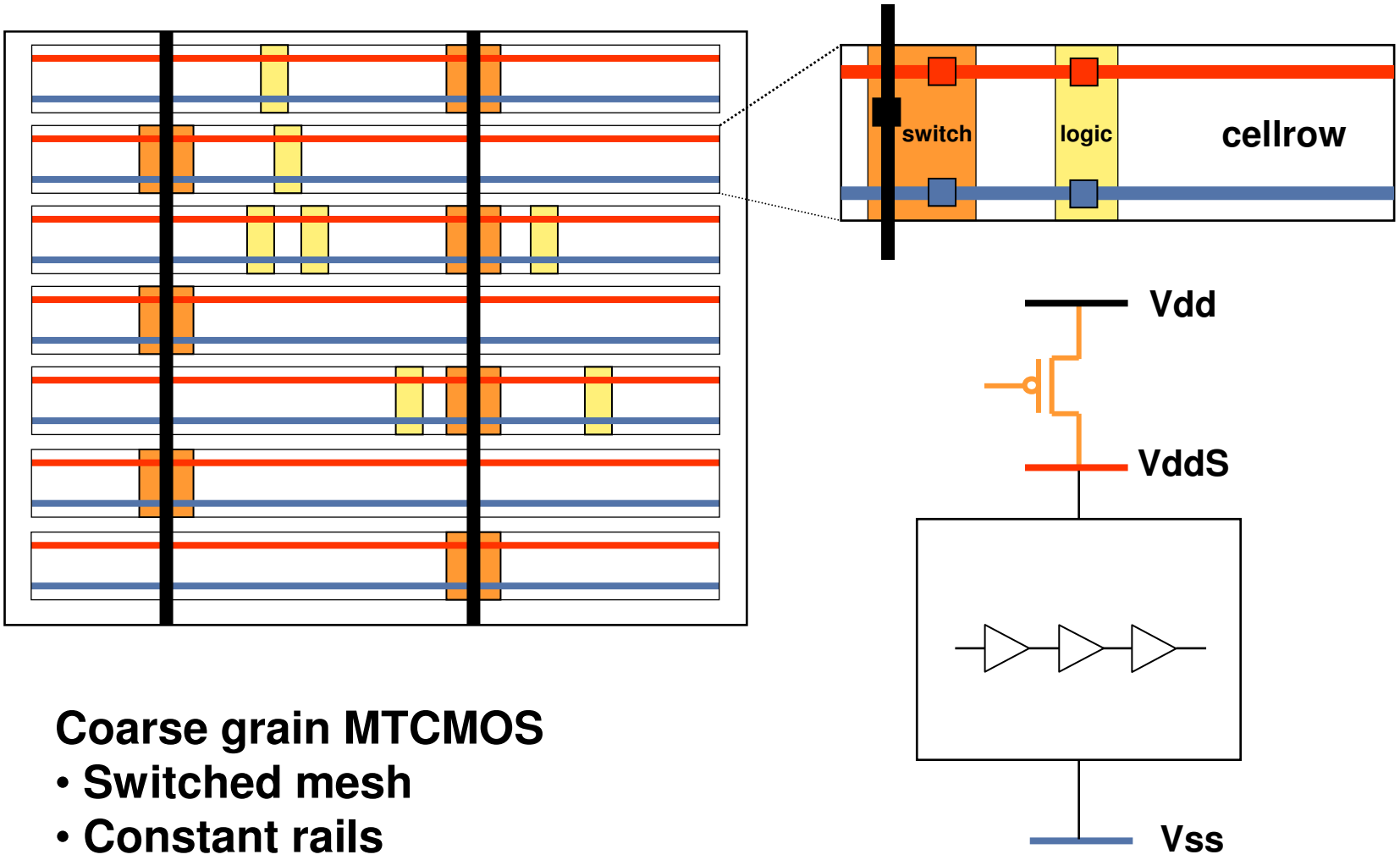
Floorplans and supply styles



Coarse grain MTCMOS

- **Switched mesh**
- **Constant rails**
- **Regular logic**

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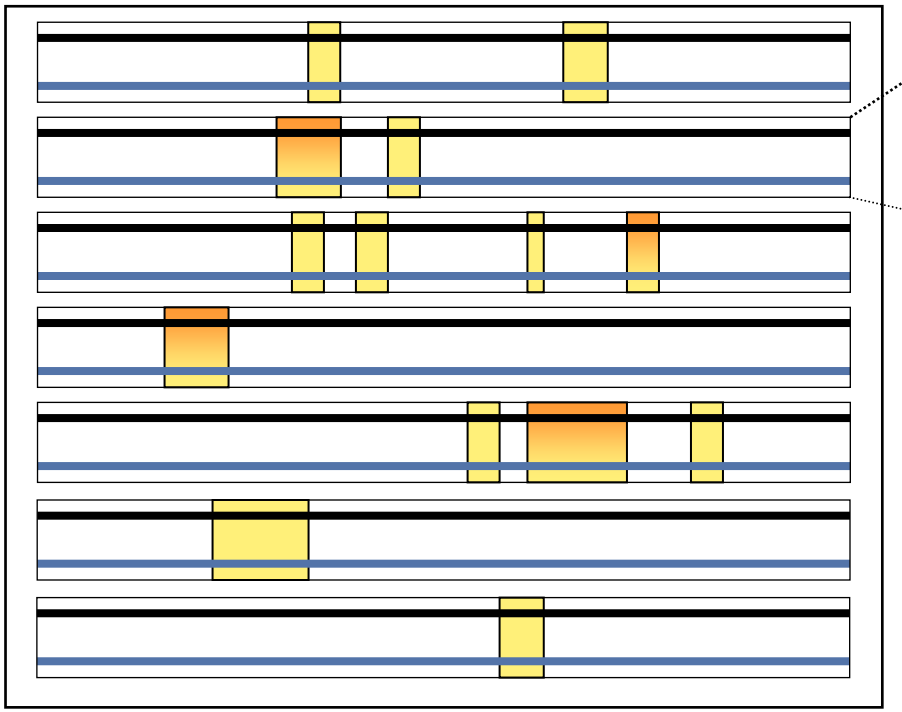
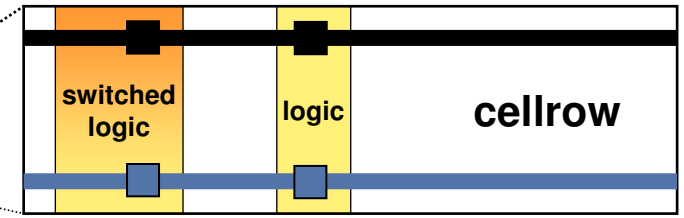
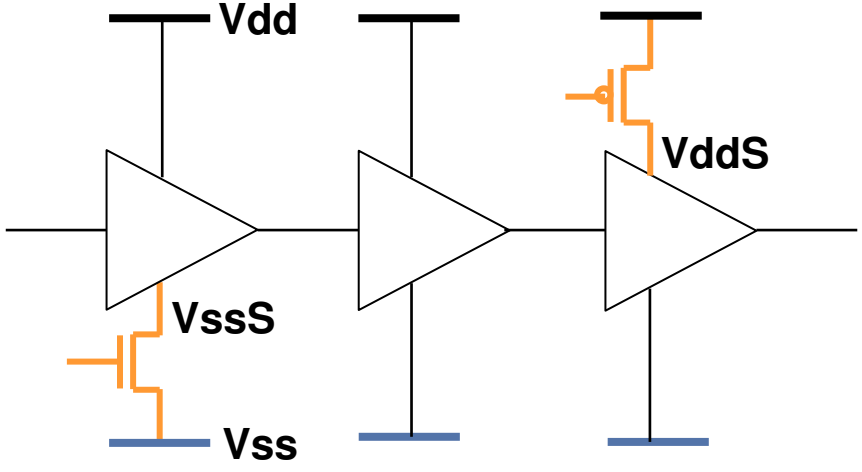
Floorplans and supply styles







Fine grain MTCMOS
- **Constant rails**
- **Regular & Switched logic**

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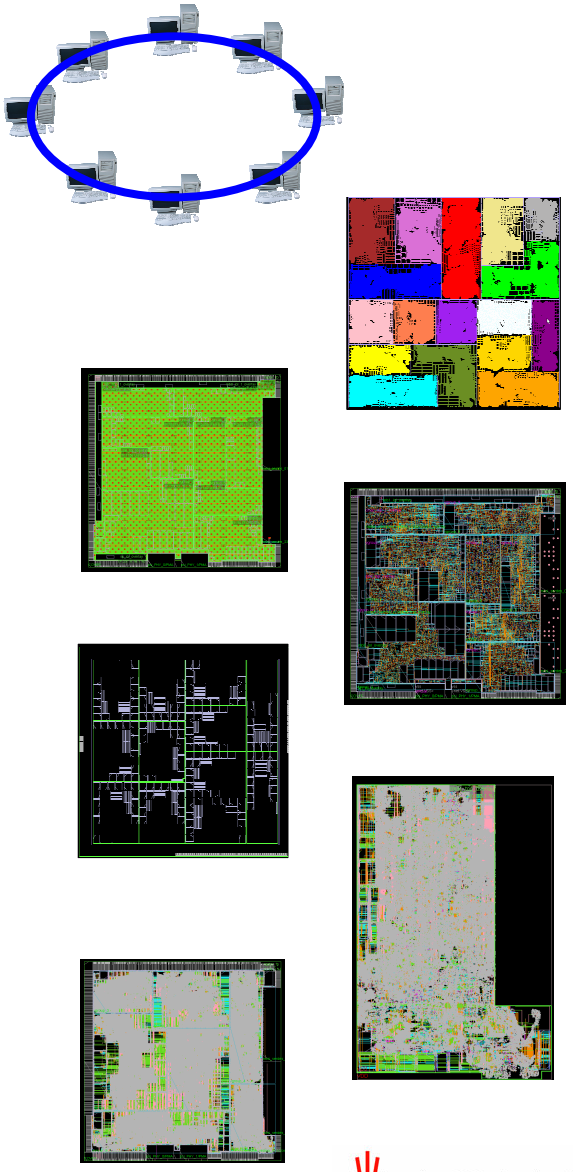
Talus – Magma's New Automation Technology

- Distributed RTL Synthesis
- Automated Partitioning and Shaping
- Automated Power Planning and Implementation
- Automated Clock Planning and Implementation
- Automated Time Budgeting
- Distributed Block Implementation
- Final Chip Assembly



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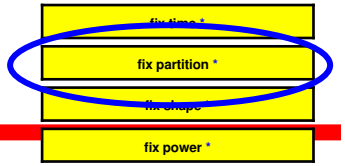
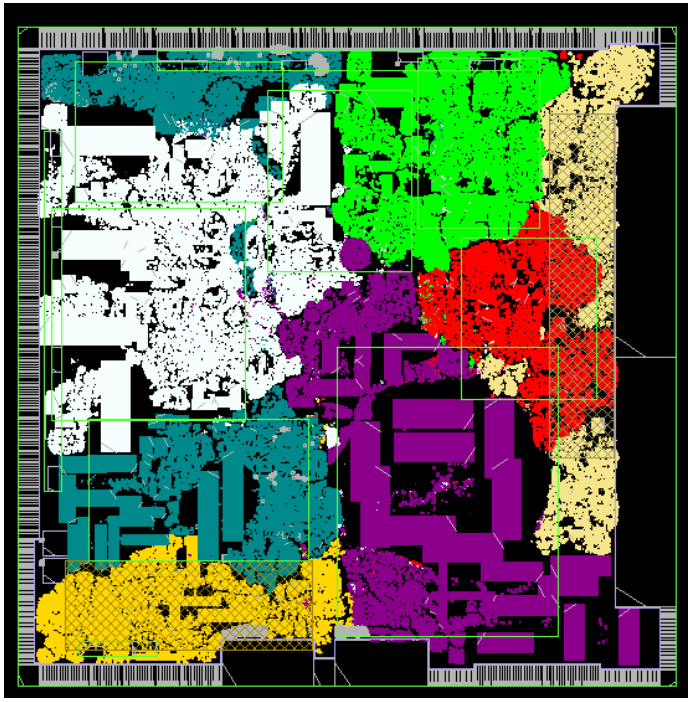
Automatic Physical Partitioning



Mapping logical hierarchy to physical hierarchy

- **Talus provides automatic partitioning**
  - allows appropriate sizes for closure flows
  - (re)grouping of attracted logic
  - **Distributes glue logic** into the partitions.
- **Use of "Overlays" guarantees that the original logical hierarchy can be extracted**



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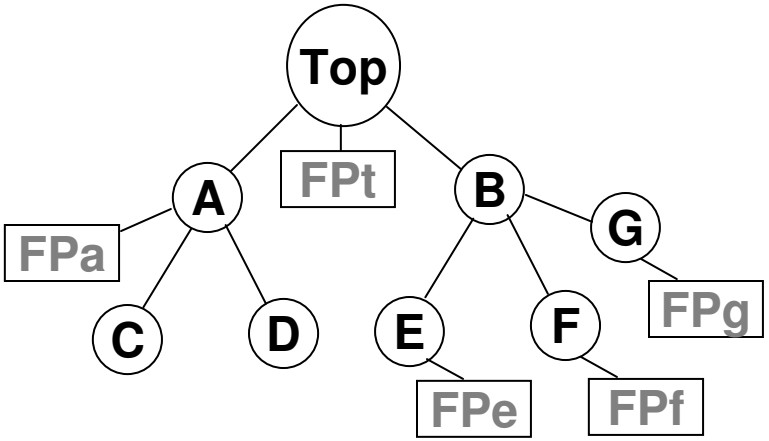
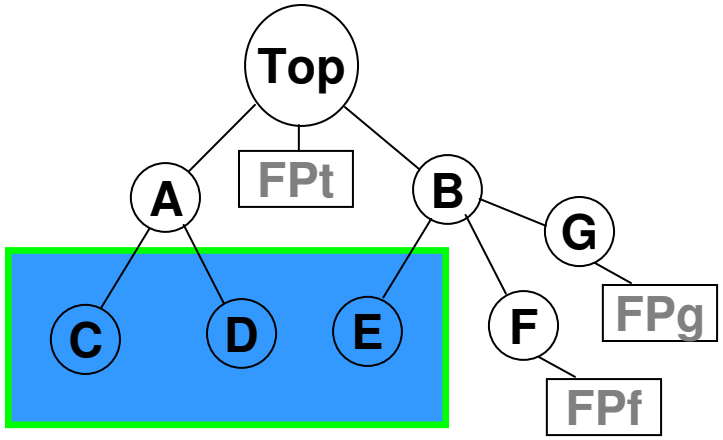
Logical Re-Partition of Hierarchy

Traditional Approach



- **Logical Hierarchy associated with floorplans directly**
  - Each partition is a level of the logical hierarchy, and user determines which level gets its own “physical hierarchy” or floorplan.

Talus Approach



- **Auto Partitioning determines what should be grouped**
  - After initial cluster placement
  - Cell proximity, block size and pin reduction are cost factors
  - Example: determines that cells C,D, and E should be grouped.

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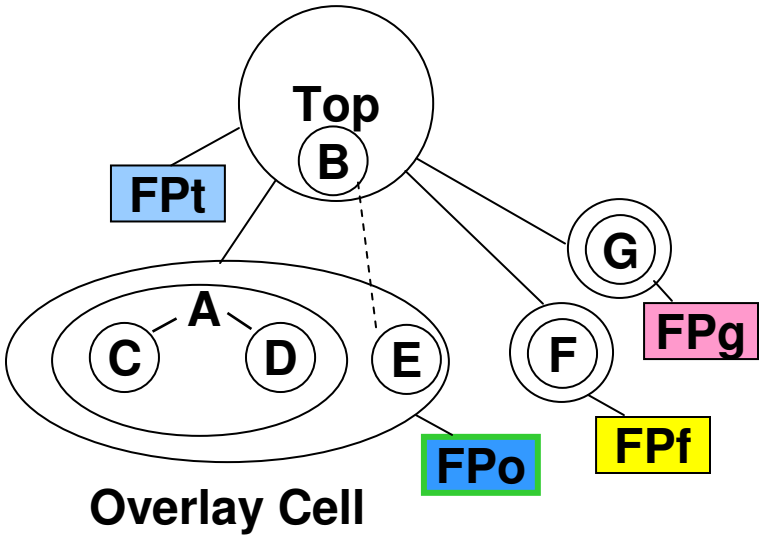
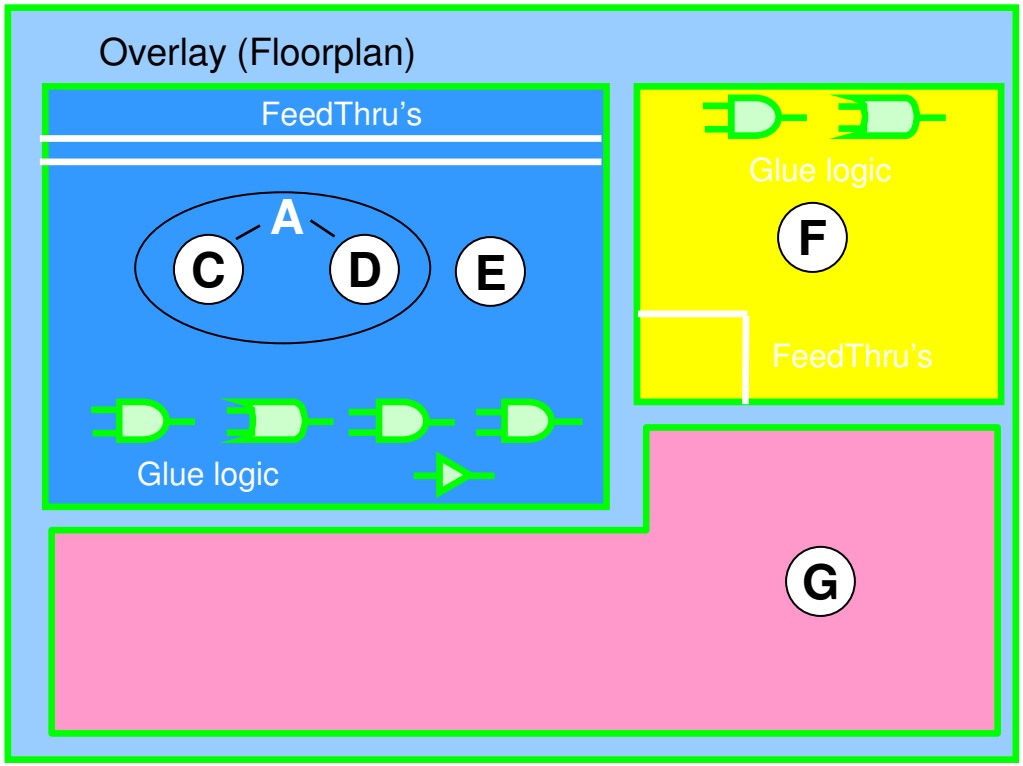
Partition Hierarchy (3 levels)

Talus Approach (Logical)



- **Overlay cell automatically generated for all partitions**
  - Multiple non-sibling cells can be instantiated in an overlay cell
  - Linked to single floorplan object
  - Original Cells are “maintained” for Verilog export

Talus Approach (Physical)



- **Physical hierarchy contains auto partitioned logical hierarchy**
  - Other logic will reside in Overlay cell, such as feedthroughs and glue logic

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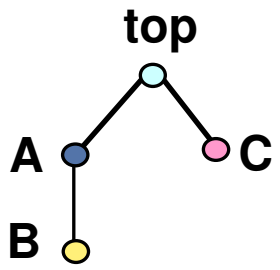
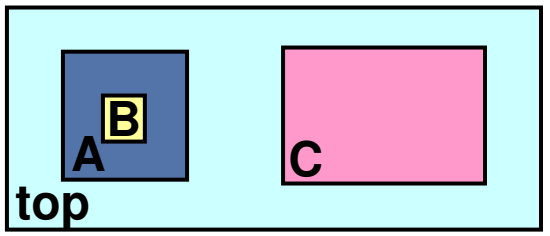
Freedom in physical hierarchy: Logic restructuring

- More and more customers are requesting the ability to allow the manipulation of physical hierarchy independently of logical hierarchy.
- This is required for a number of reason, for example the customer might have legacy blocks or receive IP that requires a different physical hierarchy.

Logical Hierarchy



Physical Hierarchy



- **Requirements for logical and physical hierarchies**
  - Each physical floorplan should map onto a single logical hierarchy.
  - Each floorplan must be contained within it's parent, i.e. B must be inside A which must be inside top.

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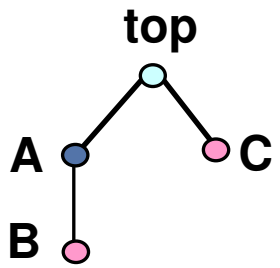
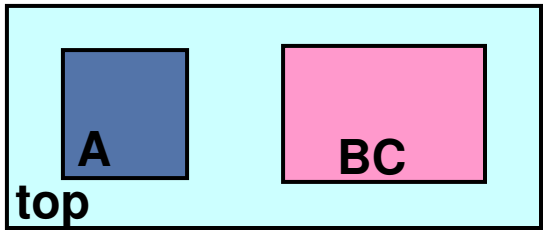
Non-sibling grouping

Logical Hierarchy



Physical Hierarchy



- The physical hierarchy shown above is one example of where the user wants break the parent sibling relationship.
- Content of both model B and model C should end up in a single floorplan BC. This is a violation of the siblings-only in a floorplan demand.

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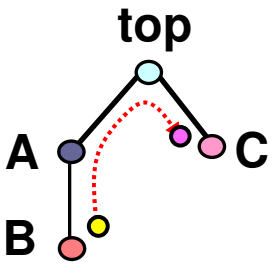
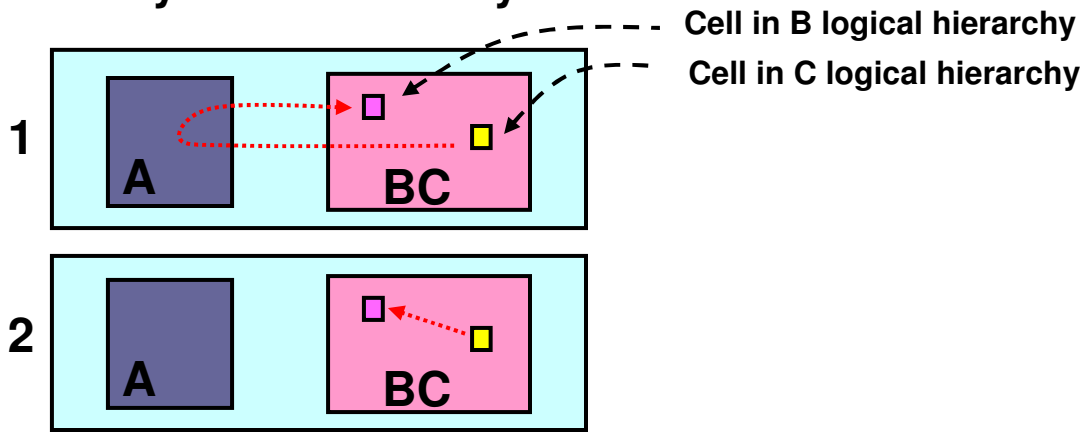
Non-sibling grouping

Logical Hierarchy



Physical Hierarchy



- The communication from the cell in model **B** to model **C** is shown both logically and physically in the above diagram.
- Obviously the physical connectivity shown in diagram **1** above isn't desired and would lead to a poor topology. Therefore we could modify this routing topology so that we have the physical topology shown in diagram **2**.
- *Basically, we let the global router connect the two cells by shortest path – no problem*
- Both of the above physical topologies wouldn't result in any modifications to the original logical hierarchy, even if a buffer had to be inserted in the path between the two cells.

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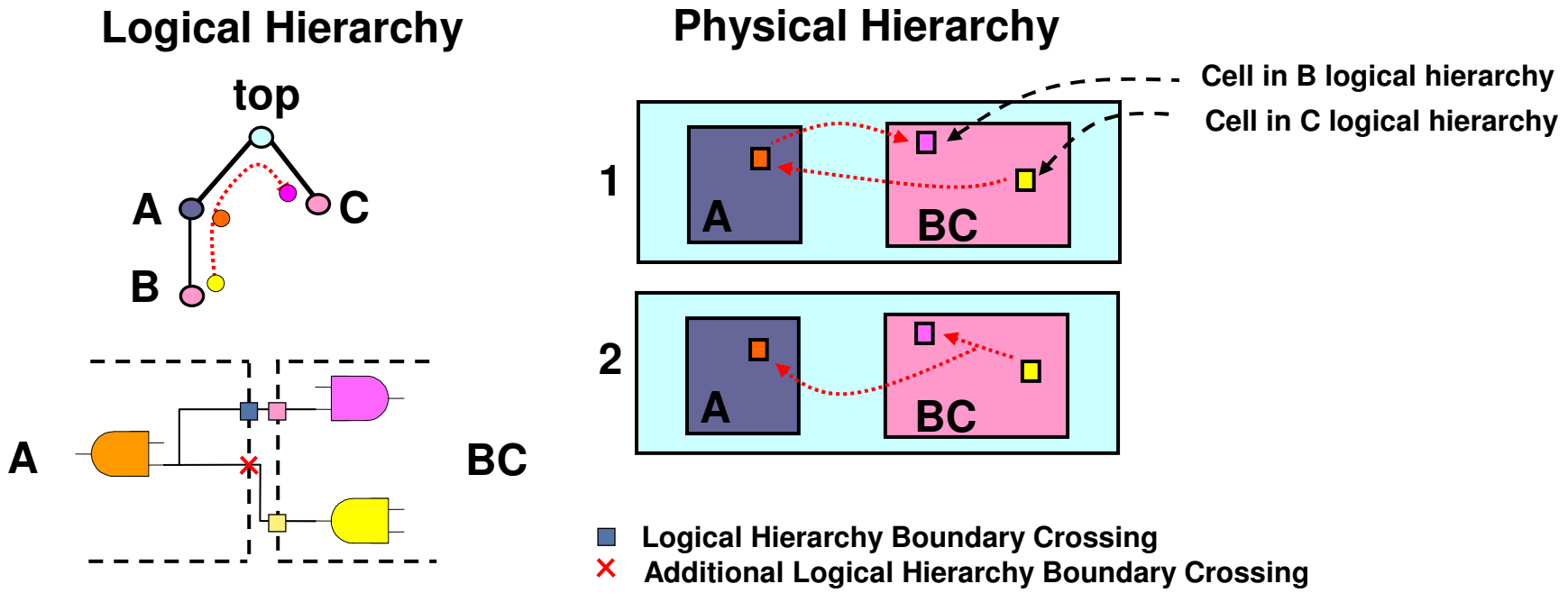
Non-sibling grouping



- This example is very similar to the previous example, but the connection to a cell in the model **A** imposes restrictions on the flexibility of the physical floorplan.
- *Note that we do need to insert an additional logical boundary crossing to 'fix' the physical hierarchy.*

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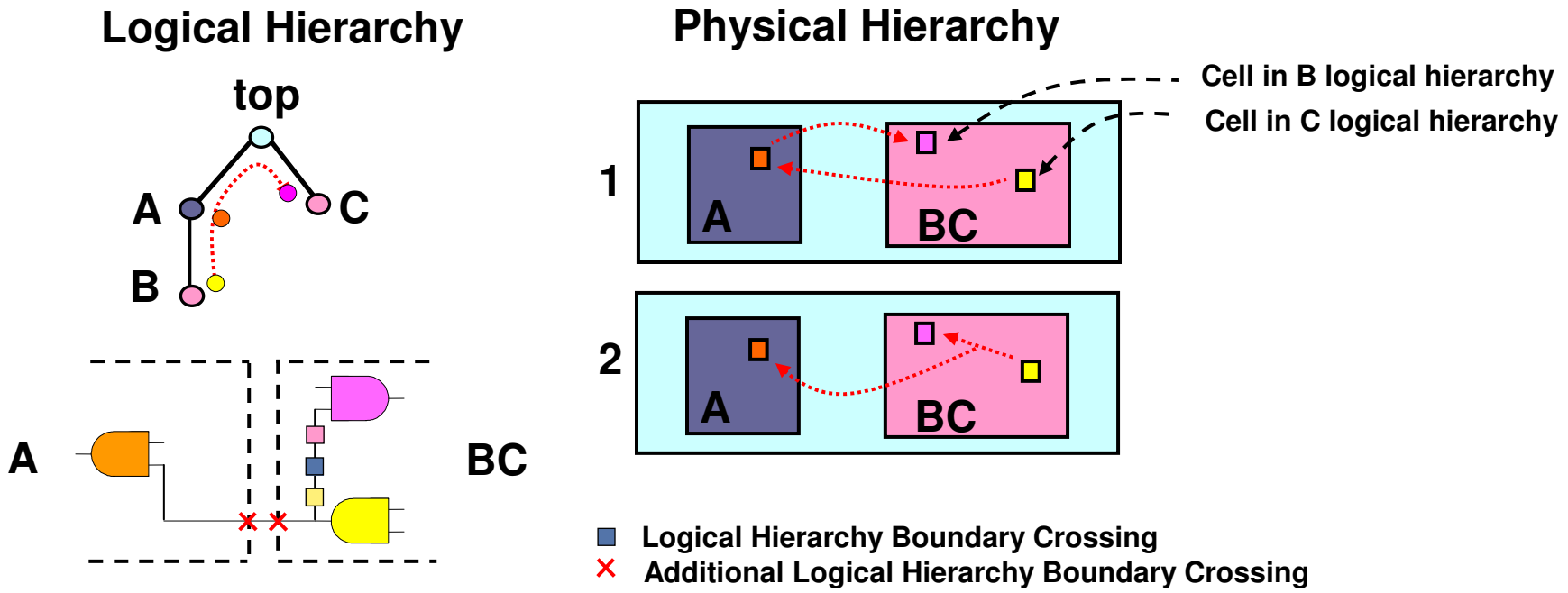
Non-sibling grouping



- If we want to achieve the routing topology shown in diagram 2, then we need to add more freedom.
- *This is like a 'physical boundary optimize', where we allow copying oflogical boundary corssings to give the router freedom to create such topology.*

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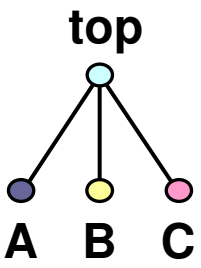
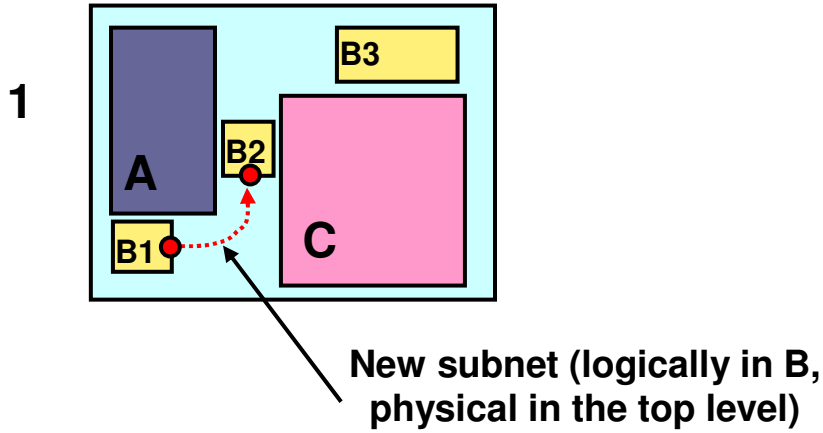
Distributed Floorplans

Logical Hierarchy



Physical Hierarchy



- **This diagram shows that the logical hierarchy for the B floorplan has been distributed over three physical floorplans (B1, B2 and B3).**
- **Two problems need to be solved**
  - (Automatic) Assignment of cells in B to either B1, B2 and B3
  - Routing and buffering of nets between B1…B3

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Summary

- **Power management typically governs design partitioning, both logically and physically**
  - A tight relation between logic and electrical boundaries seems a very pleasant property to continue to use current mapping technology
- **A semi-loose relation is possible between electrical partitioning and physical hierarchy**
- **Also, more freedom is desirable and possible between the logic hierarchy and physical hierarchy**
- **Requirement to automation the use of that freedom**

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