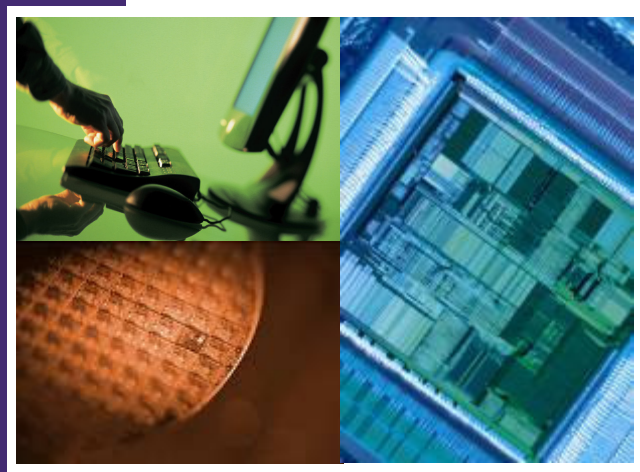
EDA To The Rescue Of The Silicon Roadmap

Monterey, April 12th, 2007



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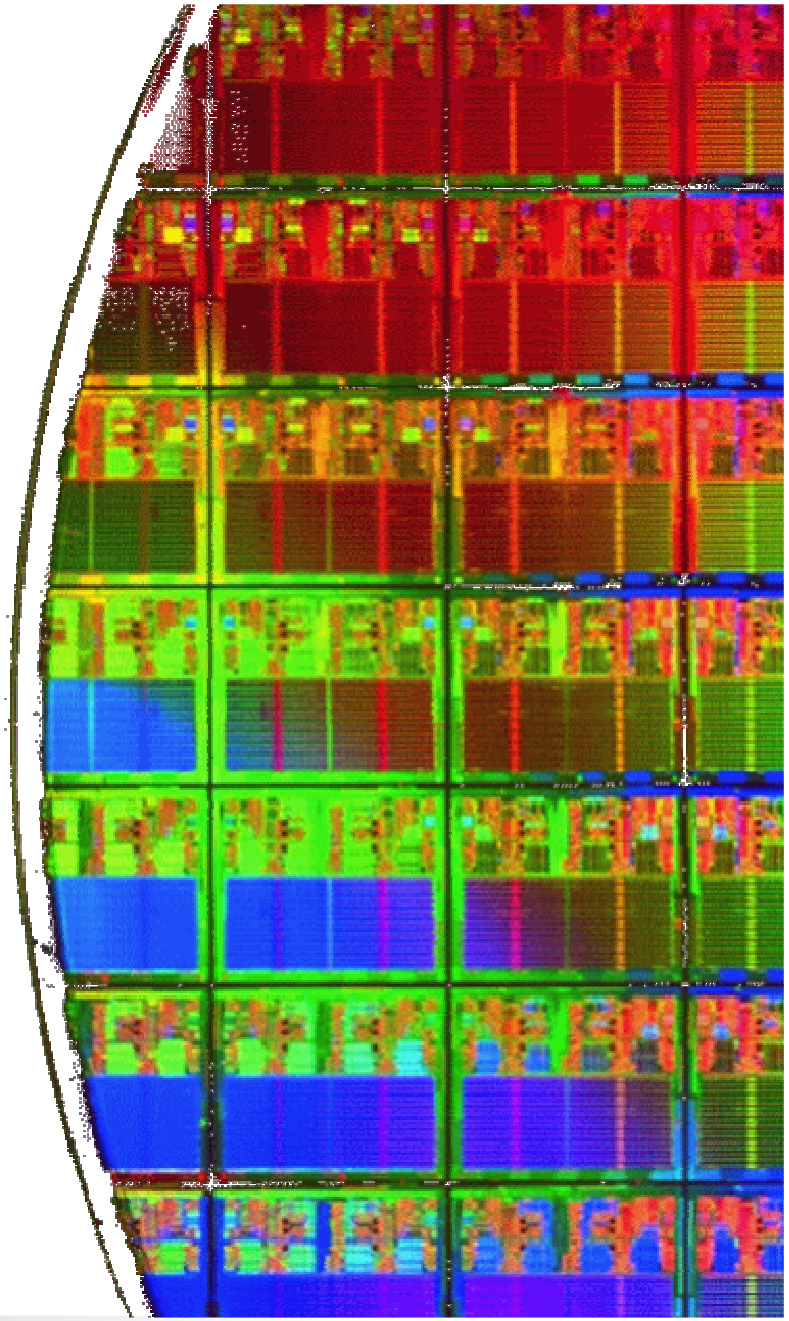
Predictable Success

Agenda

- **Rushing Or Holding?**
- Where Do We Stand?
- Design To The Rescue



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JUNCTION
ITRS
45
ITRS
250

The Era Of The Computer

"Only" 2 Billions Customers in the "Western" Countries

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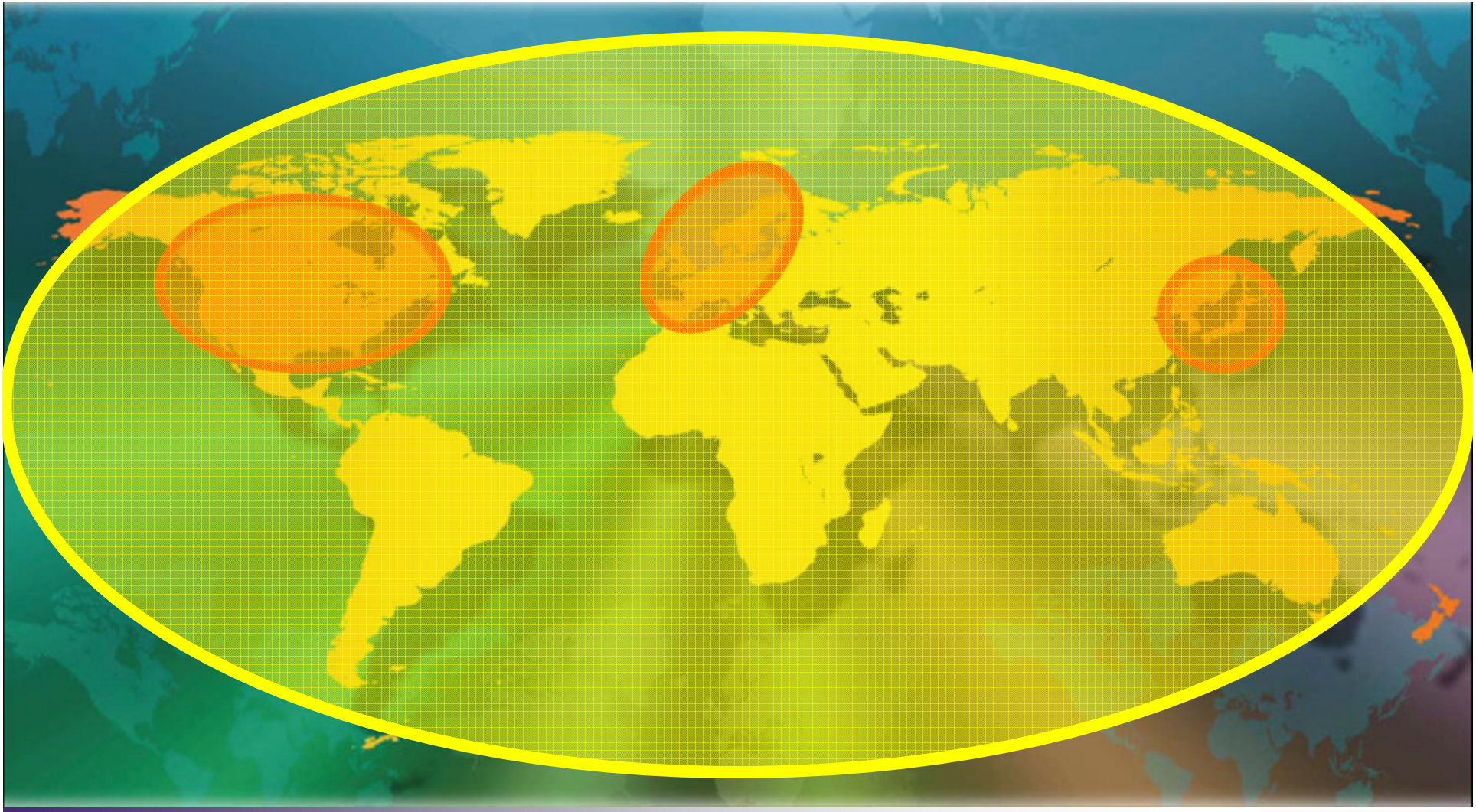
The Era Of The Consumer

More Than 6 Billions Customers All Over the World



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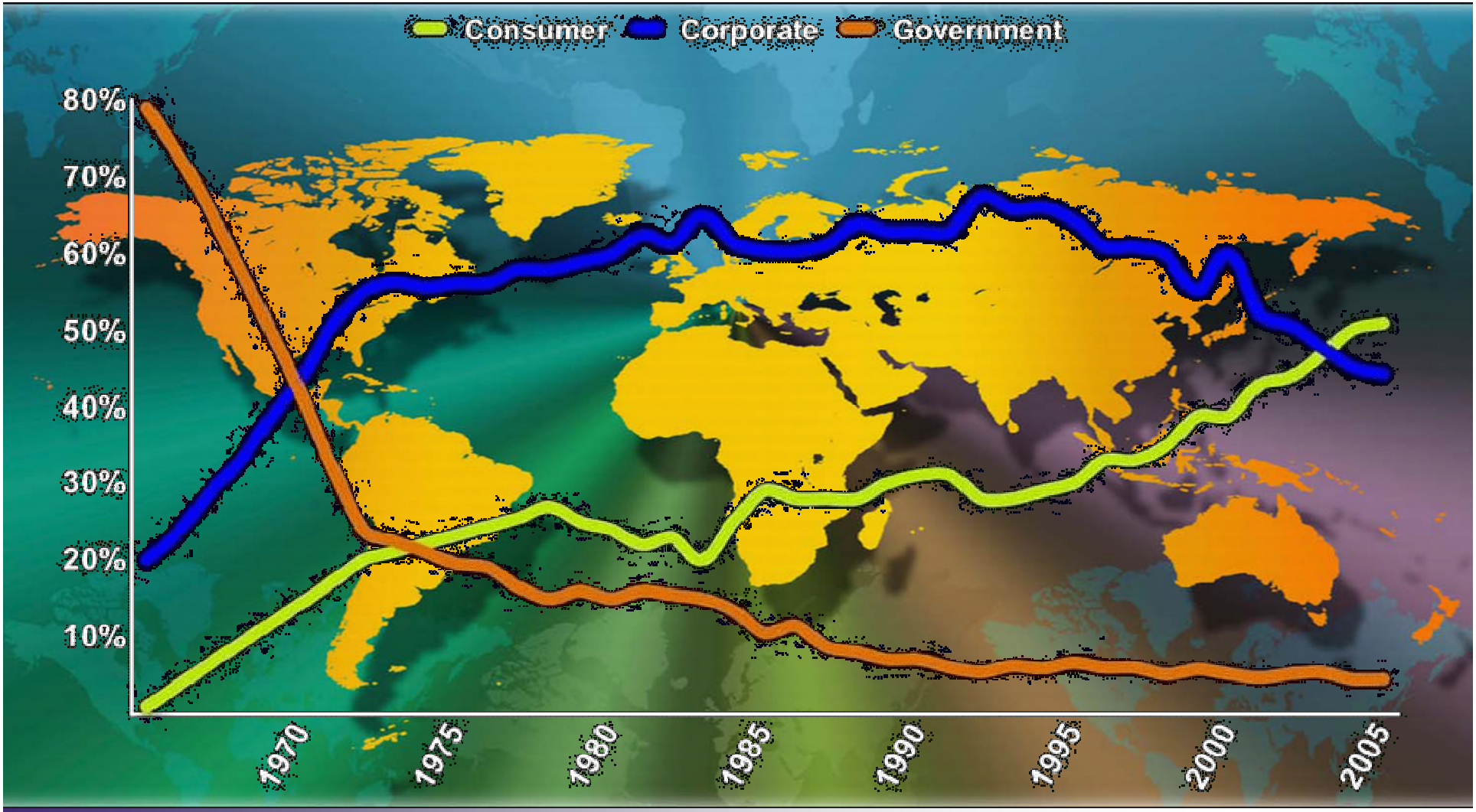
What Has Happened In Between?

Households, Semiconductor Industry's #1 Customer



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Source: J.-H. Huang, SIA 2004

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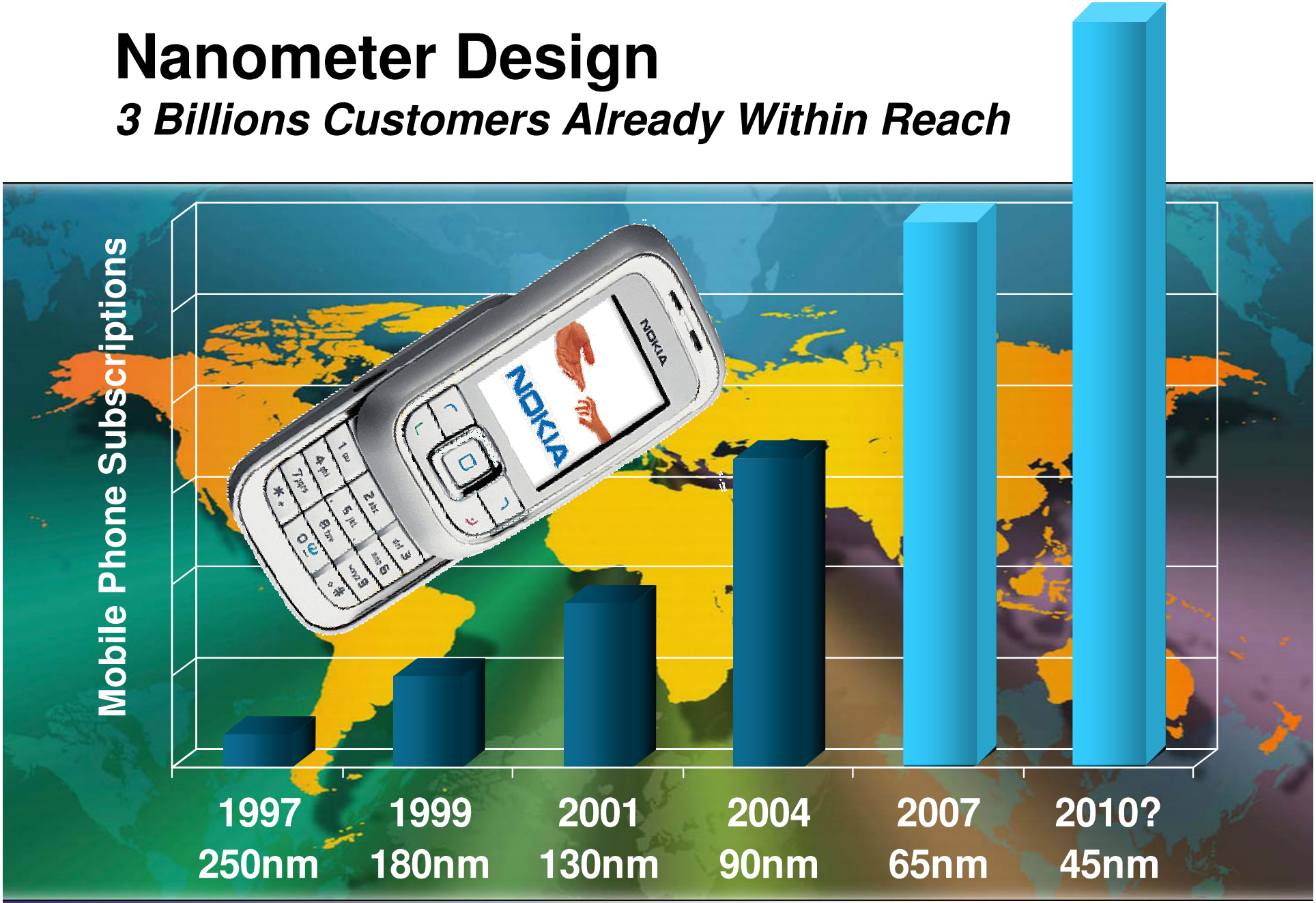
Nanometer Design

3 Billions Customers Already Within Reach



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Source: Nokia 2005

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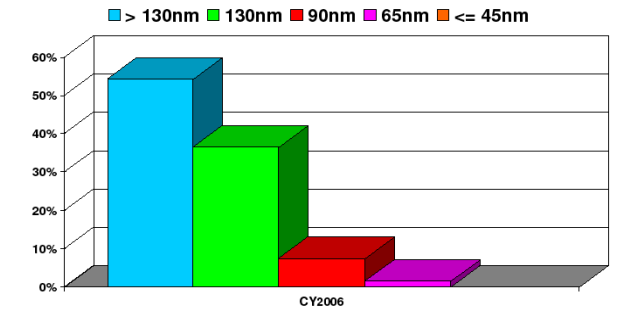
Nanometer Design

10% of Designs ⇨ 35% of Wafers ⇨ 60% of Resources

Design (Source: IBS)

In 2006 9% of New Designs' Starts @ 90nm and Below



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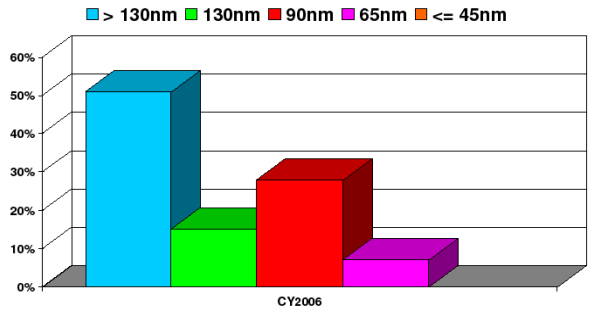
Manufacturing (Source: VLSI Research)

In 2006 35% of Wafers Out @ 90nm and Below



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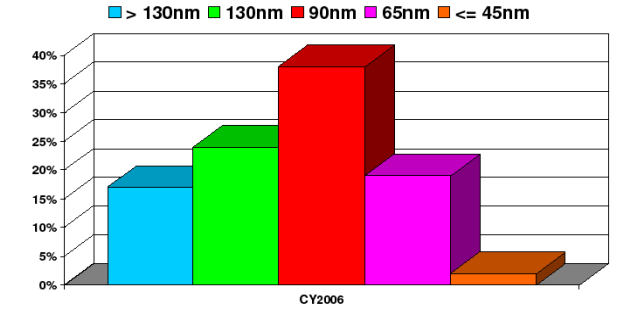
Engineering Effort (Source: SNUG'06)

In 2006 59% of Engineering Effort @ 90nm and Below



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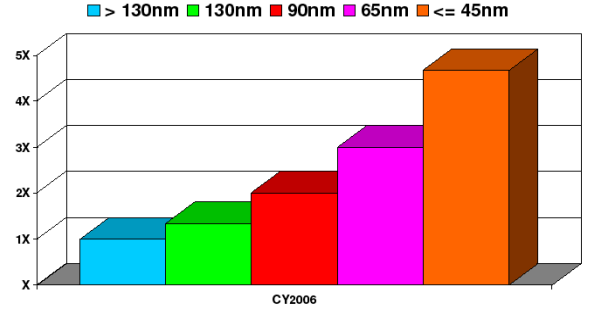
Revenue Requirements (Source: IBS)

Rule of 10: IC Revenue Must Be ≥ 10x Design Cost, and Product Revenue Must Be ≥ 10 x IC Revenue



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Nanometer Design

Few Products Qualify, Volume and Cost Rule

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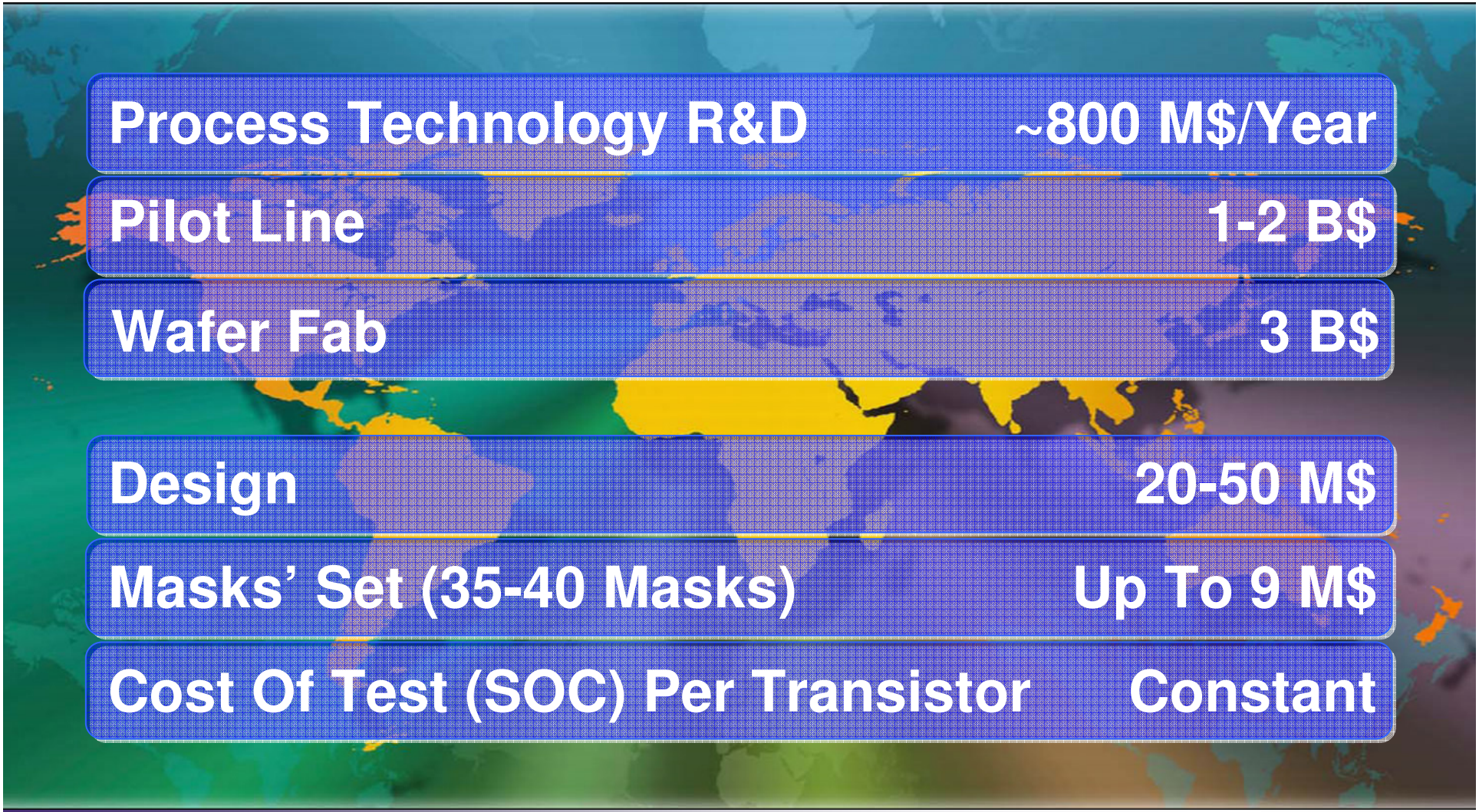
The Economy Of Scale

45nm Technology, 300mm Manufacturing



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Source: A. Bryant, Intel 2005, IBS 2005, ITRS 2005

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Very Few Can Afford The Cost!

Minimum Revenue 8.3B$ @ 65 Nanometers in 2004 & 17% 2005-2007 CAGR Required, Just to Stay Afloat

2004 Rank	2005 Rank	Company	Revenue	2004 Revenue	Percent Change	Percent of Total	Cumulative Percentage
1	1	Intel	$35,466	$31,396	13.0%	15.0%	15.0%
2	2	Samsung Electronics	$17,210	$15,759	9.2%	7.3%	22.2%
3	3	Texas Instruments	$10,745	$10,225	5.1%	4.5%	26.7%
7	4	Toshiba	$9,077	$8,752	3.7%	3.8%	30.6%
6	5	STMicroelectronics	$8,881	$8,760	1.4%	3.7%	34.3%
4	6	Infineon Technologies	$8,297	$9,180	-9.6%	3.5%	37.8%
5	7	Renesas Technology	$8,266	$9,000	-8.2%	3.5%	41.3%
8	8	NEC Electronics	$5,710	$6,503	-12.2%	2.4%	43.7%
9	9	**NXP Semiconductors**	$5,646	$5,692	-0.8%	2.4%	46.1%
10	10	Freescale Semiconductor	$5,598	$5,519	1.4%	2.4%	48.5%
14	11	Hynix	$5,560	$4,606	20.7%	2.3%	50.8%
13	12	Micron Technology	$4,775	$4,649	2.7%	2.0%	52.8%
15	13	Sony	$4,574	$4,299	6.4%	1.9%	54.7%
12	14	Matsushita Electric	$4,131	$4,669	-11.5%	1.7%	56.5%
11	15	Advanced Micro Devices (AMD)	$3,917	$5,108	-23.3%	1.7%	58.1%
17	16	Qualcomm	$3,457	$3,211	7.7%	1.5%	59.6%
16	17	Sharp Electronics	$3,266	$3,488	-6.4%	1.4%	61.0%
18	18	Rohm	$2,909	$2,849	2.1%	1.2%	62.2%
20	19	IBM Microelectronics	$2,792	$2,503	11.5%	1.2%	63.4%
22	20	Broadcom	$2,671	$2,400	11.3%	1.1%	64.5%
		Other Companies	$84,191	$80,241	4.9%	35.5%	100.0%
		Total Revenue	**$237,139**	**$228,809**	**3.6%**	**100.0%**	

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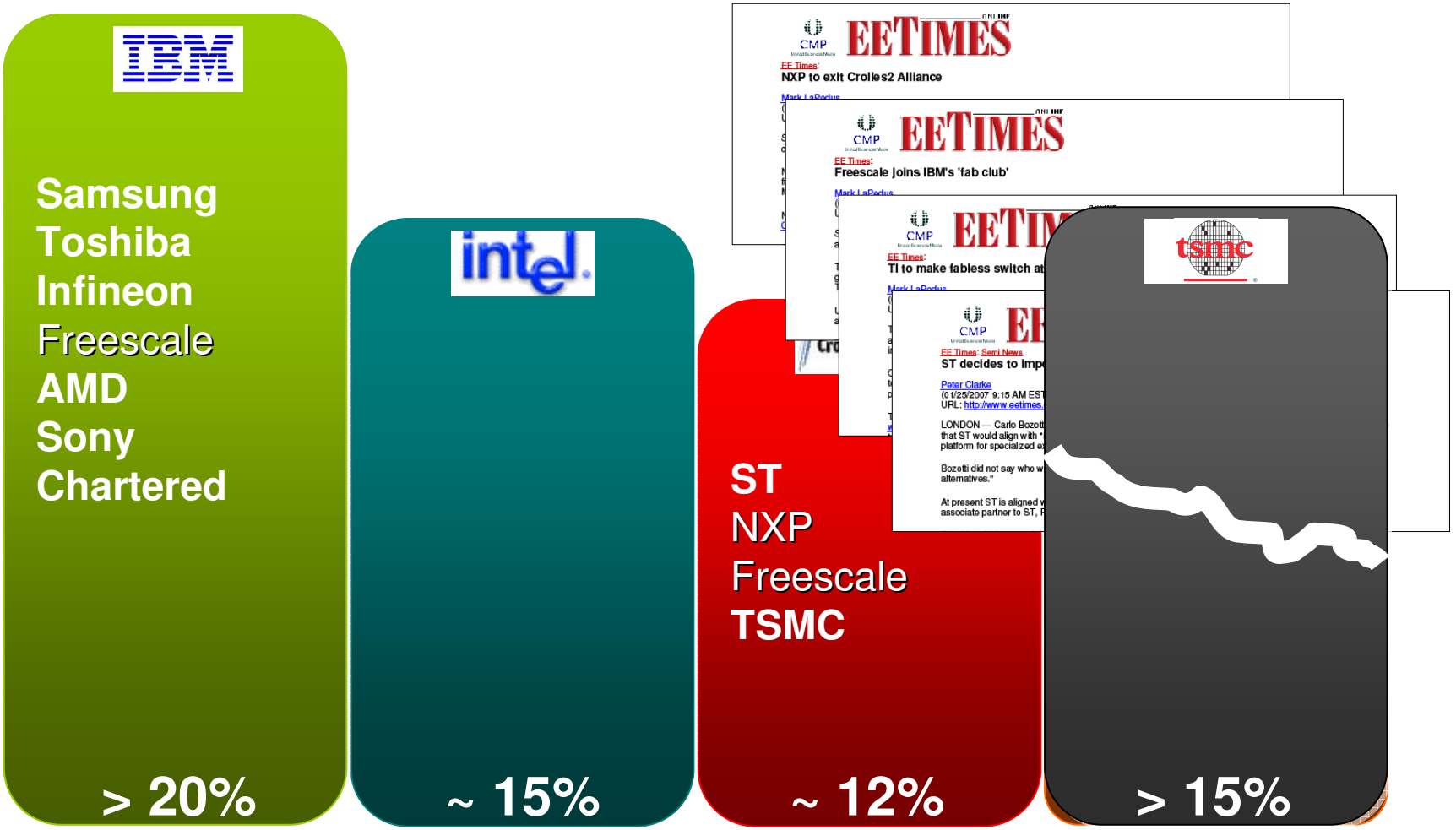
Source: IBS 2005; iSuppli 2006

Technology Alliances And Lone Stars

@ 45nm and Below and their Share of the 2005 Semiconductor Market (237 B$)



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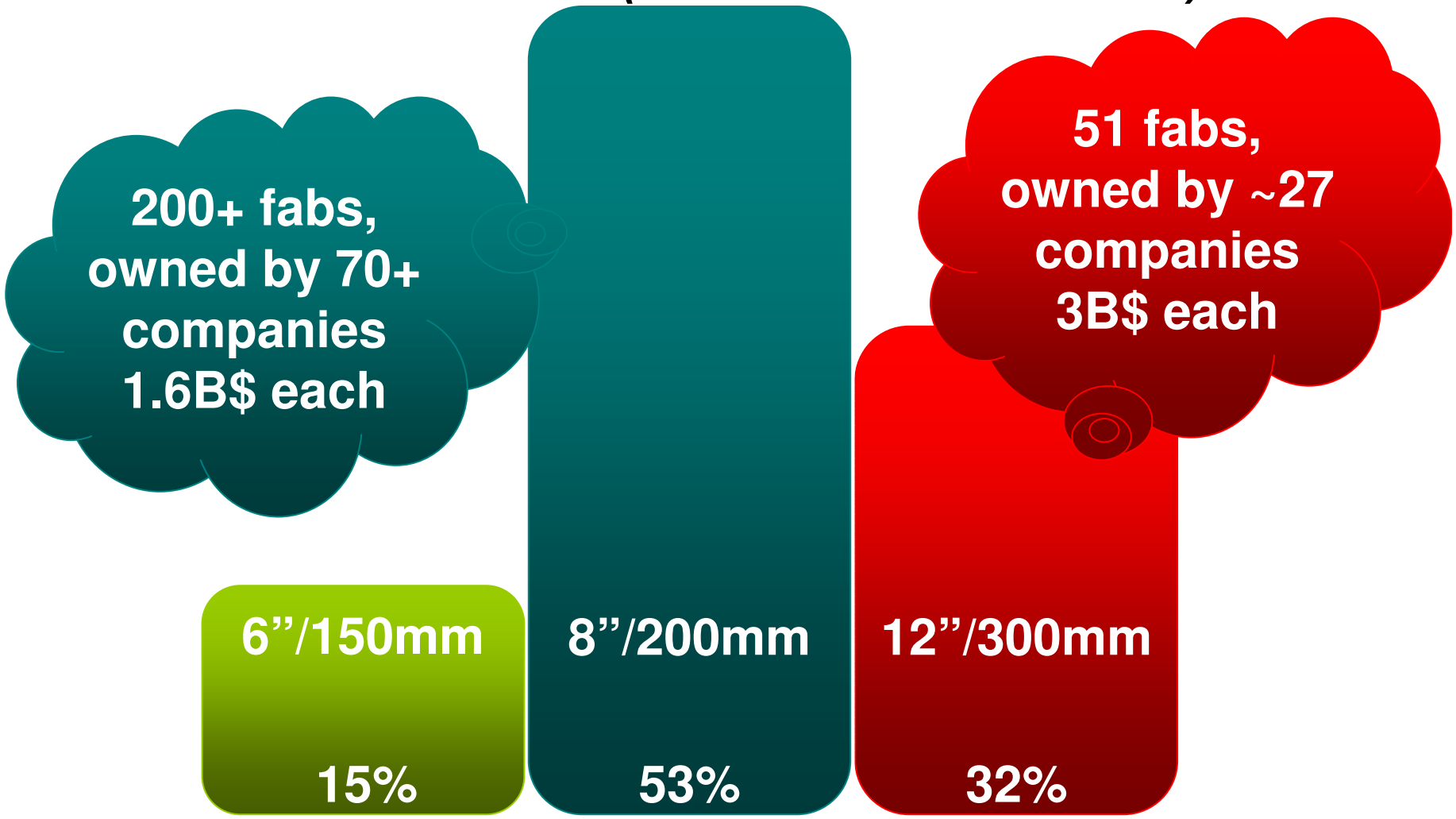
Source: iSuppli 2006

Manufacturing Clubs

300mm vs. 200mm and their Share of the 2005 Semiconductor Market (4.3 km² of Wafers Area)



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Source: IC Insights 2007, VLSI Research 2006

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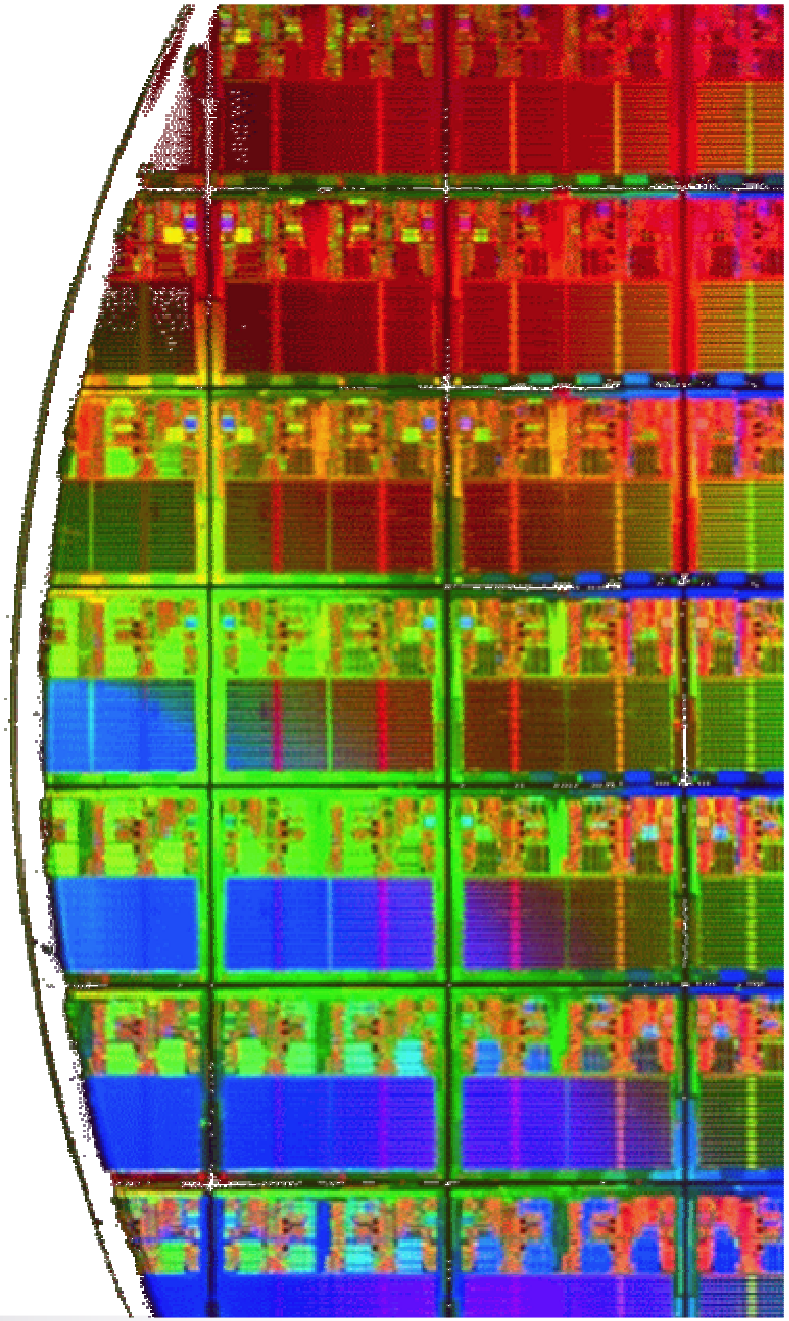
Agenda

- Rushing Or Holding?
- **Where Do We Stand?**
- Design To The Rescue



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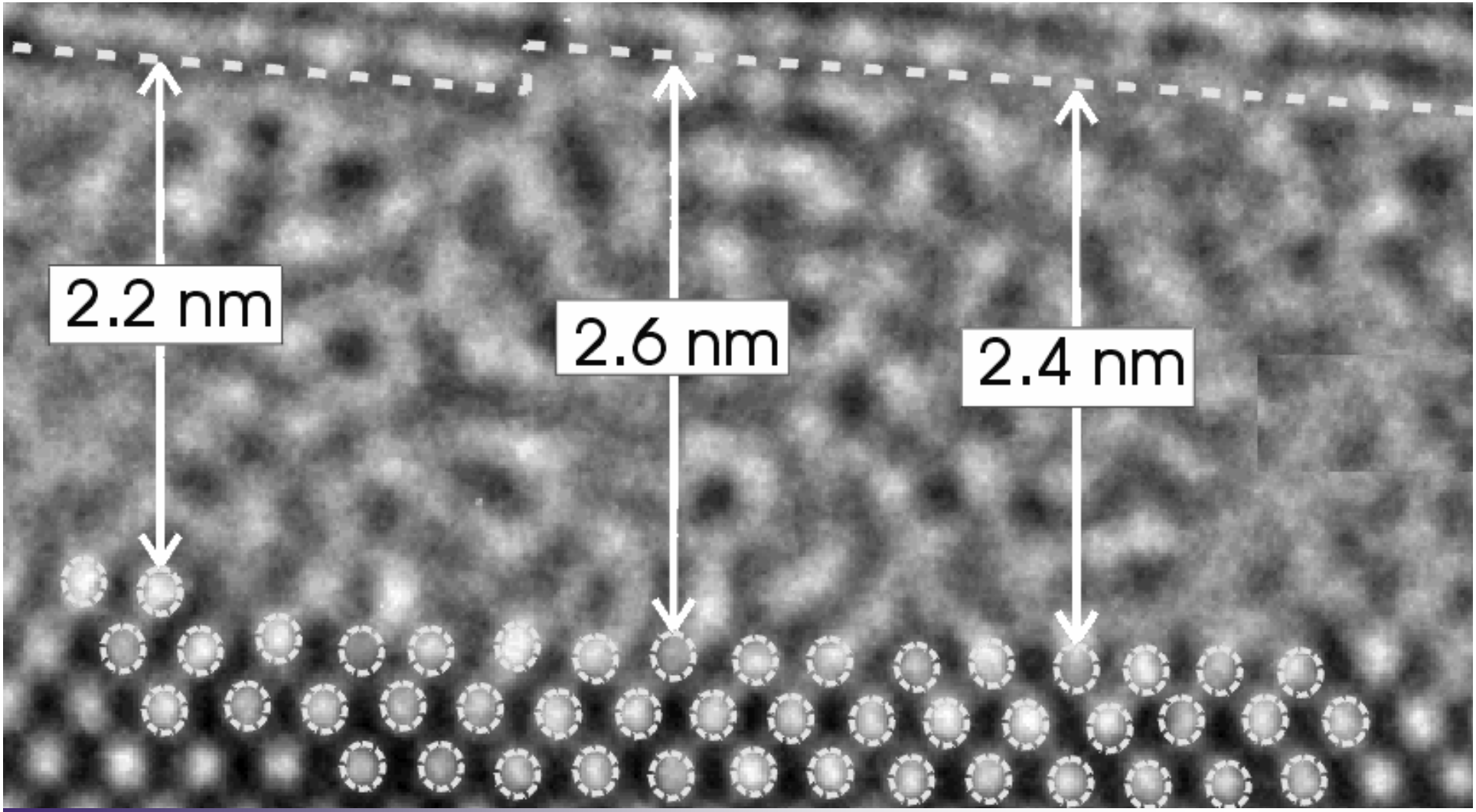
Nanometer Design

Molecules (& Atoms) Make The Difference



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© C. Visweswariah, IBM 2004, ITRS 2005

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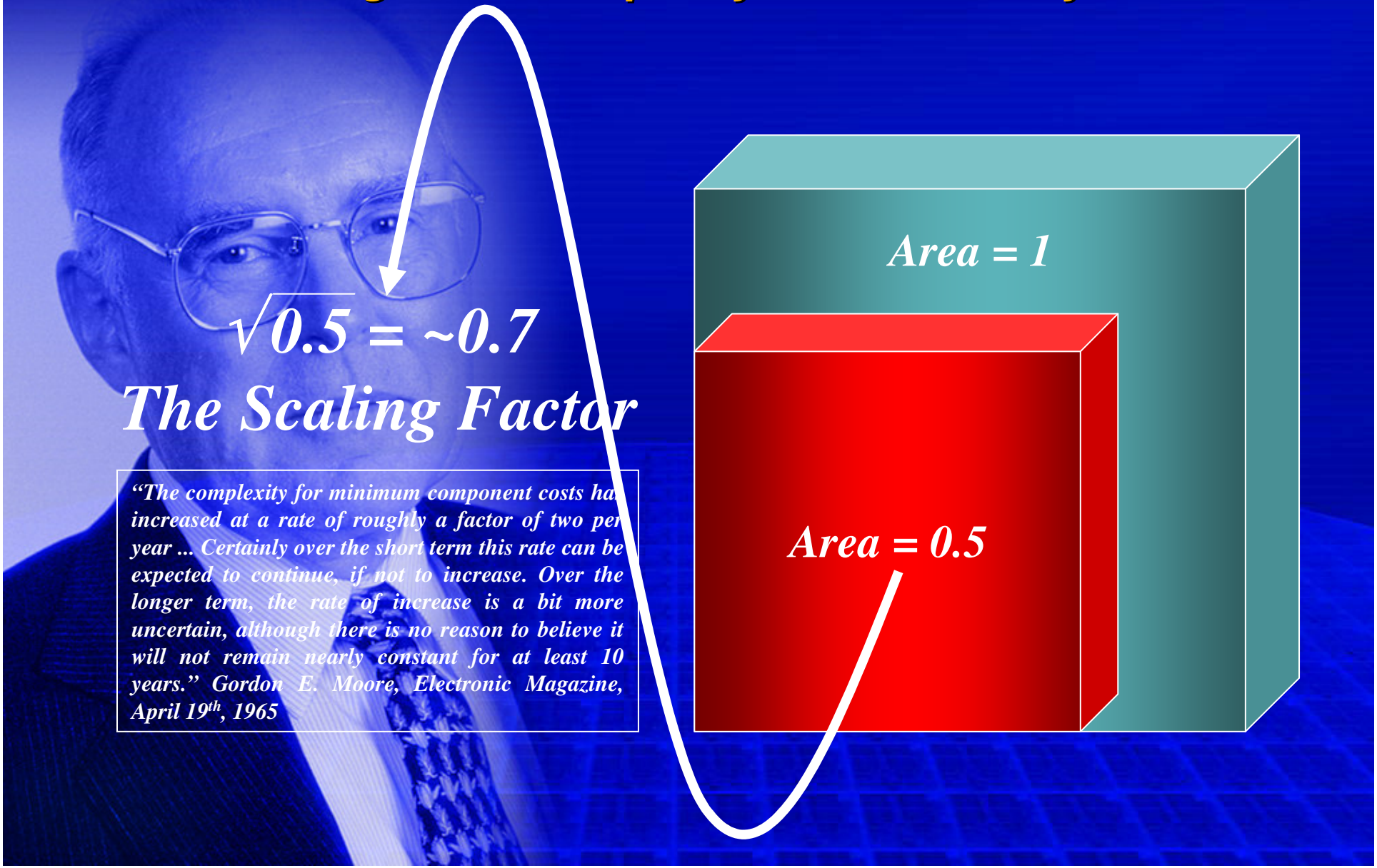
Dr. Gordon E. Moore's Law

Integration's Capacity Doubles Every Year



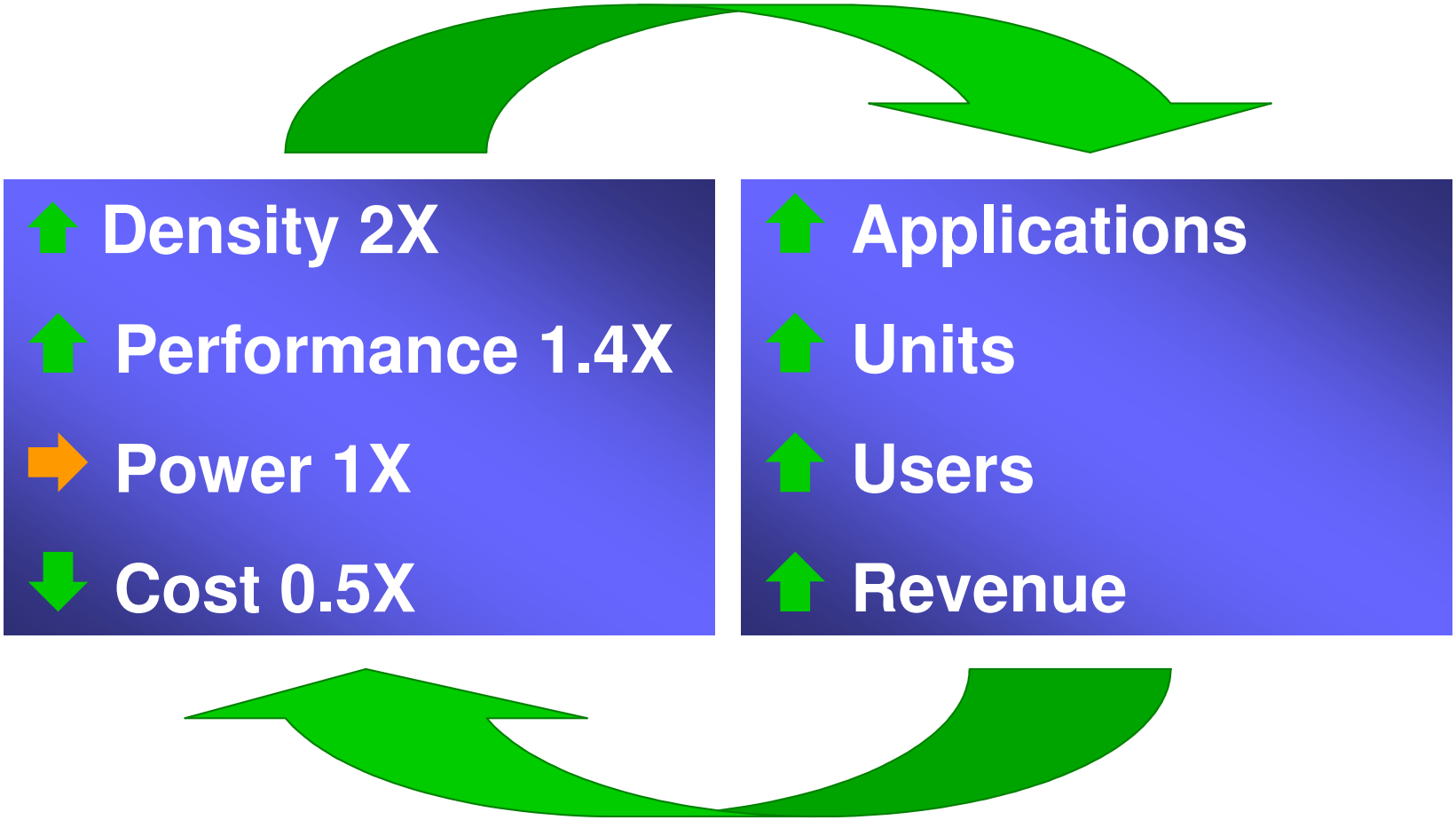
$$\sqrt{0.5} = \sim 0.7$$

The Scaling Factor

"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year ... Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years." Gordon E. Moore, Electronic Magazine, April 19th, 1965

Semiconductor Industry Cycle

Technology Advances, Market Grows



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The Signs of Crisis Are Visible Already

Voltage Is Breaking the Rules of Scaling

Source: ITRS 2005	90nm	65nm	45nm
Device Length (nm) ⇩	1x	0.7x	0.5x
Delay (ps) ⇩	1x	0.7x	0.5x
Frequency (GHz) ⇧	1x	1.43x	2x
Integration Capacity (BTx) ⇧	1x	2x	4x
Capacitance (fF) ⇩	1x	0.7x	0.5x
Die Size (mm^2) ⇨	**1x**	**1x**	**1x**
Voltage (V) ⇘	**1x**	**0.85x**	**0.75x**
Dynamic Power (W) ⇘	**1x**	**> 0.7x**	**> 0.5x**
Manufacturing (microcents/Tx) ⇩	1x	0.35x	0.12x

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The [not so] Hidden Costs of Scaling

New Materials [and Devices] Are Badly Needed

Source: ITRS 2005	90nm	65nm	45nm
V_{TH} (V) ⇘	**1x**	**.85x**	**.75x**
I_{OFF} (nA/um) ⇧⇧	**1x**	**~3x**	**~9x**
Dynamic Power Density (W/cm²) ⇧	**1x**	**1.43x**	**2x**
Leakage Power Density (W/cm²) ⇧⇧	**1x**	**~2.5x**	**~6.5x**
Power Density (W/cm²) ⇧	**1x**	**~2x**	**~4x**
Cu Resistance (Ω) ⇧	**1x**	**2x**	**4x**
Interconnect RC Delay (ps) ⇧	**1x**	**~2x**	**~5x**
Packaging (cents/pin) ⇘	**1x**	**0.86x**	**0.73x**
Test (nanocents/Tx) ⇨	**1x**	**1x**	**1x**

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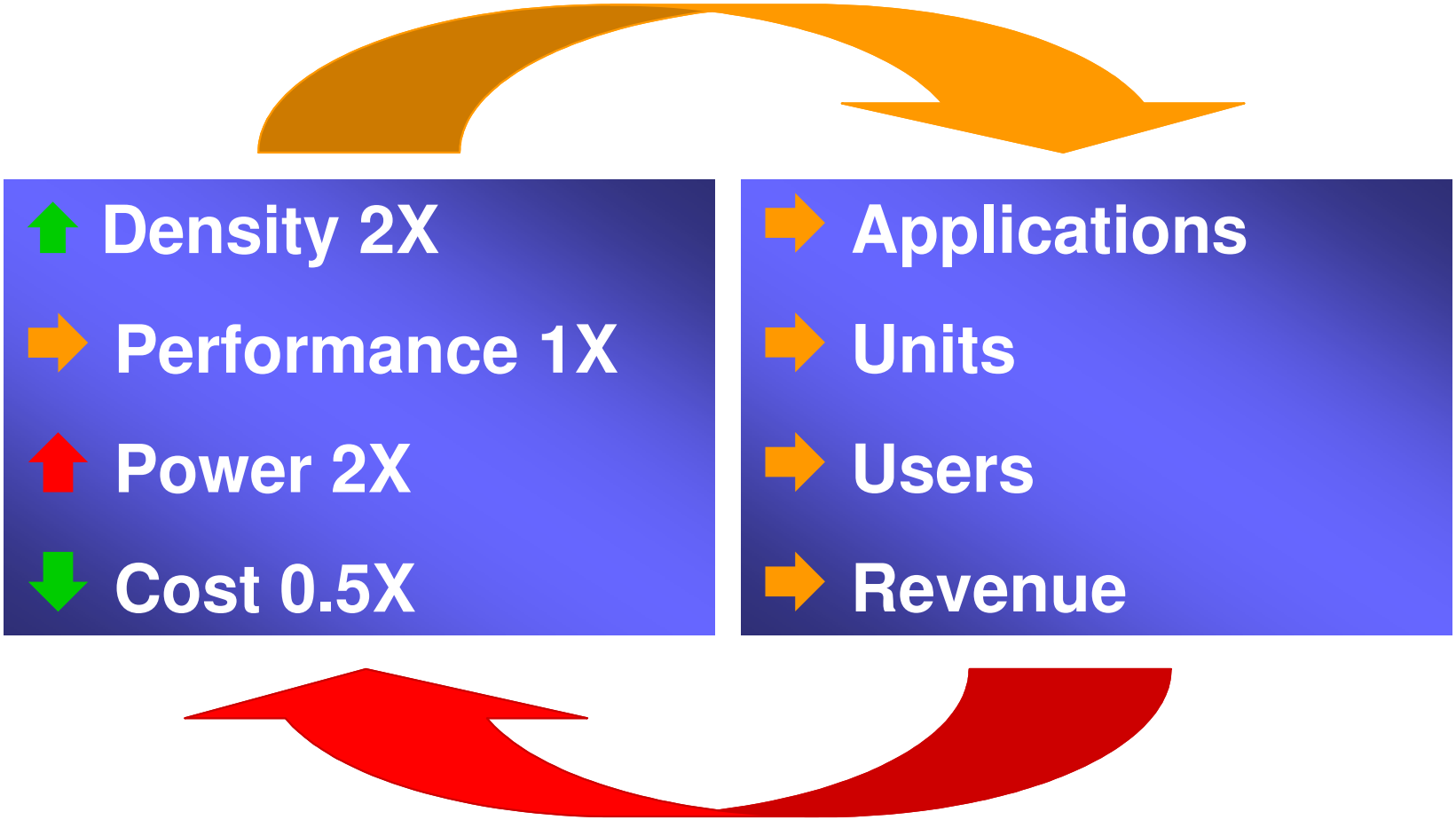
Semiconductor Industry Stalemate

Technology (CMOS) Shrinks, Doesn't Advance



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Quasi-Atomic-Level Interconnect

Main Contributor to both Timing and Dynamic Power

Source: ITRS 2005	90nm	65nm	45nm
ASIC (Gates/mm^2)	500K	1M	2M
Total Interconnect (Mx + 5 My) (m/cm^2)	1km	1.4km	2.2km
Interconnect RC Delay (My) (ps/mm)	355ps	682ps	1.8ns
τ = RC Delay (My) (um)	60um	38um	20um
Interconnect Aspect Ratio (Cu Wire/Via)	1.7 – 1.5	1.8 – 1.6	1.8 – 1.6
On-Chip Frequency (Hertz)	4.2GHz	9.3GHz	15.1GHz
Wavelength (mm)	71mm	32mm	20mm

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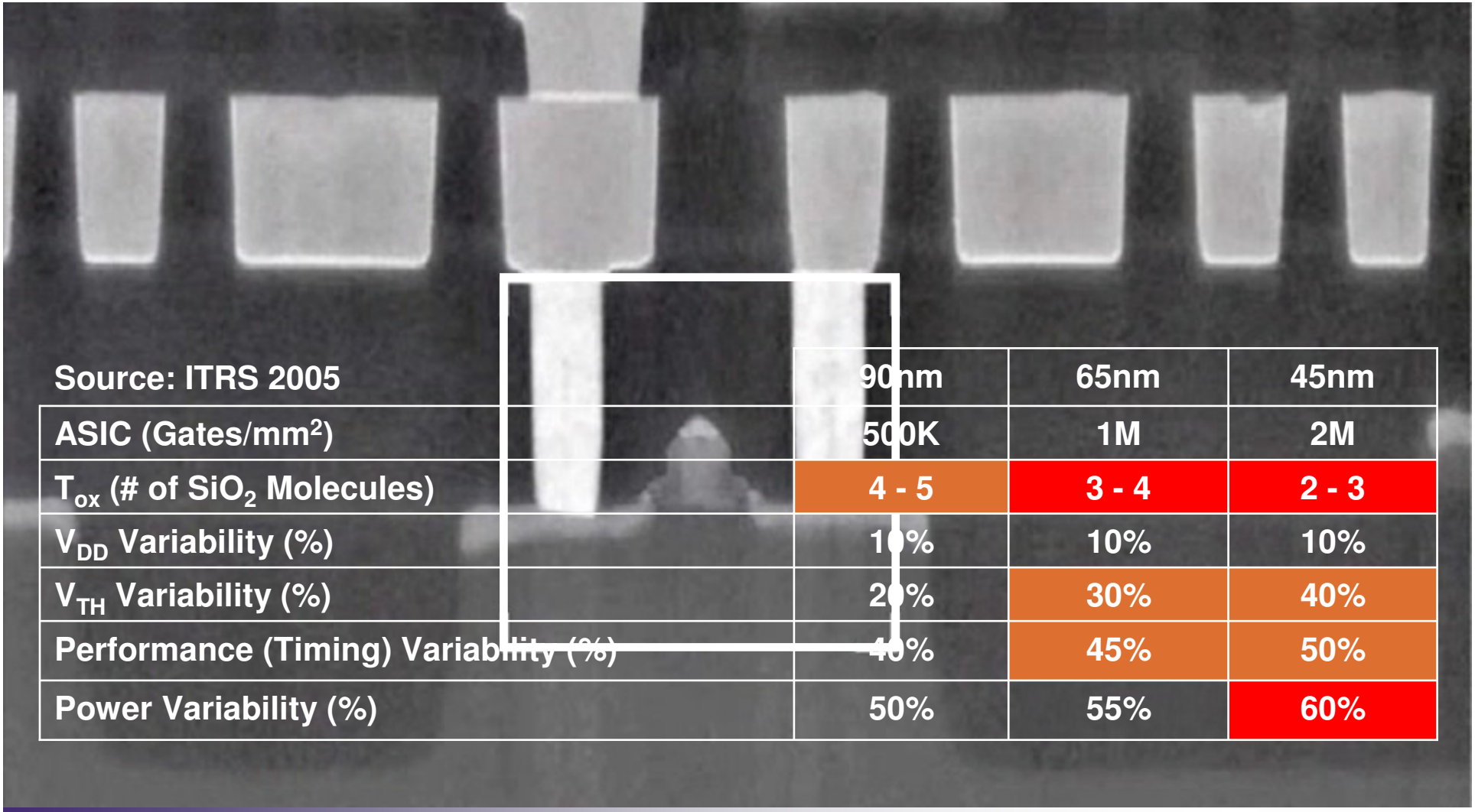
Source: R. Chau, Intel 2003

Atomic-Level Lithography

Main Contributor to both Leakage Power & Variability



Source: ITRS 2005	90nm	65nm	45nm
ASIC (Gates/mm^2)	500K	1M	2M
T_{ox} (# of SiO_2 Molecules)	4 - 5	3 - 4	2 - 3
V_{DD} Variability (%)	10%	10%	10%
V_{TH} Variability (%)	20%	30%	40%
Performance (Timing) Variability (%)	40%	45%	50%
Power Variability (%)	50%	55%	60%

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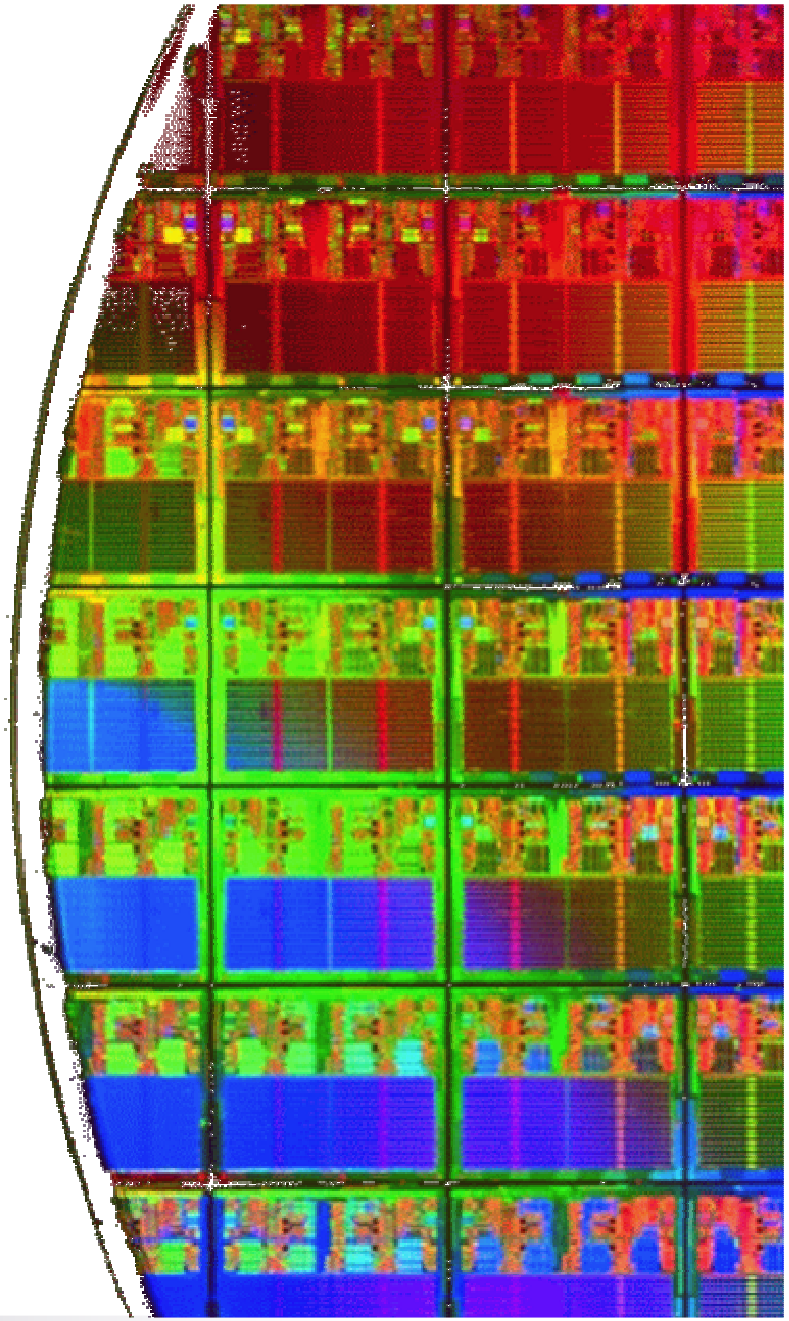
Source: R. Chau, Intel 2003

Agenda

- Rushing Or Holding?
- Where Do We Stand?
- **Design To The Rescue**



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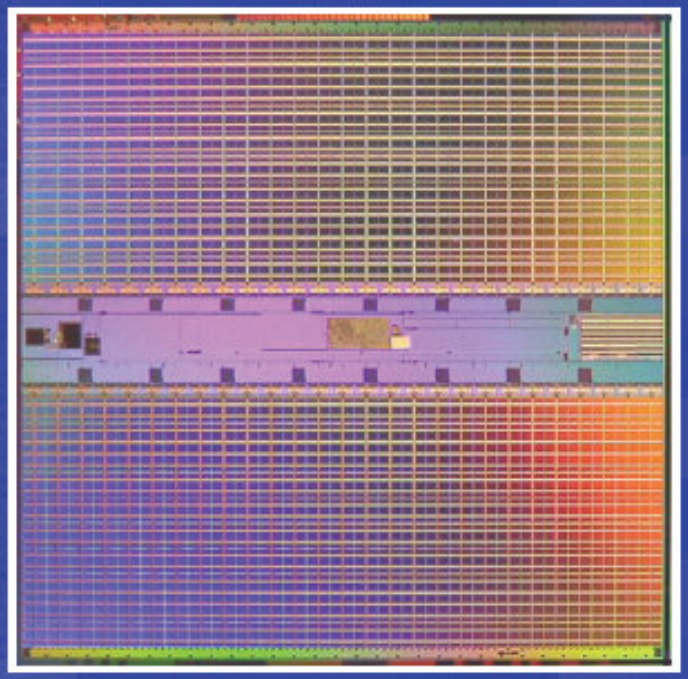
70 Mbit SRAM Chip

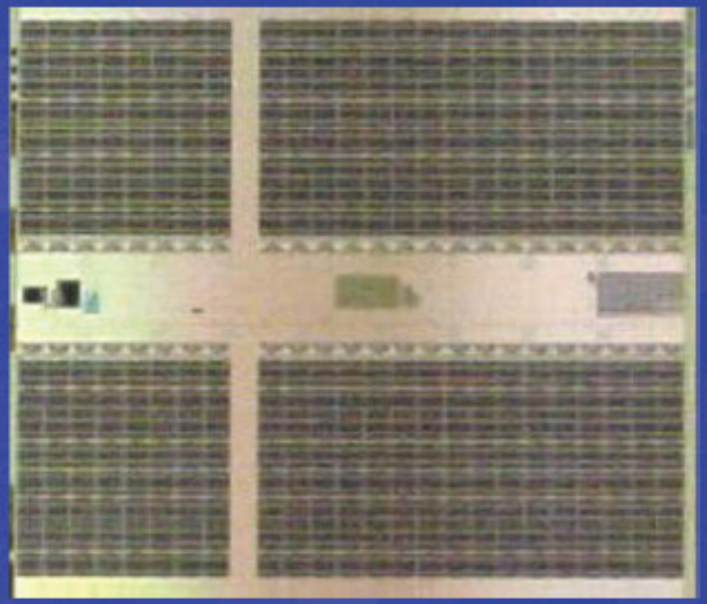
- >0.5 billion transistors
- 0.57 μm^2 cell size
- 110 mm^2 chip size
- 3.4 GHz operation
- Uses all process features needed for 65 nm CPUs



Challenging SRAM test vehicle used to demonstrate 65 nm performance, yield, and reliability

50 Mbit SRAM Chip

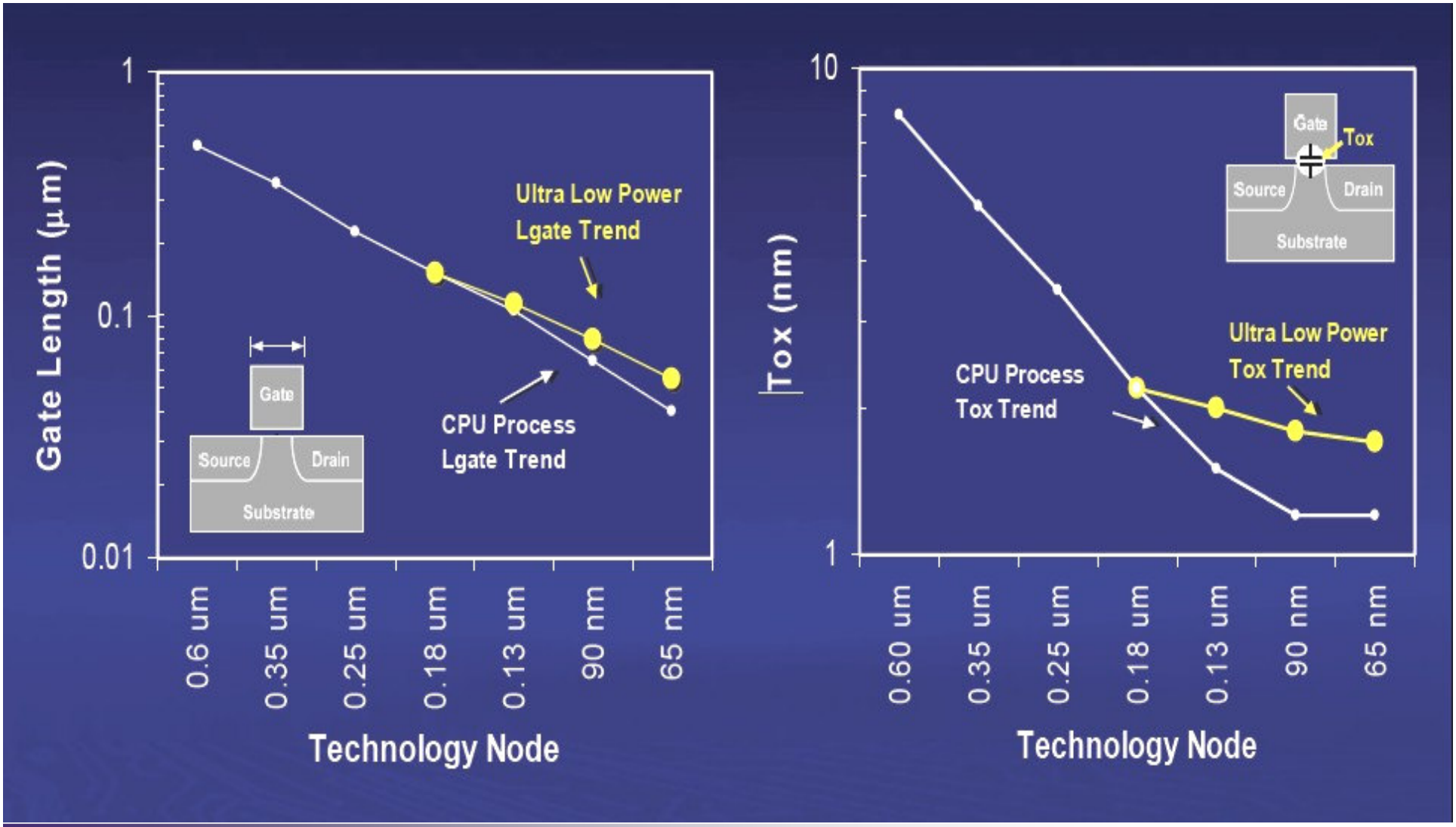
- Fully functional 50 Mbit SRAM
- >0.35 billion transistors
- 0.68 μm^2 cell size
- Ultra-low leakage power



Challenging SRAM test vehicle used to demonstrate P1265 performance, leakage power, yield, and reliability

65 Nanometers, Ultra-Low Power…

It's Actually 130nm (T_{OX}) 90nm (L_{gate}) High Performance



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Source: P. Bai, Intel, IEDM 2004; C.H. Jan, Intel, IEDM 2005

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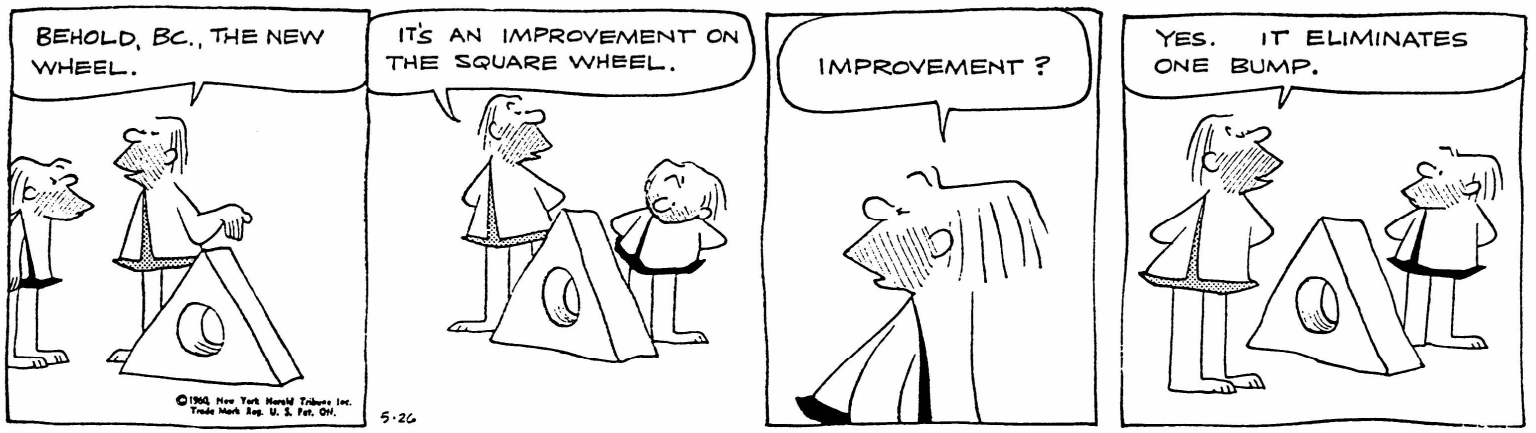
Nanometer Design

The Most Obvious Solutions Aren't Necessarily the Right Ones



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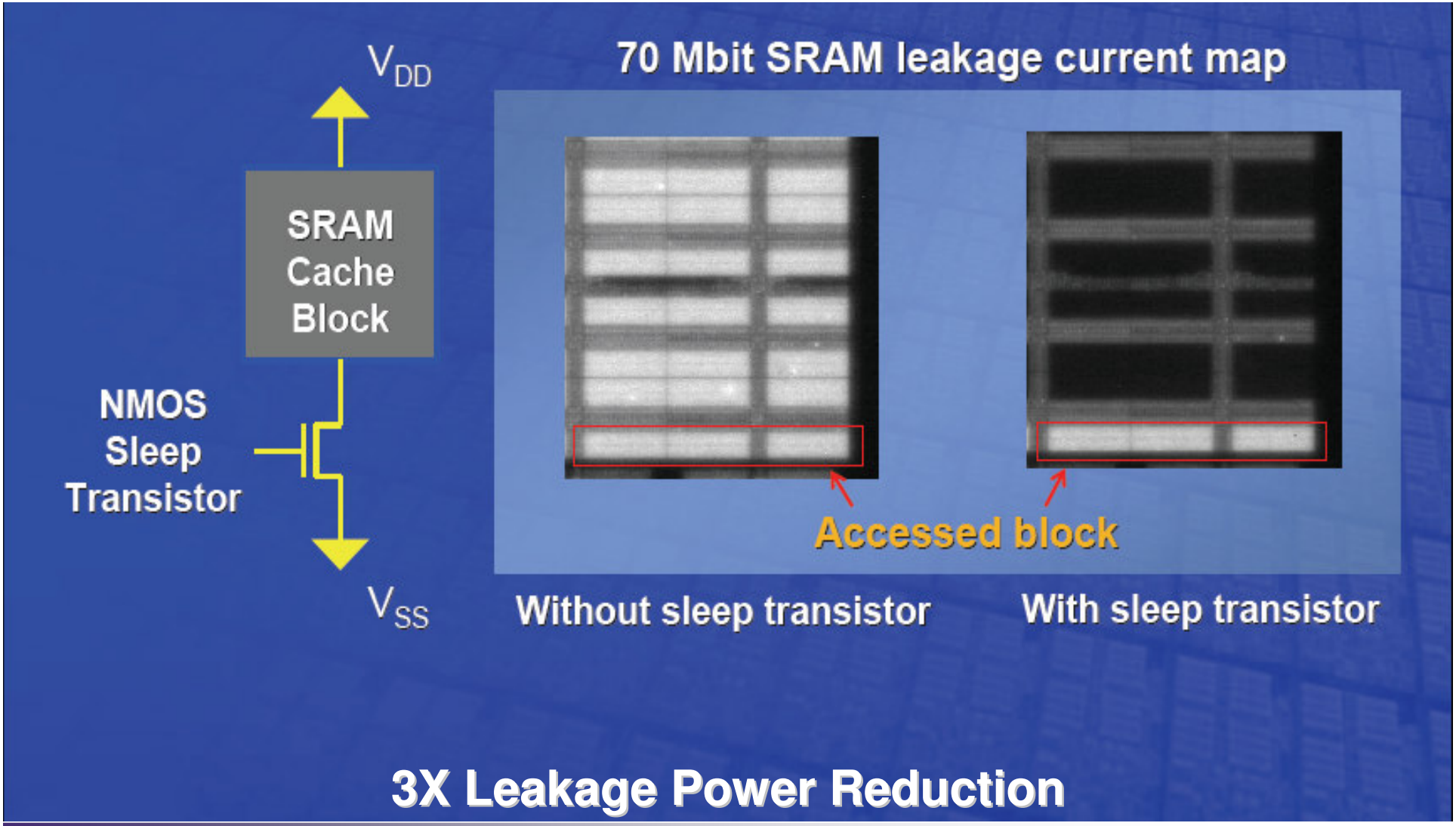
Design (& EDA!) To The Rescue

When Silicon Technology Can't Help



3X Leakage Power Reduction

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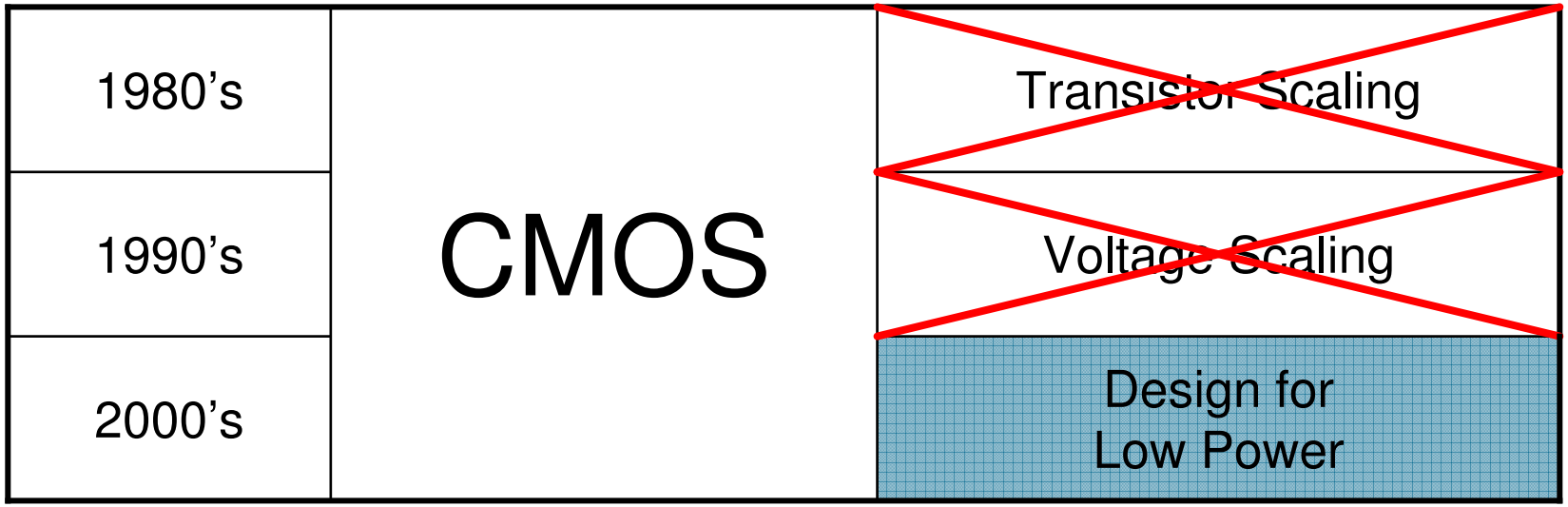
Source: S. Chou, Intel 2005

Nanometer Low Power

Transistor Size?… Power Supply?… EDA!



- **Multi-V_{DD} & Multi-V_{TH}**
- **Adaptive Voltage & Frequency Scaling**
- **Adaptive Body Bias**

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Nanometer Design For Low Power

All the Right Ingredients

	Constant Throughput/Latency		Variable Throughput/Latency
	Design Time	Non-Active Modules	Run Time
Dynamic & Short Circuit	Logic Re-Structuring, Logic Sizing, Reduced V_{DD}, Multi-V_{DD} **2.5X**	Clock Gating **2X**	Dynamic or Adaptive Frequency & Voltage Scaling **2.5X**
Leakage	Stack Effect, Multi-V_{TH} **2X-10X**	Sleep Transistors, Multi-V_{DD}, Variable-V_{TH} **10X-1000X**	Variable-V_{TH} **2X-10X**

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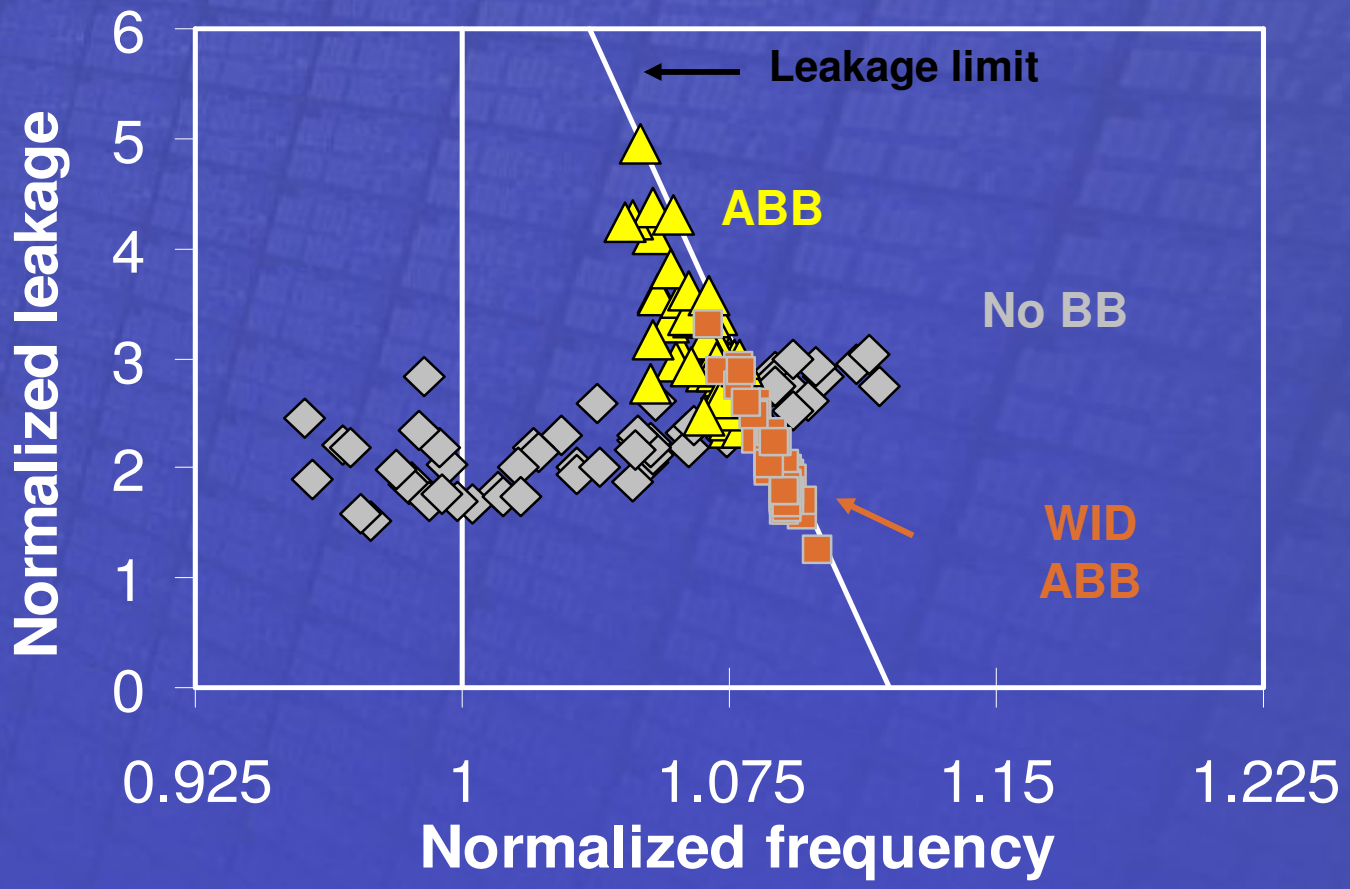
Source: J. Rabaey, UCB 2005

Design For Low Power Helps!

Variable V_{TH} (Adaptive Body Bias)



100% Performance Yield, 97% Highest Frequency Bin

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Source: V. De, Intel 2005

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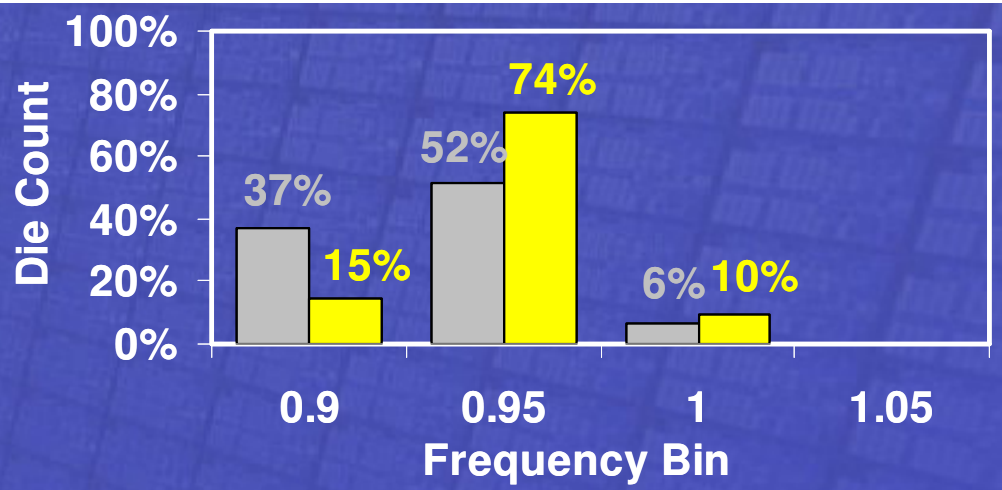
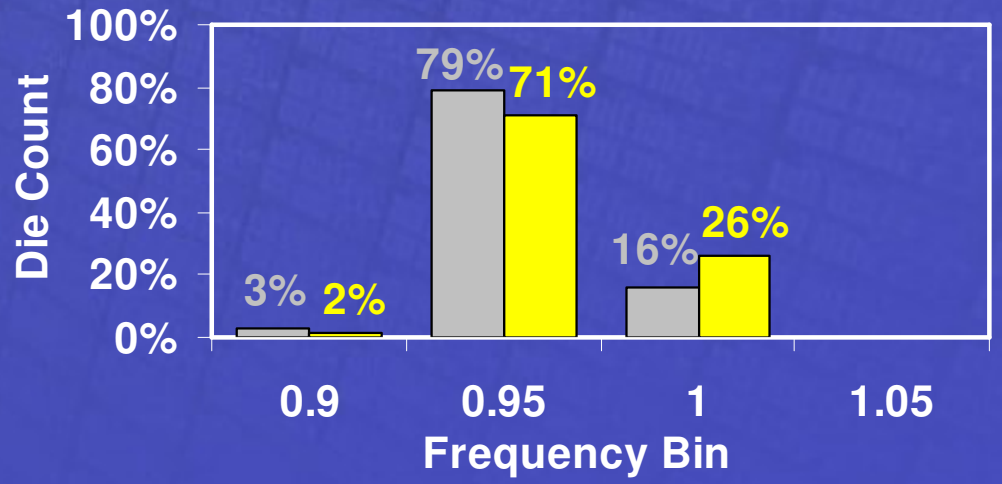
Design For Low Power Helps!

Adaptive Voltage Scaling & ABB





2X Performance Variability Reduction

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Source: V. De, Intel 2005

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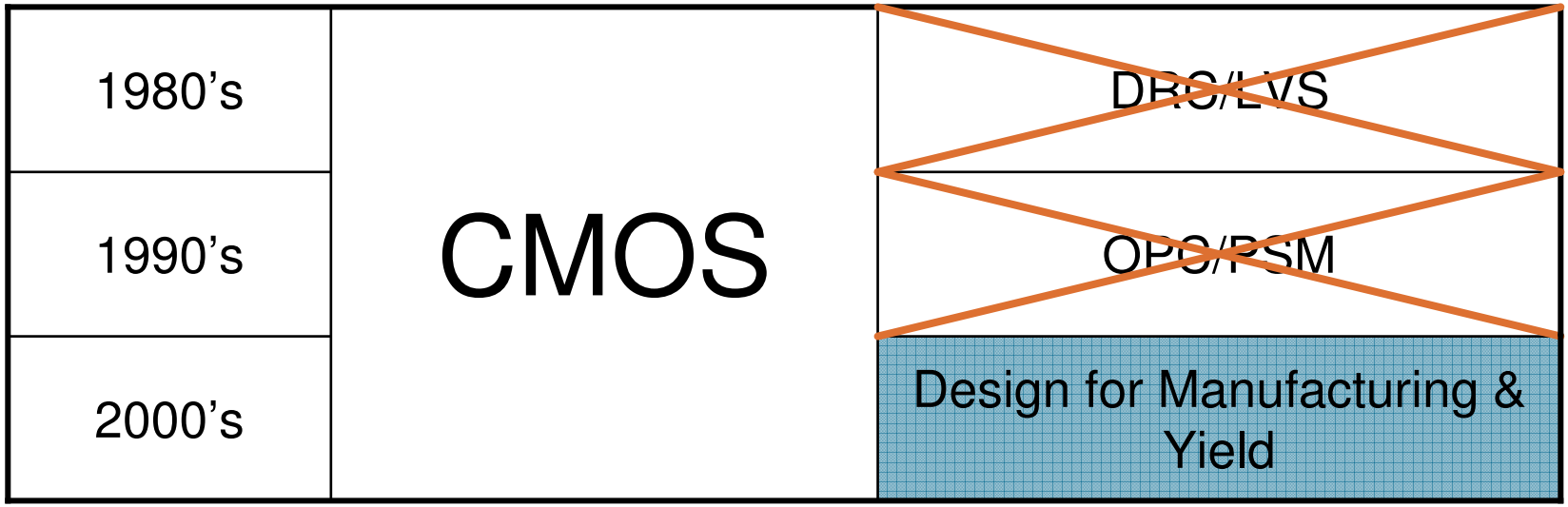
Nanometer Yield (Lithography)

Correctness?… Accuracy?… EDA!



- **Timing-Driven Wires Spreading & Vias Optimization**
- **Timing-Driven Metal Fill**
- **Lithography Compliant Routing**

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Nanometer Yield (Lithography)

All the Right Ingredients

	Functional	Parametric	
	Manufacturing Time		Run Time
Random	CAA Wires Spreading	CAA Wires Spreading	
Systematic	Diodes Insertion Vias Optimization OPC-Aware Routing LCC/OPC/PSM	Vias Optimization Metal Fill Gaussian Slack	PNA/PNS Reliability Analysis

Higher Yield

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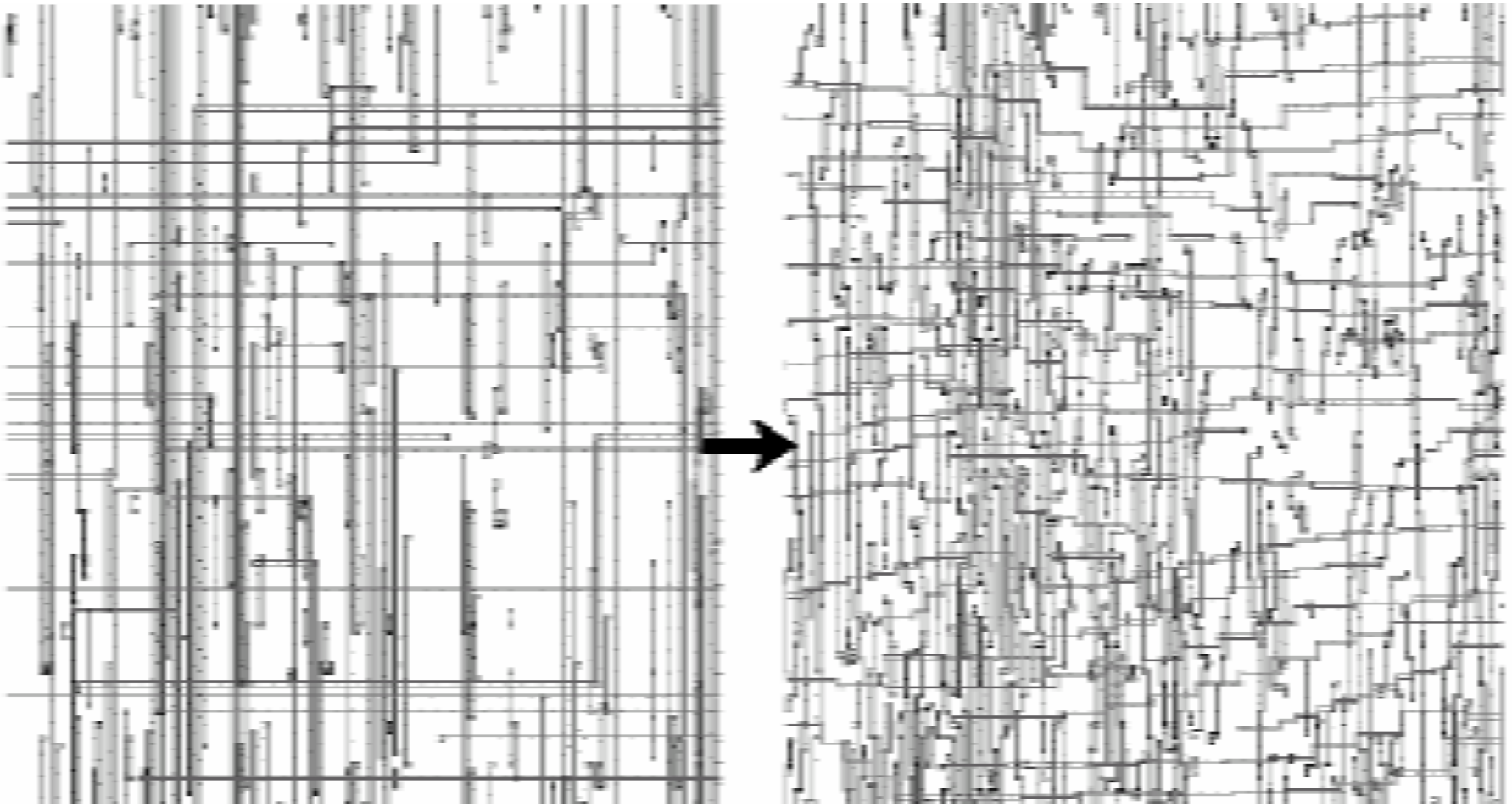
Design For Manufacturing/Yield Helps!

Timing Driven Wires Spreading



4% Better Yield: Uniformity Reduces Variability

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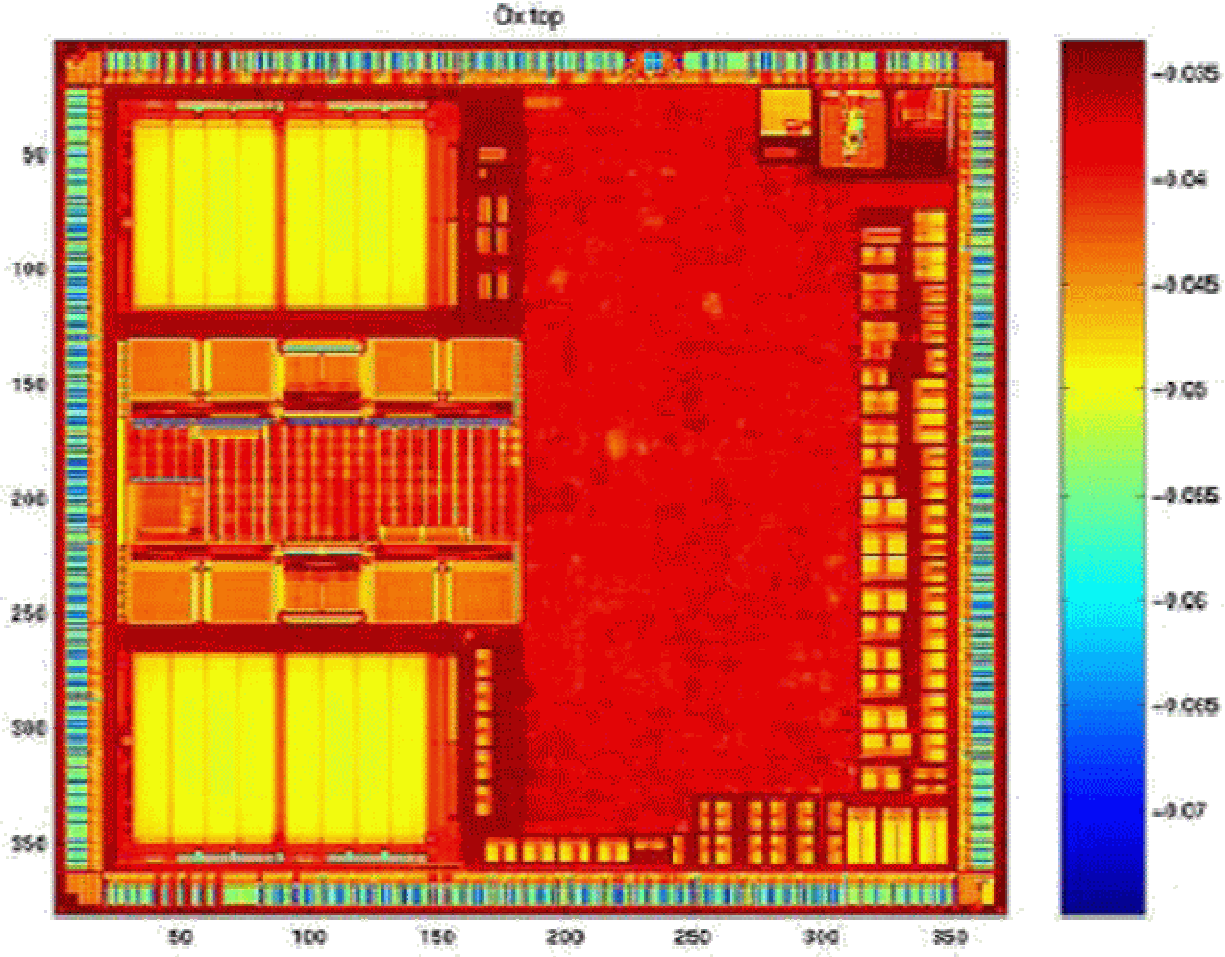
Source: European IDM 2002

Design For Manufacturing/Yield Helps!

Timing Driven Metal Fill



Cu Dishing < 40Å: Uniformity Reduces Variability

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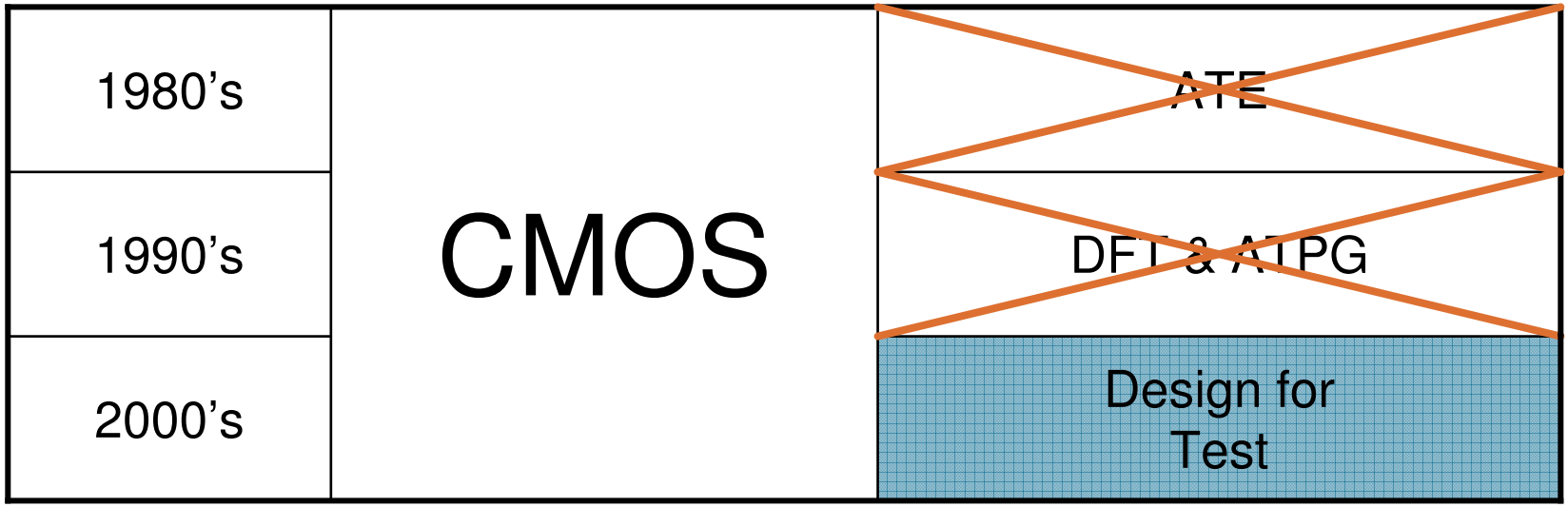
Source: L. Pileggi, CMU 2005

SYNOPSYS®
Predictable Success

Nanometer Yield (Test)

Correctness?… Completeness?… EDA!



- **Test Compression**
- **At-Speed Test**
- **Yield Diagnostic**

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Nanometer Yield (Test)

All the Right Ingredients

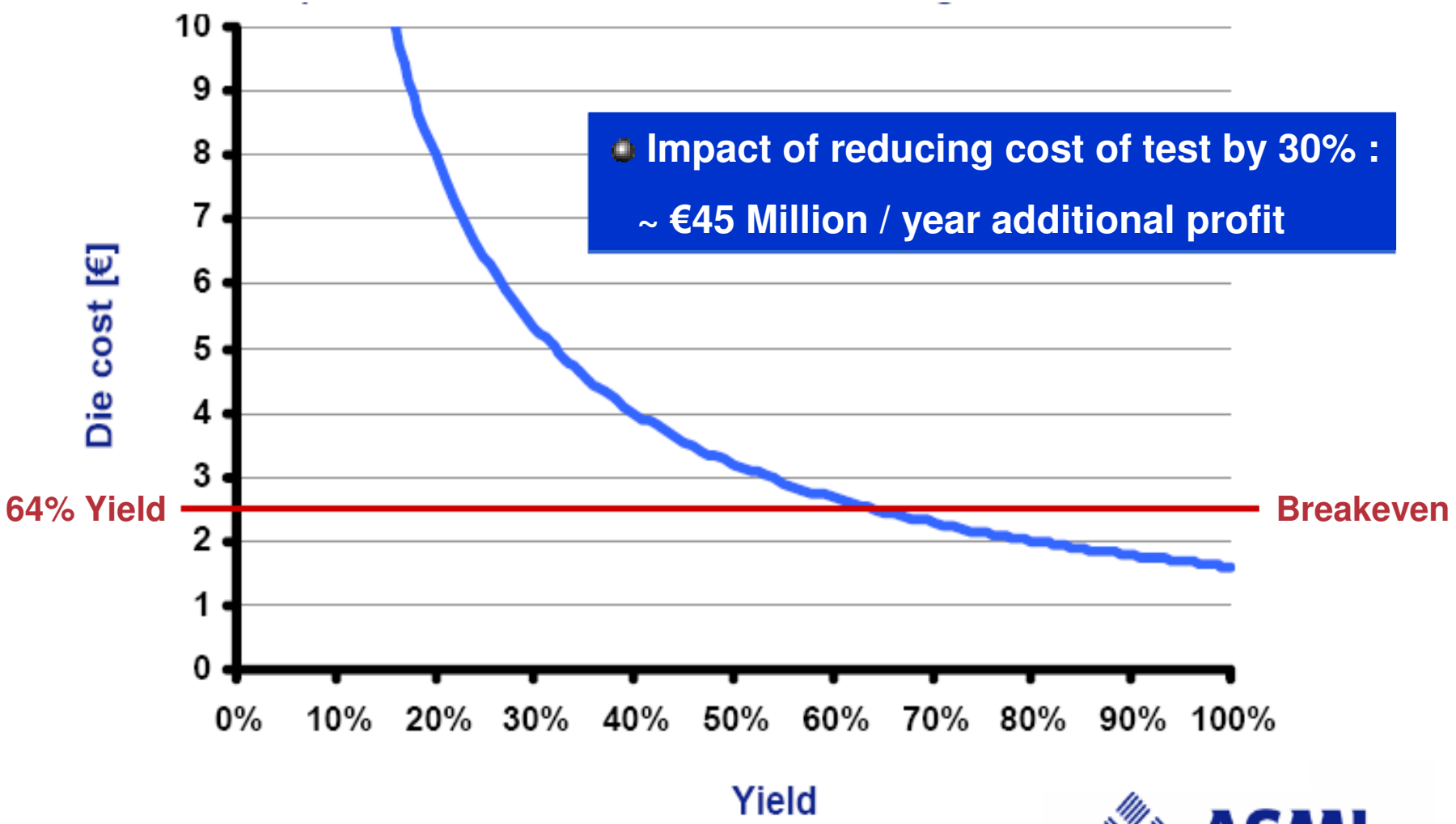
	Catastrophic	Parametric
	Composite Current Source (CCS) Models Delay & Transition Faults Models	
Static	Stuck-At Test I_{DDQ}, Burn-In	Path/Transition Delay Test, At-Speed Test I_{DDQ}, Burn-In VLV Test
Dynamic	α Particles	V_{DD}, Temperature Yield Analysis Yield Diagnostics

Source: R. Puri, IBM 2005

SYNOPSYS®
Predictable Success

Design For Test Helps!

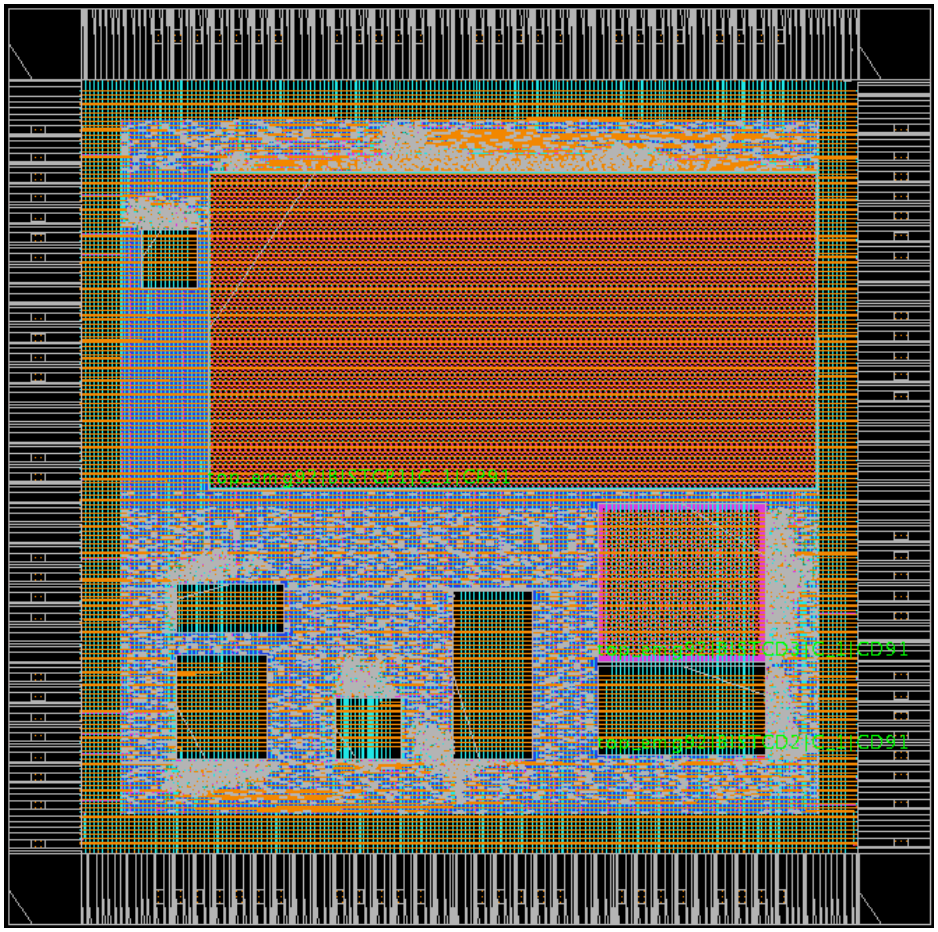
25k Wafer per Month, 625 Gross per wafer, €1000 Processed Wafer, €2.5 Package & Test, €5 ASP



ASML

Design For Test Helps!

Adaptive Scan Compression



From 50M To 4M Vectors, From 15¢ To 3¢ Per Unit

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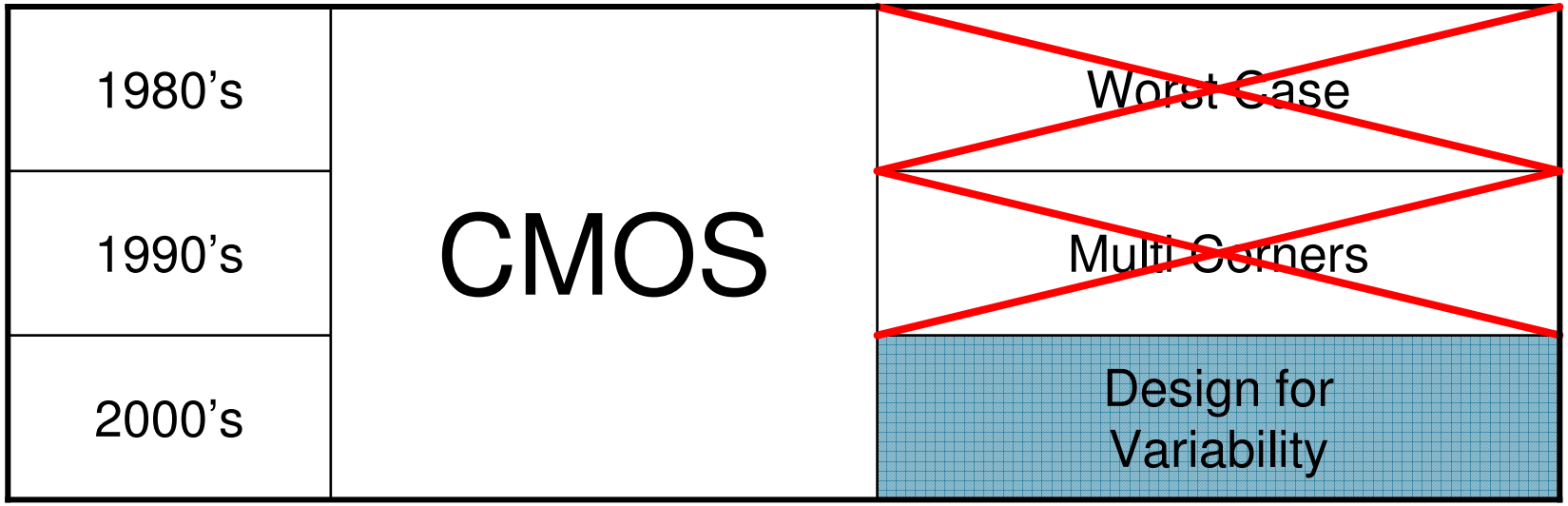
Source: European IDM, Inkjet Printer, 130nm

Nanometer Uncertainty & Variability

Margins?… More Margins?… EDA!



- **Current Source Models**
- **Statistical Extraction & Timing Analysis**

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Nanometer Uncertainty & Variability

All the Right Ingredients

	Process	Design
	Composite Current Source (CCS) Models	
Static Variations	LCC, OPC/PSM Wires Spreading, Vias Optimization & Metal Fill	CCS, Gaussian Slack Statistical Extraction & STA
Dynamic Variations	Adaptive Body Bias Wires Spreading, Vias Optimization	Adaptive Body Bias & Voltage Scaling SI, Power & Thermal Analysis

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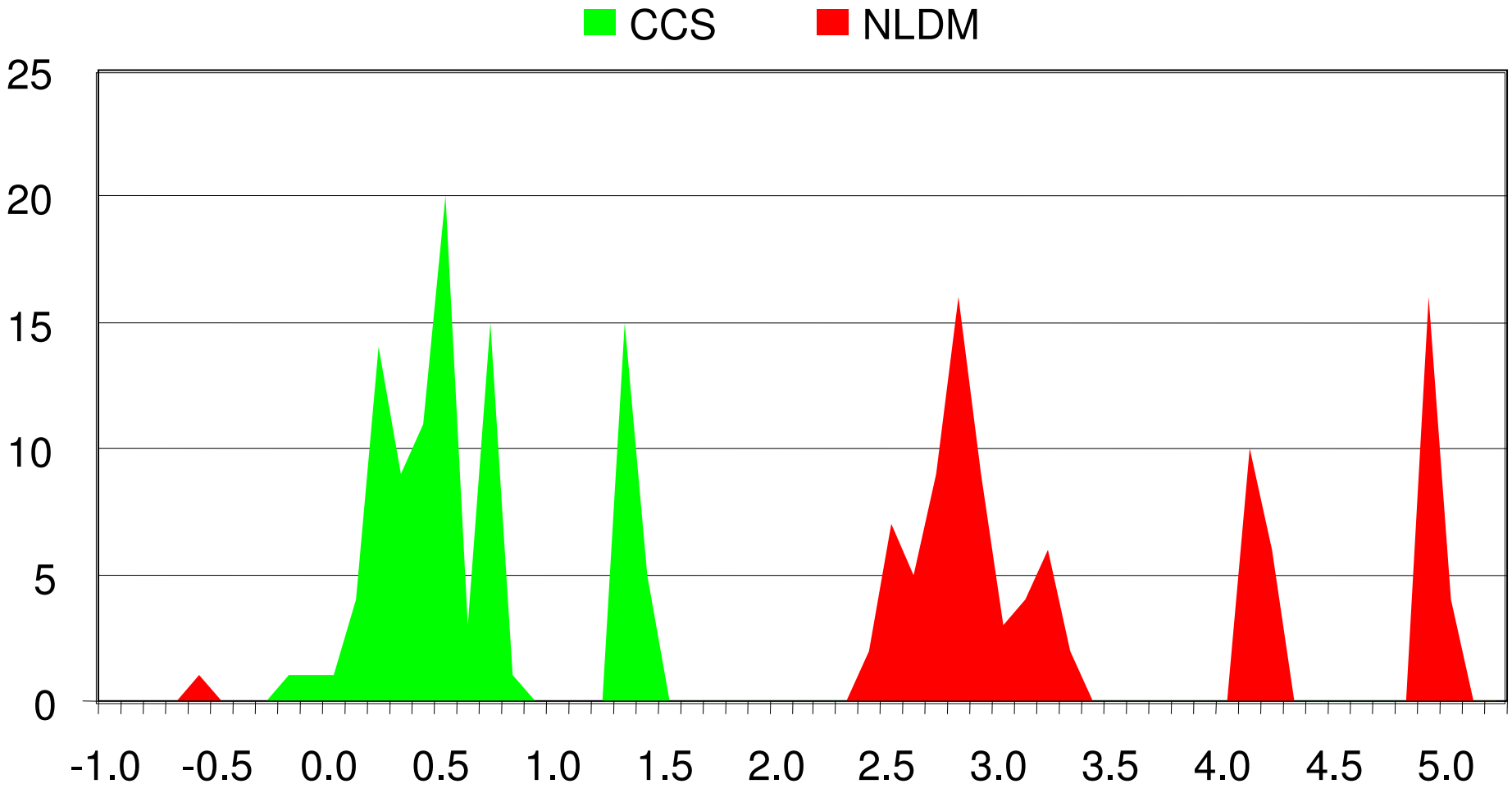
Source: J. Rabaey, UCB 2005; S. Borkar, Intel 2004; S. Nassif, IBM 2000

Design For Variability Helps!

Composite Current Source (CCS) Models



CCS Is 2.5X More Accurate Than NLDM

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Source: U.S. IDM 2005

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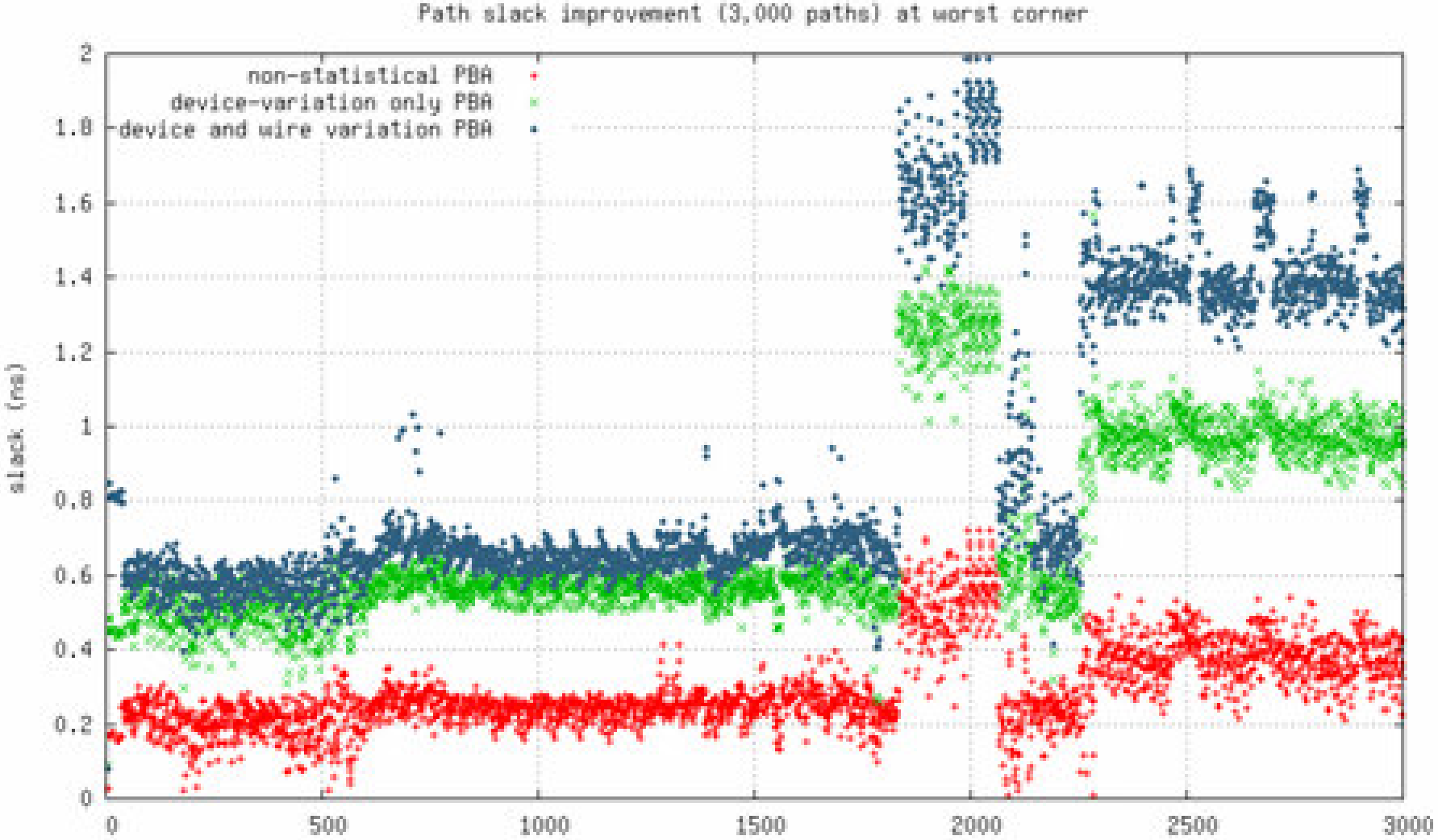
Design For Variability Helps!

Statistical Extraction & STA



⬆Accuracy ⬇Pessimism ➡10% Higher Frequency

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Source: U.S. Fabless, Wireless Application, 65nm

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