Low Power Design Challenge in Wireless with Deep Submicron Geometries

Milind Padhye
Freescale Semiconductor Inc
6501 W. William Cannon Dr.
Austin, Tx, USA
+1 512 895 7420
Milind.Padhye@Freescale.Com

Noah Bamford
Freescale Semiconductor Inc
6501 W. William Cannon Dr
Austin, Tx, USA
+1 512 895 3975
Noah.Bamford@Freescale.Com

Saji George
Freescale Semiconductor Inc.
6501 W. William Cannon Dr.
Austin, Tx, USA.
+1 512 895 6508
Saji.George@Freescale.Com

ABSTRACT
Standby time, Talk time and multimedia run time in cell phone are market performance parameters and define the quality of service in consumer mind. The battery life in a typical phone depends on the static power consumed by the chips when in sleep mode and effective active power consumed during the user specific activity. The standby power is determined by leakage in the chip and device leakage problem has increased significantly with reduction of feature size. This paper presents a variety of techniques used to minimize the power consumption and important challenges in wireless SoC for power oriented design.

Categories and Subject Descriptors
B.5.2 [**Hardware**]: Register-Transfer-Level Implementation - *Design Aids -Simulation*; B.8.2 [**Hardware**]: Performance and Reliability *Performance Analysis and Design Aids*; C.4 [**Computer Systems Organization**]: Performance of Systems - *Modeling techniques*

General Terms
Design, Performance, Theory, Verification.

Keywords
Power Estimation, Design, Design Methodologies, Power models, SRPG, S&RPG, Register-Transfer Level, Simulation, Power aware verification, Low Power Representation, DVFS

1. INTRODUCTION
In wireless market, the source of revenue is off for the carriers if the cell phone is turned off. As cell phones are battery operated devices, this puts a large emphasis on power performance efficiency in all modes. Standby time of the phone is determined by the leakage of the chips in the platforms and power consumed during the wake up sequence. The phone wakes up every half second and connects to the base station to check the presence of any call. In absence of a call, the phone enters the sleep mode. This continuous cycle of sleep and wakeup requires careful design of components in order to minimize the associated power consumption in this mode. As there is entry and exit cost associated with each wakeup and sleep cycle, higher rate of wakeup and sleep cycles would lead to reduced standby time in the absence of design changes. This sequence and its frequency are very specific to the associated wireless protocol and hence the protocol also determines the power consumption in the wireless device. Multiple low power design techniques are created to meet the battery life requirements for specific wireless protocols.

Performance and components required for a voice call may be different when compared to other active modes such as multimedia playback operation. Increased power performance efficiency can be achieved by new design techniques like DVFS.

This paper focuses on the techniques and approach used to minimize leakage and active power in baseband processor for the cell phone.

2. Low Power Design Techniques
During the sleep mode inside the phone, majority of the logic in baseband processor is in idle state. A small portion of logic is required to manage the real time and associated machine. A low frequency clock (~ 32 KHz) is used for this purpose. All modules and subcomponents that do not use the low frequency clock during sleep mode are the best targets for power management inside the chip. A variety of techniques can be used to minimize the leakage on such modules and subcomponents.

2.1 State Retention Power Gating
State Retention Power Gating (referred as SRPG hereafter) is an aggressive approach to arrest the leakage in sleep modes. The technique provides a good combination of performance when active and reduced leakage in idle mode.

In any given system, the state of the system is typically saved in flipflops and memory elements. The combinational logic present in between the flipflops provides a means for state propagation. In idle modes, the system clock is silent. The flip flops save the state but the entire combinatorial logic can consume significant portion of leakage power. SRPG provides an approach to turn off this leakage power in all non-active portions of the design.

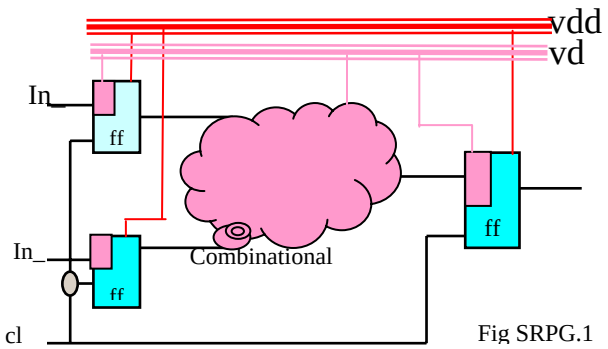


Fig SRPG.1

In reference to figure SRPG.1, VDDC is a continuous power supply and VDD is interruptible power supply. Both supplies can be derived from same source but VDD is operated thru power switches and may be driven from same source. These power switches are on/off devices and fully control the VDD grid based on sleep mode of the chip. With this technique, very small part of the design is now connected to always on supply and hence a significant leakage can be saved. Certainly, the effective leakage saving is dependent on the number of flops and its ratio to combinatorial logic.

2.2 Save and Restore Power Gating

This is another popular technique used for leakage saving. Conceptually, it is very close to SRPG, but differs significantly in implementation style. The state of the system is moved to a memory array instead of saving it locally inside the flop. Before entering the low power sleep mode, the state is captured and converted to a memory array image. After, moving the state to memory array, the full system or part of the system is powered off. The memory array saving the state is kept always alive thru the entire power off duration. When exiting the low power mode, the system or part of the system is powered up with a reset condition and previous state is downloaded from the memory.

A significant power cost may be associated with state movement from system or part of the system back and forth to the memory. In certain cases, for smaller duration, it may not be an effective way to reduce the power consumption.

This technique also impacts the overall wakeup latency of the system or part of the system. It takes much longer to save and restore from memory array as compared to SRPG where each register is restored locally.

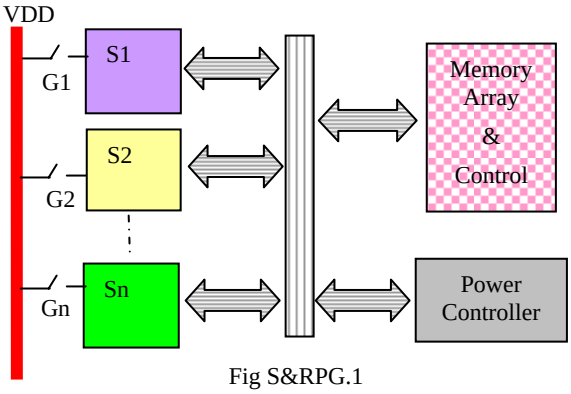


Fig S&RPG.1

In reference to fig S&RPG.1, S1,S2…Sn are subcomponents in the system which can share the same power controller and memory array for saving during power down. The controller is also responsible for turning off the power gates G1, G2.. Gn once the appropriate state transfer is complete. This design technique can increase overall complexity of power control significantly as compared to SRPG. The latency of wakeup and sleep is also dependent on data bus width, controller operating frequency and overall thruput of memory controller.

2.3 Biasing and Vt adjustments

Biasing and Vt adjustments techniques have been used for long time to control the power and performance of the design. HiVt based design when mixed with Low Vt devices in critical timing path provides a path for power performance optimization. In cases, where the leakage can not be mitigated using mixed Vt design, power gating based design are the better approach for leakage reduction.

2.4 Dynamic Voltage Frequency Scaling

Active power during the wakeup and connection to base station is also an important parameter for standby time definition of a cell phone. Talk time and multimedia run times are primarily defined by the active power consumption by the components in cellular platform. Operating voltage is the primary parameter to affect the power. For lower operating frequency, the voltage can be reduced and this can lead to significant active power savings.

Power is proportional to square of the operating voltage.

$P= C*V^2*F$

For example, if an application can meet the performance need at half the normal frequency and operating voltage can be reduced by 10% to meet the timings, approximately 19% power savings can be achieved. This enable the approach to dynamically adjust the voltage based on performance need of the system. Thus, the operating voltage range of a high performance subsystem needs to be separated from the operating range of low performance subsystem.

In summary, the low power design focuses on three major points.

1. Turn off the part of the system that is not in use.
2. Reduce operating voltage for low performance region.
3. Increase the voltage for high performance region in high performance needs.

2.5 Power Control Diamond

The drive to save power has led to creation of multi-voltage domains in wireless designs. Management of these multiple power domains is done thru a specialized power controller. This controller is fully responsible for linking up the state machine of the chip to power-up, power down and dynamic adjustment of the voltages.

The power control diamond involves interaction exchange between the core, power managed subsystem, clock controller and power controller. Functional synchronizations must be achieved across all these components when power-up/down decisions are made. Any loss of synchronization can lead to system corruption and unstable response.

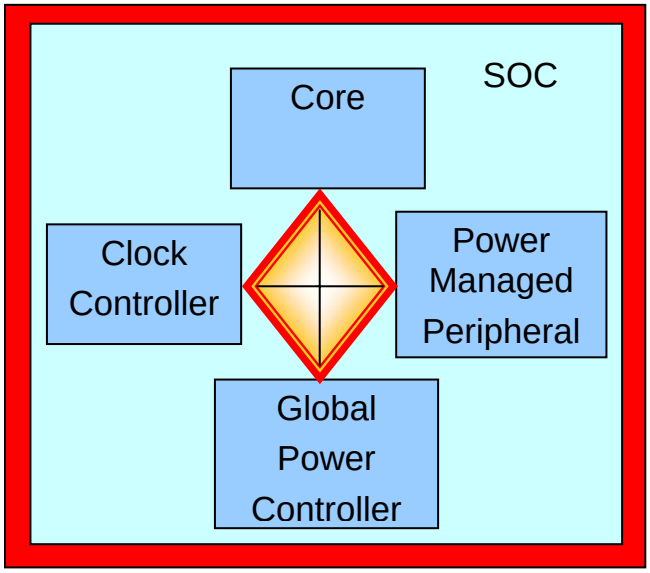


Fig. Power_Control_Diamond.1

The sequence involved with power control diamond may vary based on the chip architecture and specific modes.

3. Major Challenges

All low power techniques have brought in the complexity of design representation, implementation and complete verification. Power estimation in various situations is also equally complex as power control parameters have been made as variable and brought into design equations.

3.1 Low Power Design Representation

Multi-voltage design style affects all parts of the design flow. A consistent representation of the power partition and constraint across various tools and flow is crucial to design success. Common design representation of power related data significantly impacts the design productivity and reduces the scope of manual errors in interpretations.

3.2 Low Power Design Implementation

Complete RTL2GDS flow is significantly influenced and altered due to multi-voltage partitions and low power design techniques. Power partition plays a significant role in floorplan and drives the need for good power integrity for the grids at a very early stage of design. The power grid includes multiple switching devices and IR considerations must be addressed at very early stage of design.

Change of voltage impacts timings and performance inside the design. Clock insertion delay estimates are different based on the operating modes in the chip and hence timing optimization and analysis across various modes and corners is critical. The synthesis process is more iterative and can lead to instability if power and timing constraints are not properly correlated.

Placement and clock tree balancing has become much more complex due to SRPG and multi voltage designs. In cases, where the synchronous clock crosses the voltage boundaries, special attention is needed for clock balancing.

Special attention is needed when stitching the scan chains and generating test patterns for multi-voltage design. Scan connection of power controller is very crucial as it can trigger unspecified power up or down during scan test.

In place optimization and router tools should be aware of power partitions while optimizing timings and inserting the buffers.

Physical verification tools also need full understanding of power partitions for correctly verifying the power connectivity in layouts.

3.3 Low Power Design Verification

Combination of various low power techniques has brought multiple challenges for the verification of wireless design. Conventional simulation had an assumption that power is always alive. New design techniques have broken the boundaries of this assumption and hence the power aware verification is crucial in early stages of RTL definition. Presence and absence of power was never modeled in conventional verilog and hence modeling of this feature in itself is an important step in verifying low power design techniques. In cases explained in fig SRPG.1, representation of powered off combinational logic and state retention behavior of flipflops at RTL stage is very important. In a typical design, there could be a combination of retention and non retention flipflops. Power-up and power down of such design requires accurate modeling of such features.

Power domains are isolated using special isolation cells. When signals are crossing the voltage boundary, power off condition in one domain can induce corruption in receiving domain. Isolation states of such power domains must be fully validated before entering the design implementation phase. Incorrect isolation states can trigger the state machines in sleep mode and create functional problems.

Another challenge is upgrading existing PLIs to make them power aware. Existing conventional PLI do not understand the power down condition. The updates are needed to bring in power awareness in these routines.

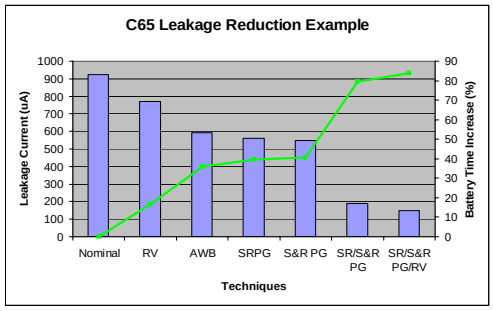
The control diamond responsible for power modes has to obey certain power up and power down sequences. The control diamond should be fully verified with correct power state models.

3.4 Design Power Estimation

Power partition decisions are primarily driven from power estimates. This is an iterative loop in early phase of design. Consistent and accurate power estimates at early stage of design are very crucial to freeze the power partitions for further implementation. Change of power partition is extremely difficult decision when the design has entered the implementation stage. Consistency and accuracy of power estimate is of utmost importance to reach to correct power partition decision and then constantly checking the estimates as the design progresses thru various stages.

4. Case Study and Results

A case study was performed on an early version of a baseband processor in CMOS65 technology node. The histogram represents effectiveness of low power design techniques.



Combination of various low power design techniques was used to achieve minimum standby power. RV stands for reduced voltage and AWB stands for Active Well Biasing.

5. Authors

Milind Padhye is Low Power Design Manager at Freescale Semiconductor, Wireless design organization. He has been working in the field of low power design for last six years and has multiple patents on power reduction techniques and integration. He has lead multiple chips for low power architecture and design. Milind holds MS-EE from IIT Kharagpur, India in 1990.

Noah Bamford has worked for 8 years as a verification engineer in the wireless group of Freescale Semiconductors. He received his BS in ECE from Carnegie Mellon University.

Saji George has led the integration of numerous wireless and transportation SoC products at Freescale Semiconductors. He received his MS in EE from UTEP

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