Wireless
Low Power Design and Verification Challenges

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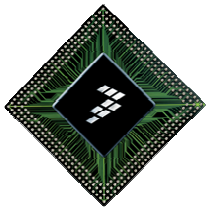
Milind Padhye, Noah Bamford, Saji George
Freescale Semiconductor Inc.



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Wireless and Handheld Devices

- ►Standby & Talk time - Benchmark parameters in cell phone industry.
- ►Music playback time - Benchmark for MP3 capable phones.
- ►Frequent battery charging - Major negative in consumer mind.
- ►Increase performance with large battery – Increased Cost
- ►Increased Heat in phone – Increased liability and TCO.

❖Power Performance ratio must be very good to win consumer mind.

End Consumers are becoming power aware and can make intelligent decisions and smart choices on power.

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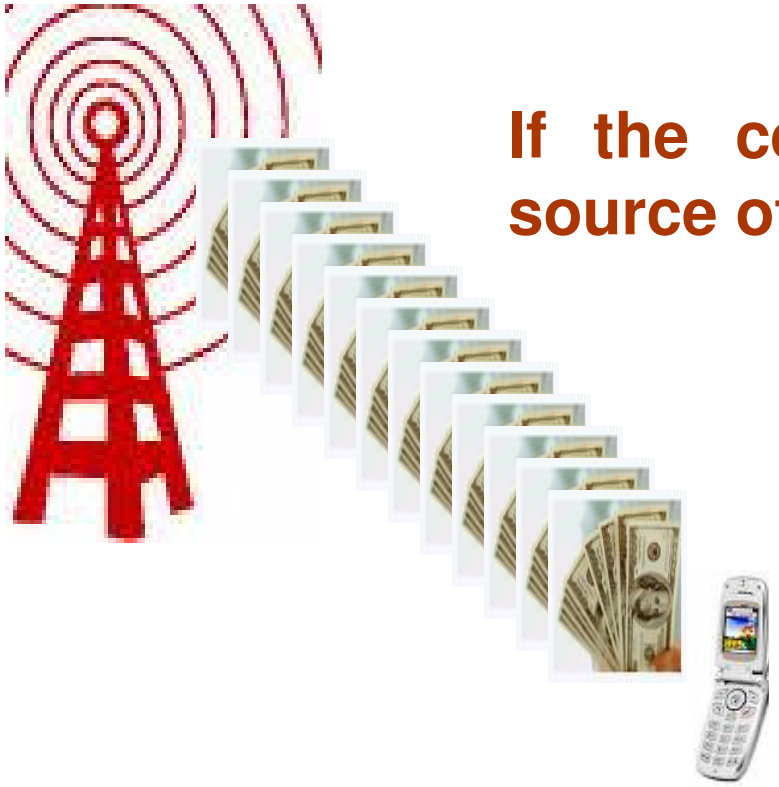
Wireless Carriers

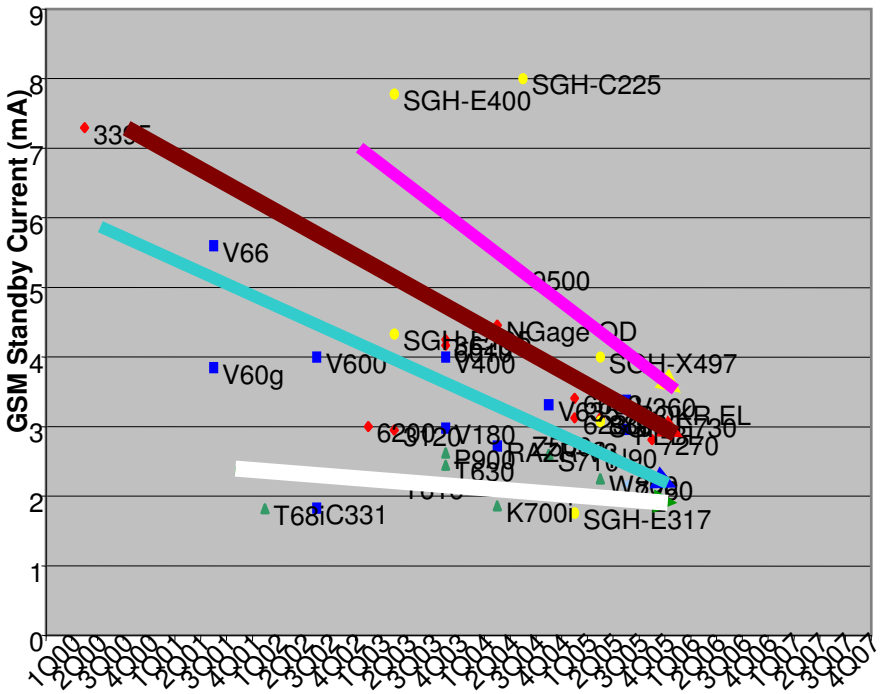


If the cell phone is powered off, The source of revenue is off for carrier.

Those Electromagnetic waves are turned Dollar-Magnetic …. only if cell phone is alive!

Low Power Design is business critical need and has a direct impact to carrier revenue.

Phone Standby Current



GSM Standyby Current Over last 4 years

Standby mode of phone is a continuous repetitive cycle of sleep and wake.

Cell phone wakes up, connects to base station and in absence of call returns to sleep.

During sleep, minimum activity exists inside phone and hence leakage is major factor for power.

Minimize leakage in sleep mode.

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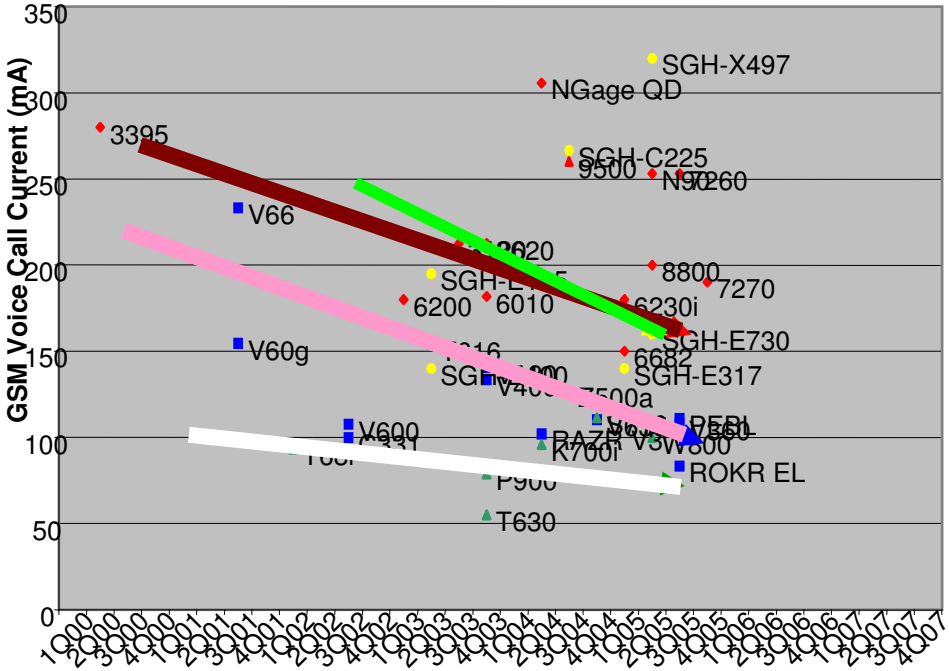
Phone Application Current



GSM Talk Current in last 4 years

Multiple applications are targeted on each phone.

Each application has different performance needs

Application run time is limited due to battery limits.

Power Performance ratio must be optimized for target applications

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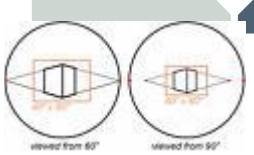
It's about Energy

Goal: Extend Phone Battery Life

- Battery life is proportional to energy consumed
- Energy is power consumed over time
- Wireless designers must manage energy consumption.

To extend battery life, designers must minimize active and leakage power.

Power Problem



Software Definitions	Dynamic system monitoring and intelligent control of energy saving
Platform Definitions	Power Trees, Connectivity components & consistent platform power modes
Architectural Definitions	Heterogeneous processing resource optimization: MCU, DSP, accelerators, functional processing units
Design Definitions	Hardware support for power gating, low-power idle modes, SRPG, AWB, DVFS, DPTC, Biasing techniques
PROCESS node Definitions	Transistor design, Vt Optimization, memory bitcell design. Special circuits, libraries, custom and analog blocks

System Level

Design Level

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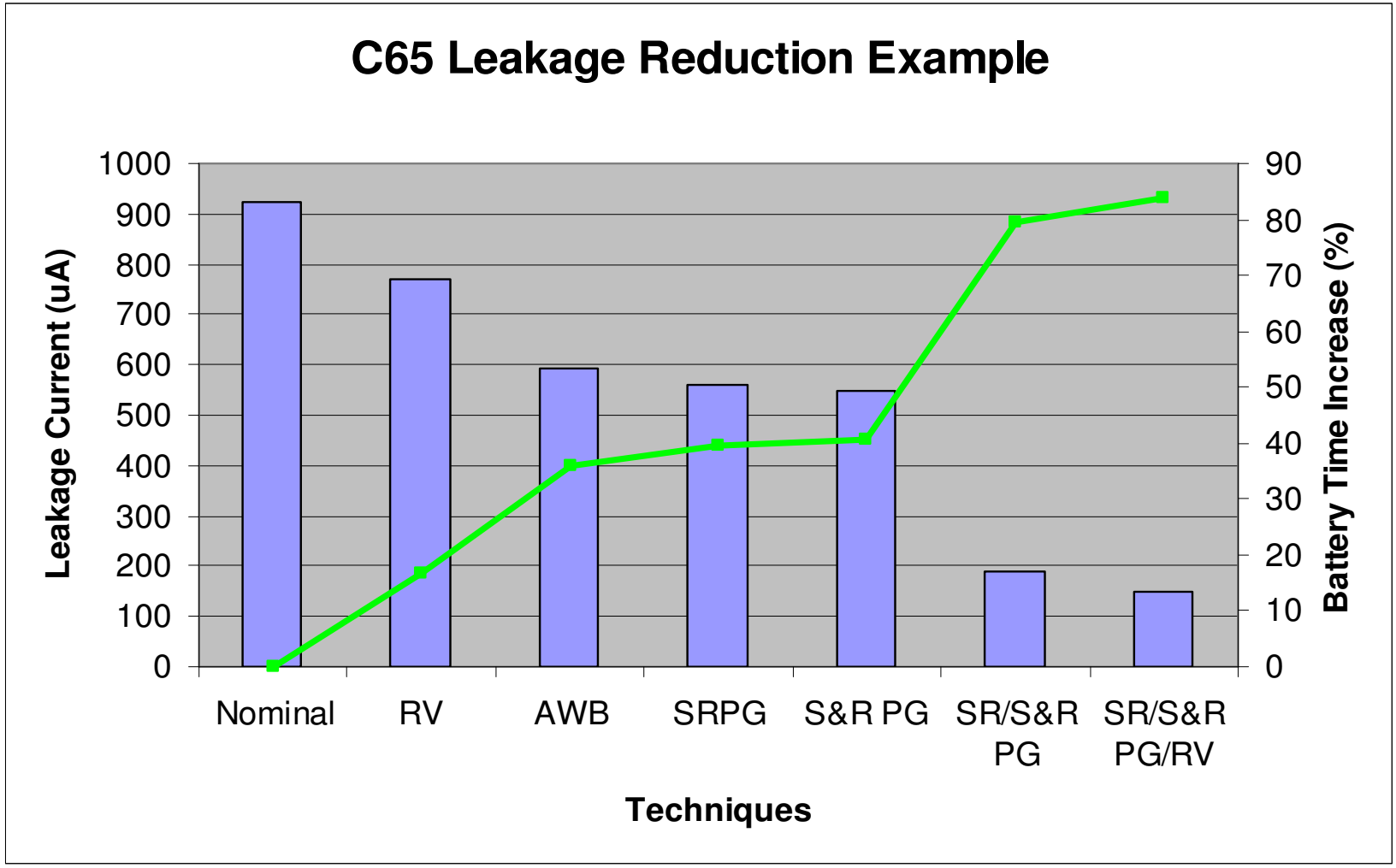
Static Power Design

- Static Power is crucial for defining standby time of cell phone.
- Multiple Leakage Reduction Techniques
  - Active Well Biasing (AWB)
  - State Retention Power Gating (SRPG)
  - Save and Restore with power gating. (S&R PG)
  - Complete Power Shut Off with Isolation.
  - Aggressive Voltage Reduction during standby mode (RV)
  - Multi-Vt based design styles
  - Device biasing.
- In cases, Static Power a big part of active power
  - Use switches for power mode switching.
  - Thermal dissipation issues in packaging.

Example Leakage Reduction Techniques



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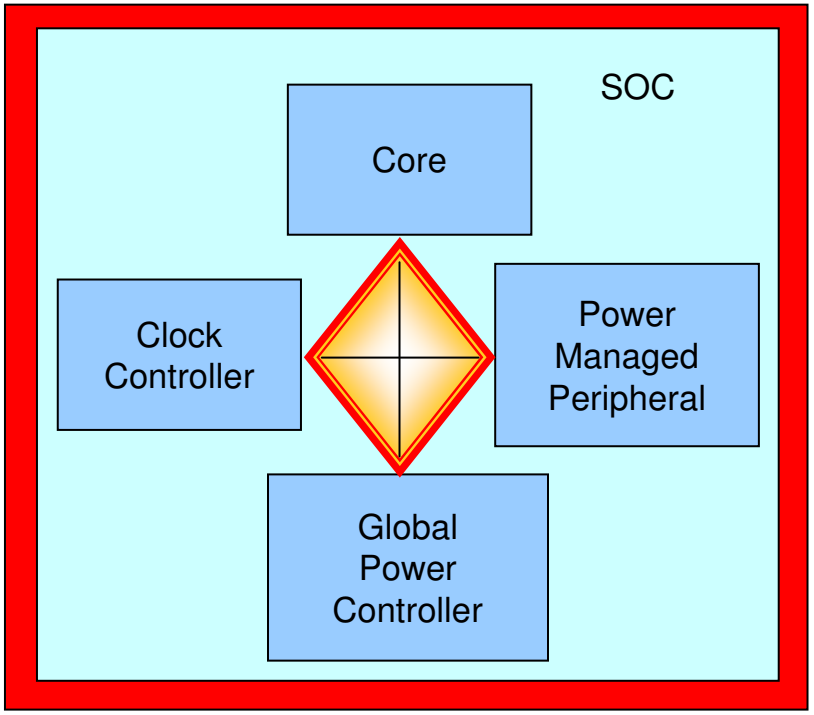
Multi Voltage Design Styles & DVFS

- Voltage has quadratic effect on power.
- Lower performance can be reached at lower voltage.
- Voltage partitioning decision is crucial and key for power performance optimization.

- A Simple Definition of multivoltage design style
  - Unused portion of design is switched off.
  - Low performance portion is running at lower voltage
  - High performance portion is at higher voltage.

- Clocking is the major challenge for multivoltage designs.
  - Clock timings shift with voltage and hence timing optimization has become much more complex.
  - Need intelligent clock tree tools.
- Asynchronous styles can enable efficient voltage partitioning.

Power Control Diamond



Power Control Diamond

►A Centralized controller for required power related operations.

►The controller has to handshake multiple components before making final decisions.

►Power management must be consistent across the entire chip.

Power Aware Verification and Debug

- Architectural analysis required to achieve efficient voltage partition.

- Global Power Controller
  - Partial or full power up and power down is a controlled sequence.
  - Verify the sequence control and state machine completely.
  - The Global Power Controller should be capable of capturing and relinquishing the controls appropriately.

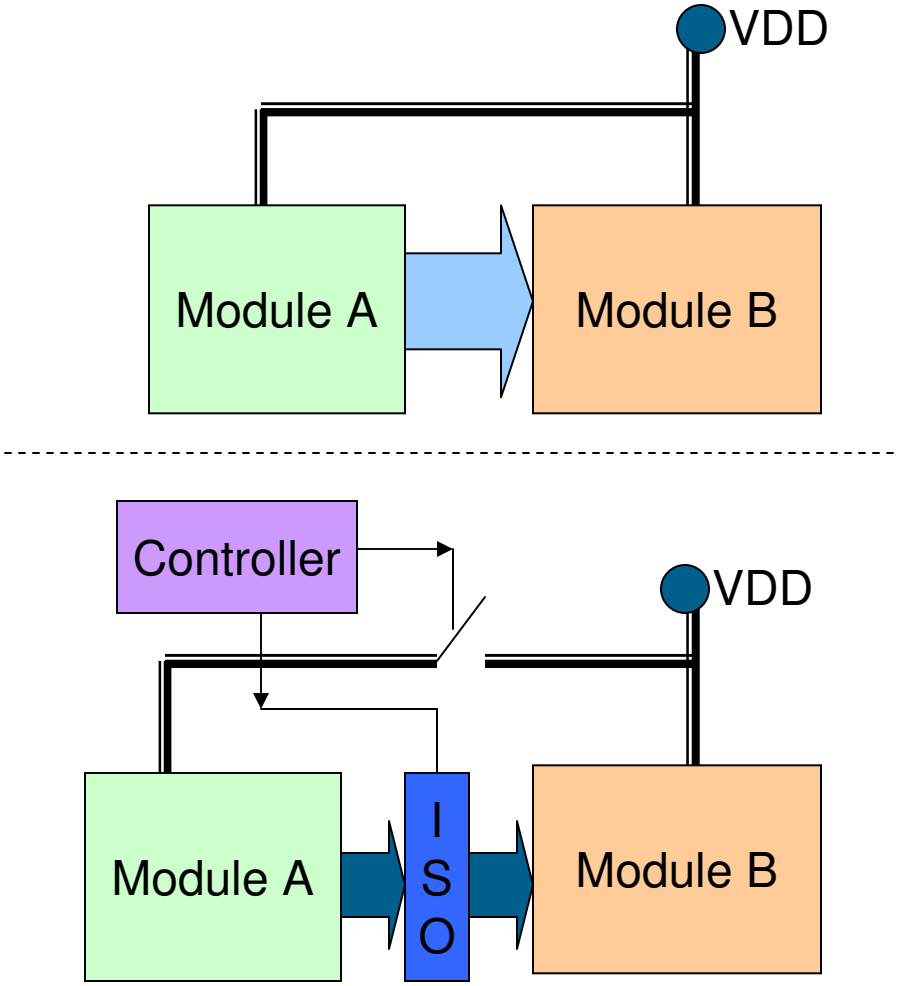
- The system should be functional and must be verified
  - During power off process
  - After power off has completed
  - Power up decision making
  - During power up
  - Full recovery after power-up.

- Debug of these power features at silicon is very complex.

- Ensure consistency of Power Programming Model in specification.

Isolation and Percolation

- ►Picture power managed vs non power managed design implementation
- ►When a module is powered off, outputs will float.
- ►These outputs can corrupt the state of receiving modules.
- ►Modules must be isolated
- ►A separate logic is inserted to isolate and percolate.
- ► Logic State of isolation is important and can cause adverse effects if improper.



Retention Verification

►A module can be turned off to save leakage.

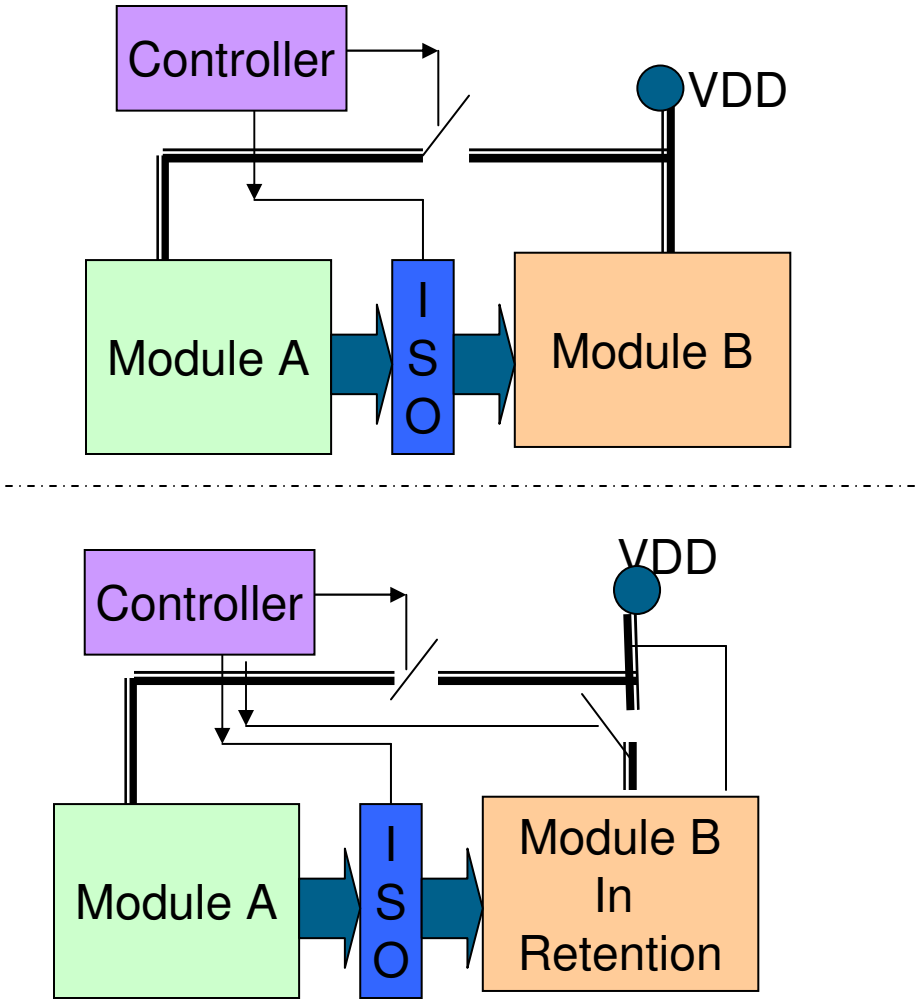
►The state of module B must be retained during power off.

►Special circuits and flipflops have been created for this purpose.

►Need to verify

- The state was saved correctly.
- State restored correctly.
- System can function after powerup.

►The controller must ensure the correct save & restore elements and sequences.



Voltage and Frequency Variation

►Voltage of module A is reduced when lower performance need.

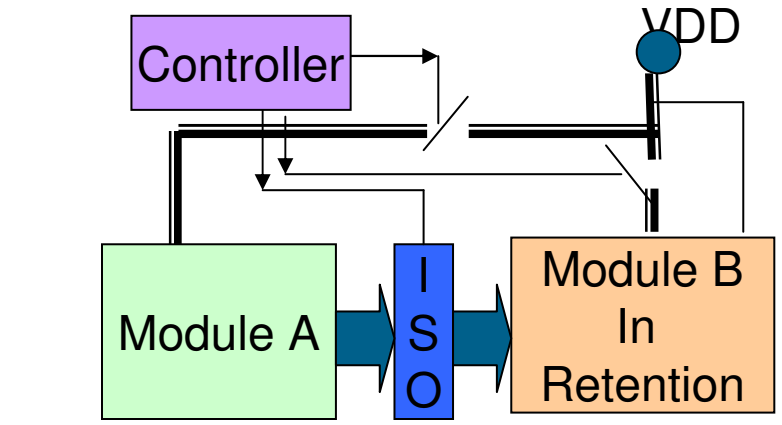
►Change of voltage is associated to change of Clock.

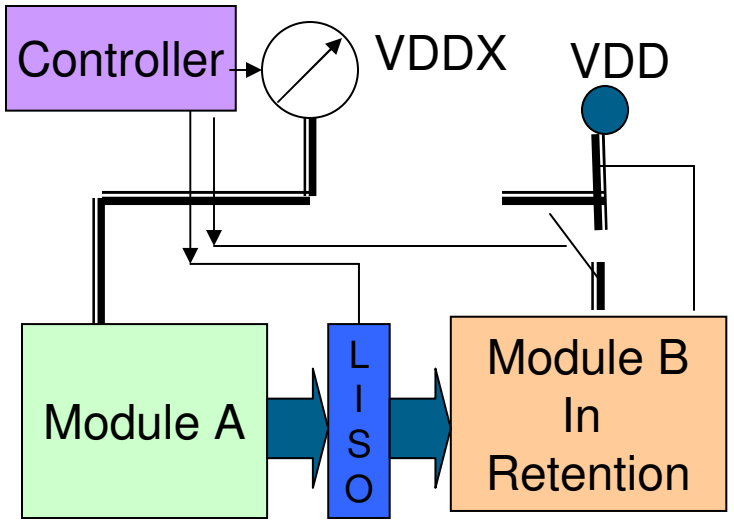
►Isolation is now Lisolator. (level Shifter & isolation)

►Need to verify

- System performance state.
- Prepare & communicate regarding voltage change..
- System operational during change.
- System operational after change.

►The controller must ensure the correct operating sequence and monitor progress.





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How Does the world of Verification Change

- Verilog does not have a concept of power on/off.
- Verilog does not have association of voltage levels.
- Gate level and circuit level simulations are expensive and time consuming and very late to fix the problems.
- Functional coverage of state of system at the time of power off and activities following power up should be gathered
- All power related features must be checked at RTL stage.
- Power Equivalency Checks needed between RTL & gate.
- Power estimation in various functional mode needs to be integrated with power verification.
- Power Aware PLI formulation standard.

Low Power Design Needs

►Support Low Power Design Techniques consistently through out the entire design flow.

- Design Representation
  - Accurately define and capture the low power design intent, modes and constraints.
- Design Implementation
  - Floorplan and power grids.
  - Common constraints for all tools (Synthesis, APR, timing, DFT)
  - Design analysis tools with single power constraints.
  - Accurate power estimation and measurements
- Design Verification
  - Voltage oriented simulators
  - Various static power technique modeling and simulations.
  - Silicon validation and correlation.

Take it To Next Level

►Decisions made at system level have a large influence on power optimization.

►Enable System Level trade-off analysis with Low Power features.

- Accurate estimation of power performance ratio.
- Power vs Area trade off analysis is very important.
- Retain consistency through out the entire flow.

Thanks!

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