



Words of Power: Reusable, Holistic, Scalable Multi-voltage Design.

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Outline

- ▶ Why Low Power is important
- ▶ Trends in Low Power implementation
- ▶ New techniques more intrusive on the implementation
- ▶ Power Network representation
- ▶ Power mode verification
- ▶ Hierarchical use model of power intent format
- ▶ Conclusion



Less **Operating power** is important

- ▶ For cost sensitive battery operated devices with no stand-by mode
 - Convergence of computing, communication & entertainment increase the complexity, requires higher level silicon integration and more battery life time
 - Exotic heat dissipating packages are costly
- ▶ For Home consumers who want products that enhance the user environment
 - Reduced noise (no fans)
 - Cooler running (lower power dissipation)
- ▶ Must be addressed at all design levels
 - Transistor, Logic, RTL, Interconnect, Architectural, System



Less leakage power is important

- ▶ For handheld devices with stand-by requirements
- ▶ The Perfect Storm
 - Customers want smaller, cooler mobile devices at lower cost
 - The convergence of computing, communication and entertainment on mobile devices leads to
 - A dramatic increase in functionality and complexity
 - More demand on battery life time
 - Requires high levels of Silicon integration in advanced processes, but ...
Advanced processes have inherently higher leakage current
- ▶ Addressed by
 - Choice of process, library options, threshold, and design techniques



Low power implementation trends

- ▶ So far:
 - **For dynamic power**
 - Reduce power dissipation source when not needed.
 - Minimize switching capacitances.
 - **For leakage power**
 - Use of multiple $V_t(s)$ synthesis / optimization

- ▶ More recently:
 - **For dynamic power**
 - Use voltage islands and frequency scaling to meet both chip performance requirements and operating power goals.(Dynamic and Adaptive Voltage and Frequency Scaling)
 - **For leakage power**
 - Suppress current when not needed.
 - Intrusive on functionality
 - Impact across design tasks (Design-In and Implementation)
 - Island of voltages increases the complexity and throughput time of implementation.



New laws, New cells, New constraints

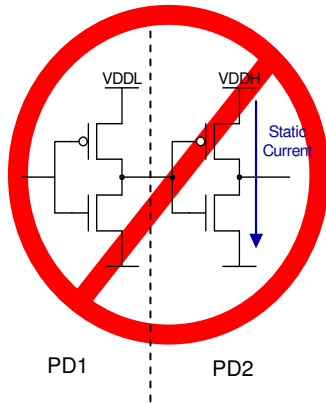
- ▶ Level shifters
- ▶ Isolation clamps
- ▶ On-Chip Switches
- ▶ Retention

Specifying intent for automated implementation and verification is very complex



Level Shifters

▶ With Multiple Supplies

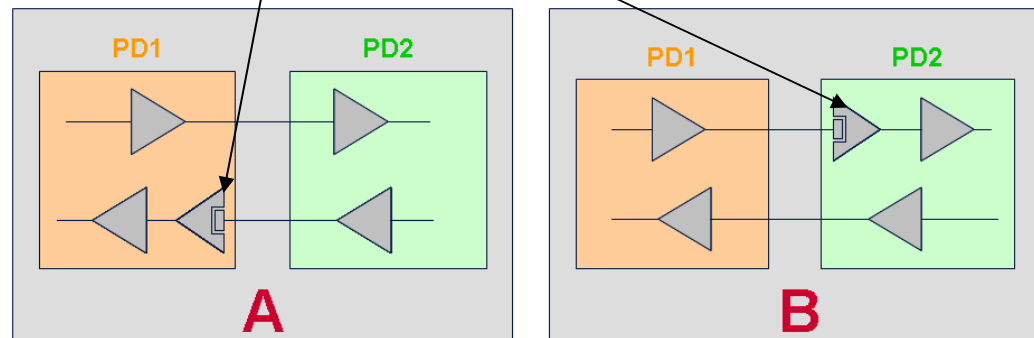


- ▶ Cannot directly connect V_{DDL} and V_{DDH} cells
 - Output of V_{DDL} gate can't be raised higher than V_{DDL}
 - When connected to V_{DDH} gate, PMOS will never be completely cut-off → Static Current

- Use Level Shifters

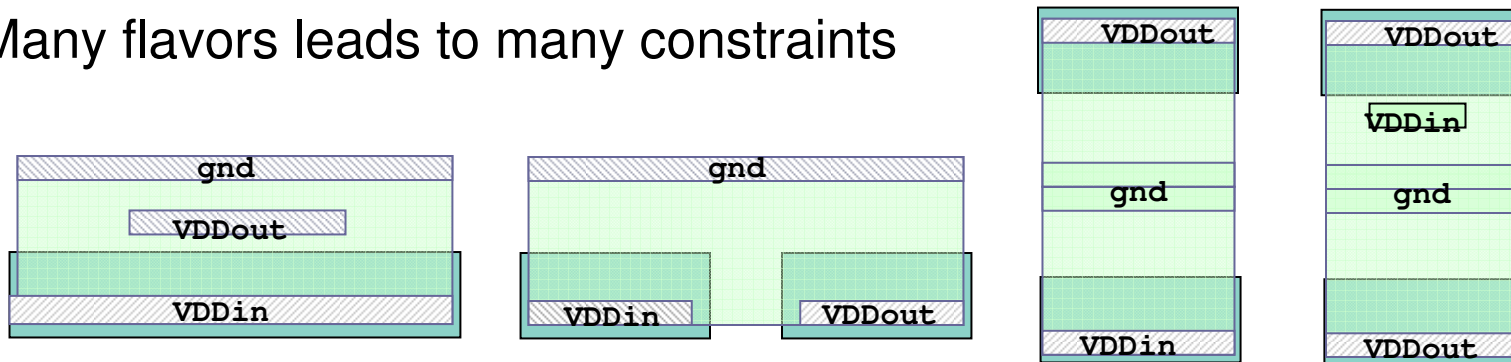
▶ Quiz → 2 modes:

- | | | |
|-----------|------------|------------|
| | PD1 | PD2 |
| - Mode 1: | 1.2V | 1.2V |
| - Mode 2: | 0.9V | 1.2V |

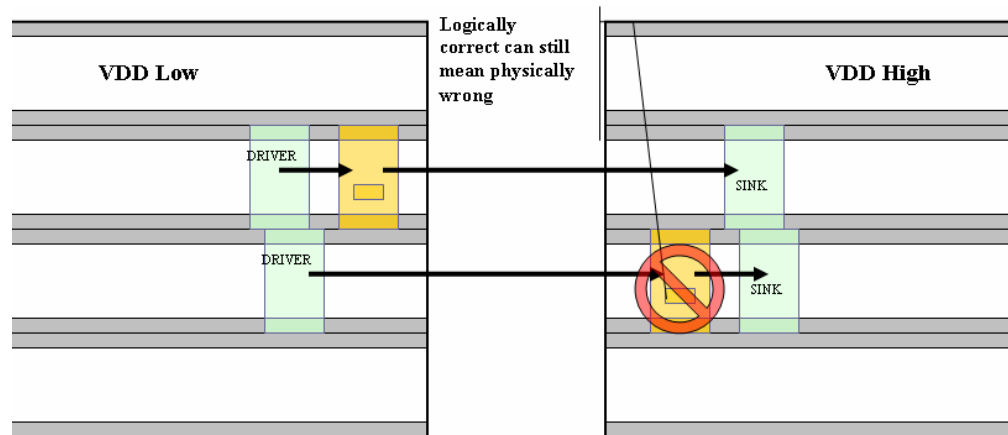


Level shifters introduce layout constraints

- ▶ Level shifter are leaf cells with 2 supplies
- ▶ Many flavors leads to many constraints

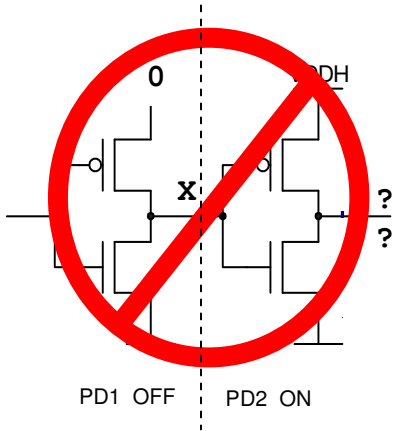


- ▶ Logically correct can still mean physically wrong



Isolation clamps

- ▶ For power switching

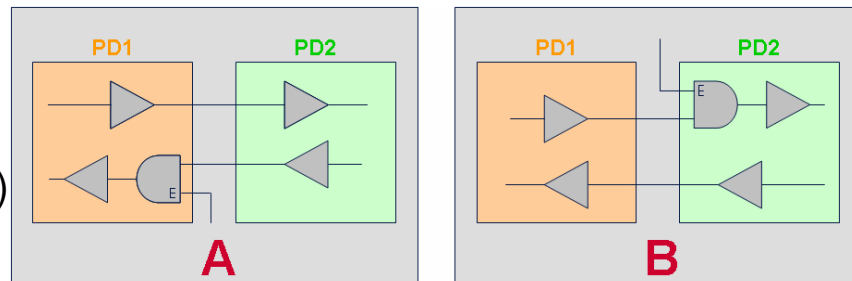


- ▶ Cannot directly connect output of a powered down block.
 - Can propagate unwanted data in the logic driven
 - Floating input will potentially generate short circuit current.
- Specific Inactive state or reset values may be forced on inputs driven by power down logic

- ▶ Quiz → 2 modes:

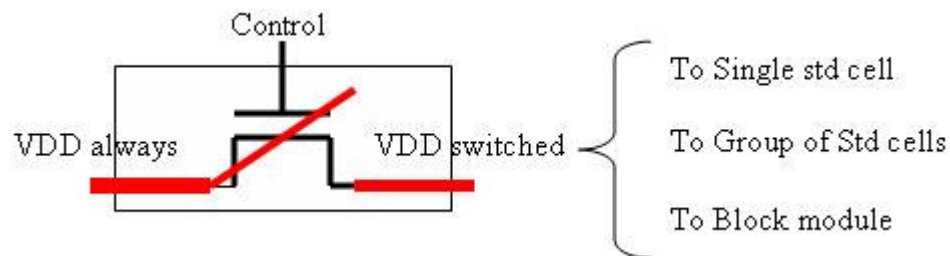
PD1 PD2

- Mode 1: 1.2V 1.2V
- Mode 2: 0.9V 0.0V (power down)



On-chip switches

- ▶ Voltage islands are turned ON/OFF with on-chip switches
- ▶ Many flavors

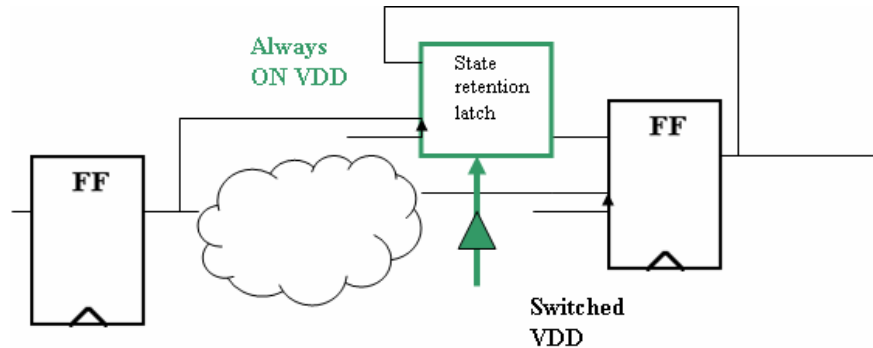


- ▶ **Constraints and requirements**

- Power distribution and floorplanning is more complex
- Switches need proper sizing: Balance current carrying vs area and leakage
 - Static IR drop analysis is necessary to verify sizing
- Sequencing of the Control signals influences wake-up time and inrush current.
 - Transient analysis is required to assess impact of a switching block on surrounding

Retention

- ▶ Many possible variants : integrated cell or shadow register with or without save & restore.



- ▶ Constraints and requirements
 - Block with retention will have several supplies.
 - Retention may require always-on buffer tree to the control signals.
 - Connection of supplies is error prone and time consuming. Difficult to rely on global connection with pattern matching on pin or instance names

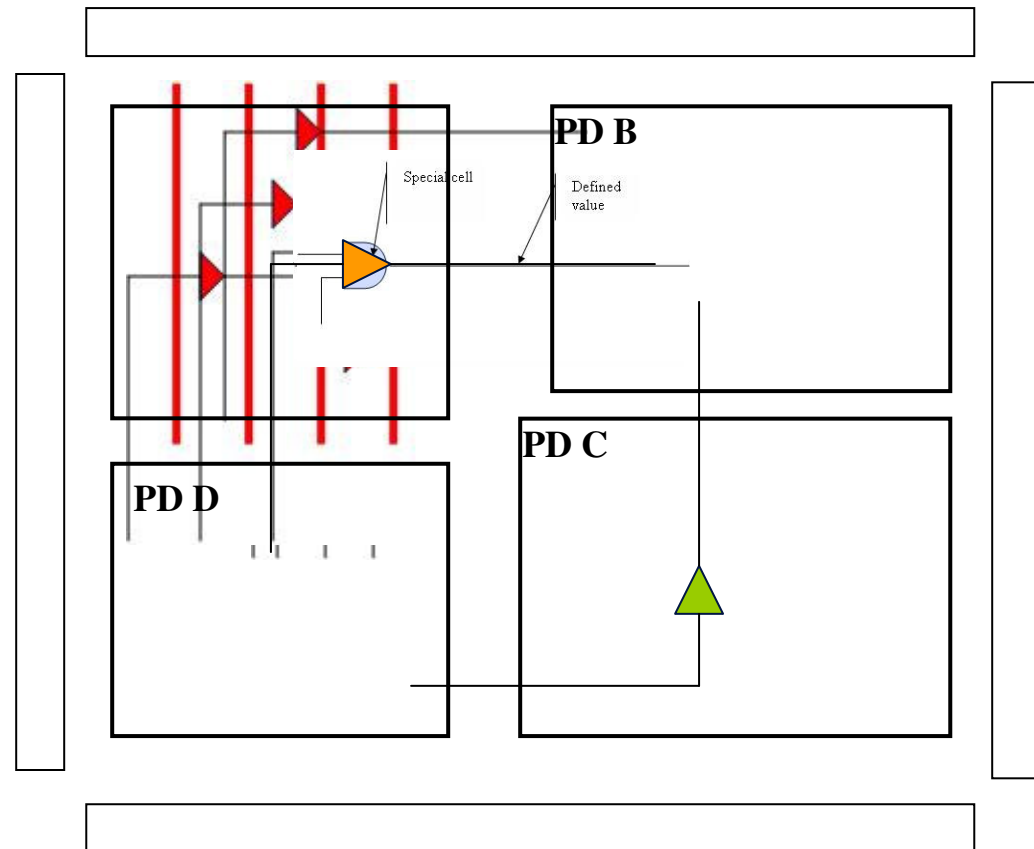
SoC is more complex

- ▶ Signal distribution
- ▶ STA
- ▶ DFT
- ▶ ...

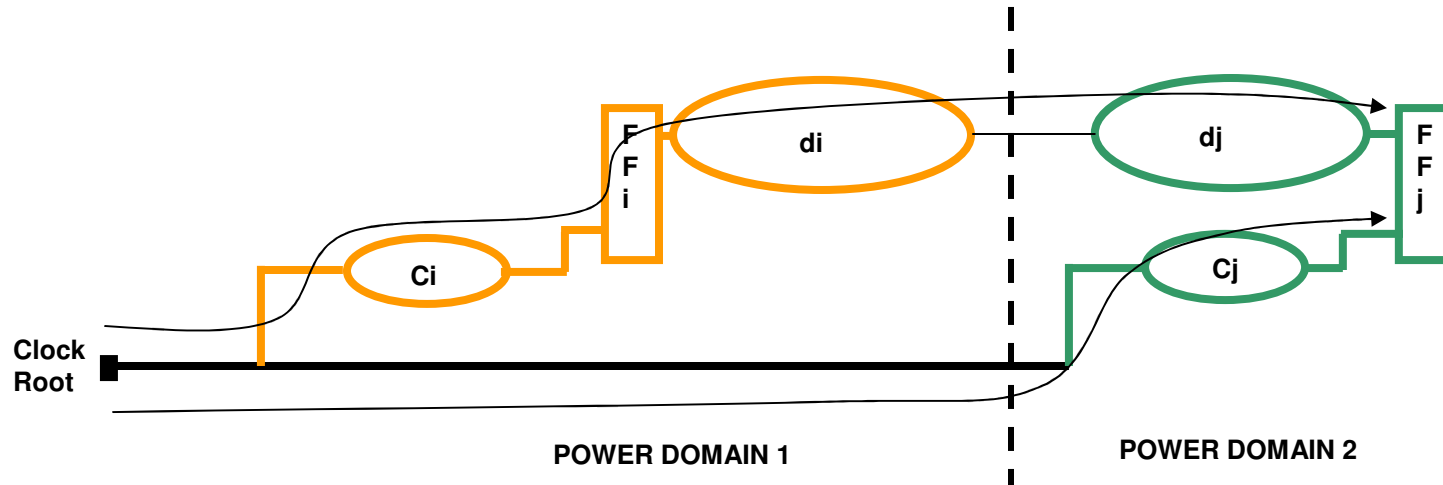
The total problem is more than the sum of its parts

Signal distribution

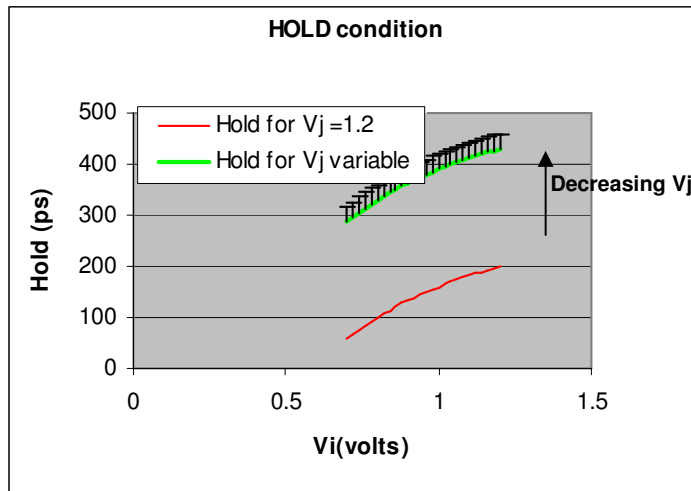
- ▶ Combined Level shifter clamps are usually necessary
- ▶ Multiple implementation are usually possible. Generic rules are often needed but all have pro's & con's
- ▶ Global buffering strategy and power distribution are complex
 - Special buffers
 - Gas stations
 - ...
- ▶ Goal is to minimize special handling during floorplanning and layout
- ▶ Not always possible. Certain design tasks do get more complex



Power Domains Interfaces – Rule of thumbs



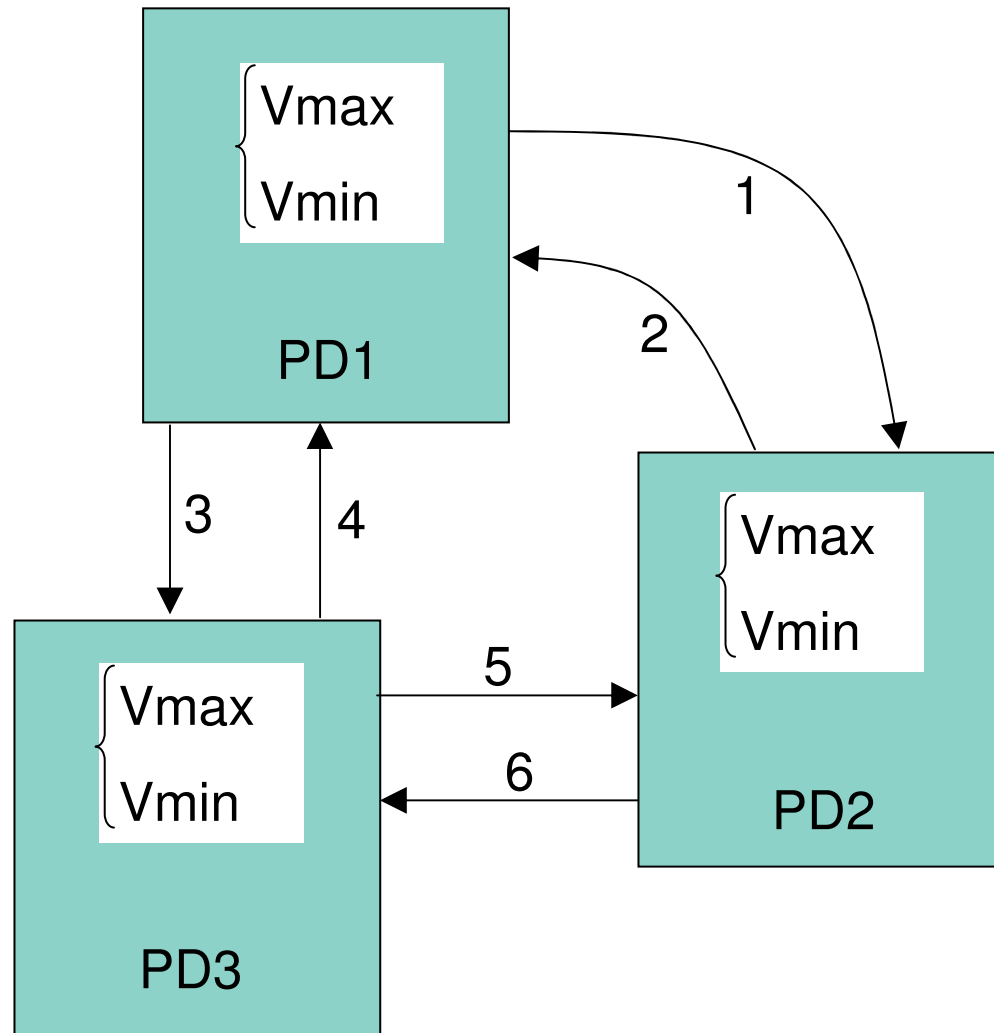
HOLD CONDITION $\min(di + dj) > Cj - Ci$



Sign-off hold at highest voltage on driving end.

Sign-off hold at lowest voltage in receiving end

PD Interface – Rule of thumbs



Voltage corners ?

1- PD1(vmax) PD2(vmin)

2- PD2(vmax) PD1(vmin)

3- PD1(vmax) PD3(vmin)

4- PD3(vmax) PD1(vmin)

5- PD3(vmax) PD2(vmin)

6- PD2(vmax) PD3(vmin)

- Number of corners and STA runs can explode
- Blocks will have operating conditions , constraints and libraries that will be combined to create many analysis and optimization views.
- This needs placeholder and abstraction for proper management.

DFT impact

- ▶ Insertion of scan chains across voltage islands can complicate implementation
 - Test Control Block needs to be assigned a power domain
 - Scan chains may span across PD and require LS
 - Commercial Tools are not MSMV aware yet
 - CTAG may span voltage domain boundaries. Isolation should be placed in domain of IO pin.
 - Scan chain routing within the bound of the voltage islands is preferred over random stitching of scan flip-flops across the voltage islands.
- ▶ If all power sequencing circuits will be held to power-on state during test operation, scan chain may not have to be designed based on Voltage islands...
- ▶ Testability of LS, switches ...

Way Forward

- ▶ Scalable Solutions
- ▶ Capture Power Network intent
 - Placeholder format
- ▶ New Tool functionality
 - Verification
- ▶ Reuse



Scalable solutions

- ▶ We have in some cases experienced 2X productivity drop for the implementation phase.
- ▶ It is not sufficient for tool vendors to address these areas by simply providing the basic low level hooks in their tool infrastructure.
- ▶ Tools understanding the same power design intent with the highest possible level of abstraction are needed to compensate the throughput time overhead introduced by designing with multiples supplies.

Power Network Intent

- ▶ Power and Ground traditionally defined and implemented in the layout phase as they had no functional impact (other than being necessary)
- ▶ Power gating is making PG nets partly functional as the behavior of the device depends on their state (clamping value) and level (performance)
- ▶ RTL does not have implicit representation of these nets, nor do the logic views for the leaf cells.

- ▶ Standardized placeholder with a defined semantic
- ▶ Separate from the functional specification. Power intent may change
- ▶ Golden reference
- ▶ Design Specification = {Power Intent, Functional specification} pair



Why a Common Format ?

- ▶ Power information is sometimes available as a paper specification, but very often only in the SoC architect's mind as it is not usually explicit in functional descriptions.
 - What hierarchy to what power domain, at what supply
 - What the power modes are
 - What block can be turned off
 - What block require retention
 - Level shifting done in both directions or only low to high supply
 - Where in the hierarchy should the LS / isolation be inserted
- ▶ Many implementation tools now need to understand this information, today recaptured as many times as required.
- ▶ Should separate intent from implementation such that early exploration of different power architecture intent can be done
- ▶ Support mixed description (already added “low power logic” with “non power aware RTL”



Common Format

- ▶ Good news is we went from no format to some format
- ▶ Bad news is we went from none to one too many
- ▶ Tools now need to understand this format and add value with it.

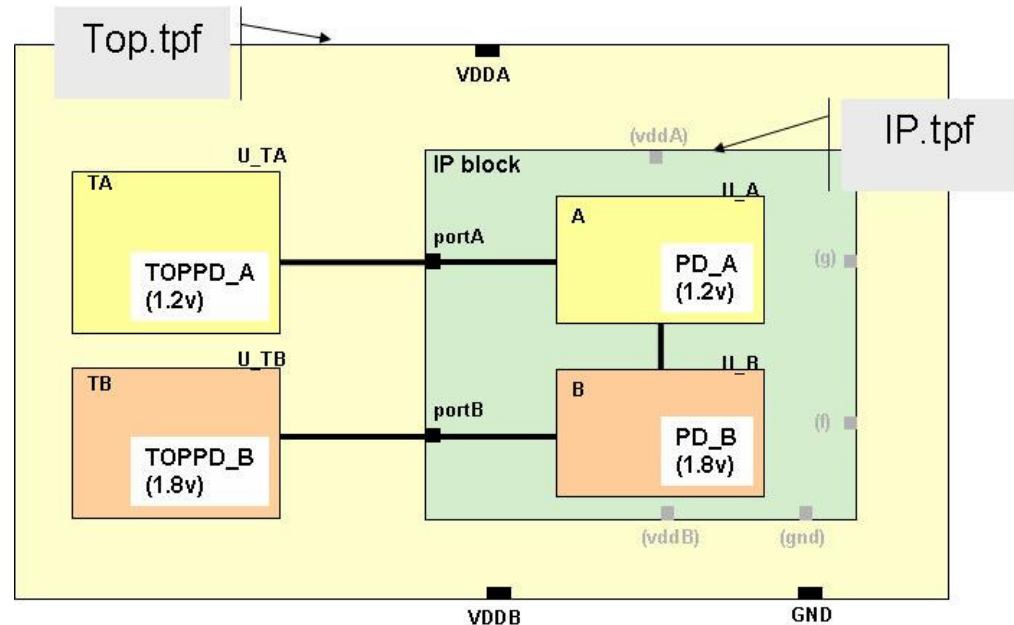
Verification

- ▶ Must be able to verify
 - the power down modes
 - clamping to the proper value
 - Retention save and restore
 - System recovery at power-on
 - ...etc in the context of RTL simulation
- ▶ Incisive Unified Simulator and CPF have proven to be useful to identify system bugs on a complex NXP device.



Use cases (1)

- ▶ Tools and Format must support Hierarchical usage of Power Intent description

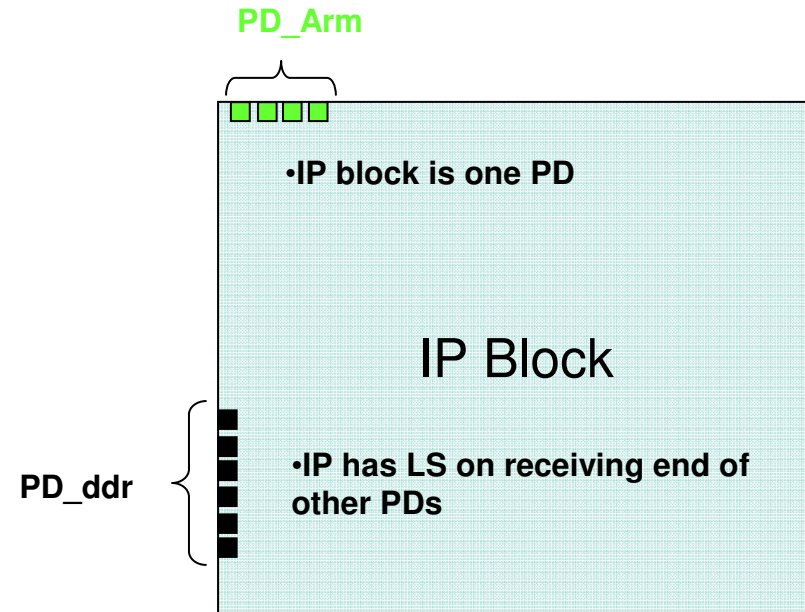


- ▶ Bottom-up reuse: Power design intent has been developed to implement an IP:
 - Soft IP
 - It should be reusable for the integration of this IP.
 - Must not have to rewrite the intent specification of the entire SoC.
 - Hard IP
 - Automatically be derived from the IP implementation.
 - Such description should also be usable to give IP visibility from the chip level for integration.

Use cases (2)

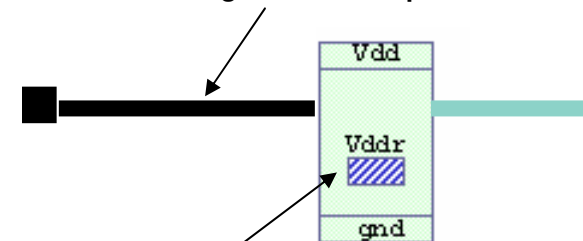
- ▶ Top-down constrain of lower level IP implementation:
 - Chip level power design intent is created.
 - Low level blocks should have their power design constraints derived from this chip level description.
 - Chip level context visible during IP implementation

Without doing MANUAL design / floorplan
Without specifying instance by instance
By staying at the abstract level



Need to :

Avoid buffering of nets from pin to LS



Properly Connect LS extra power pins to power distribution

Conclusion

- ▶ Low Power design needs to move from hand crafting to automation.
- ▶ NXP has been using existing solutions and driving tool vendor's additional functionality required for designing with Voltage Islands.
- ▶ There are 2 “version 1.0” standards different in every details, and alike in every intent. (GD – LSI)
- ▶ NXP is contributing to all industry forums where convergence may happen.
- ▶ Are we there yet ?
- ▶ A lot remains to be addressed
 - Separate rules from context
 - Library modeling and HDL extensions
 - Power aware DFT and testability of new IP
 - Hierarchy & reuse
 - etc

Thanks to Judith Richardson for her suggestions and help in reviewing this material



