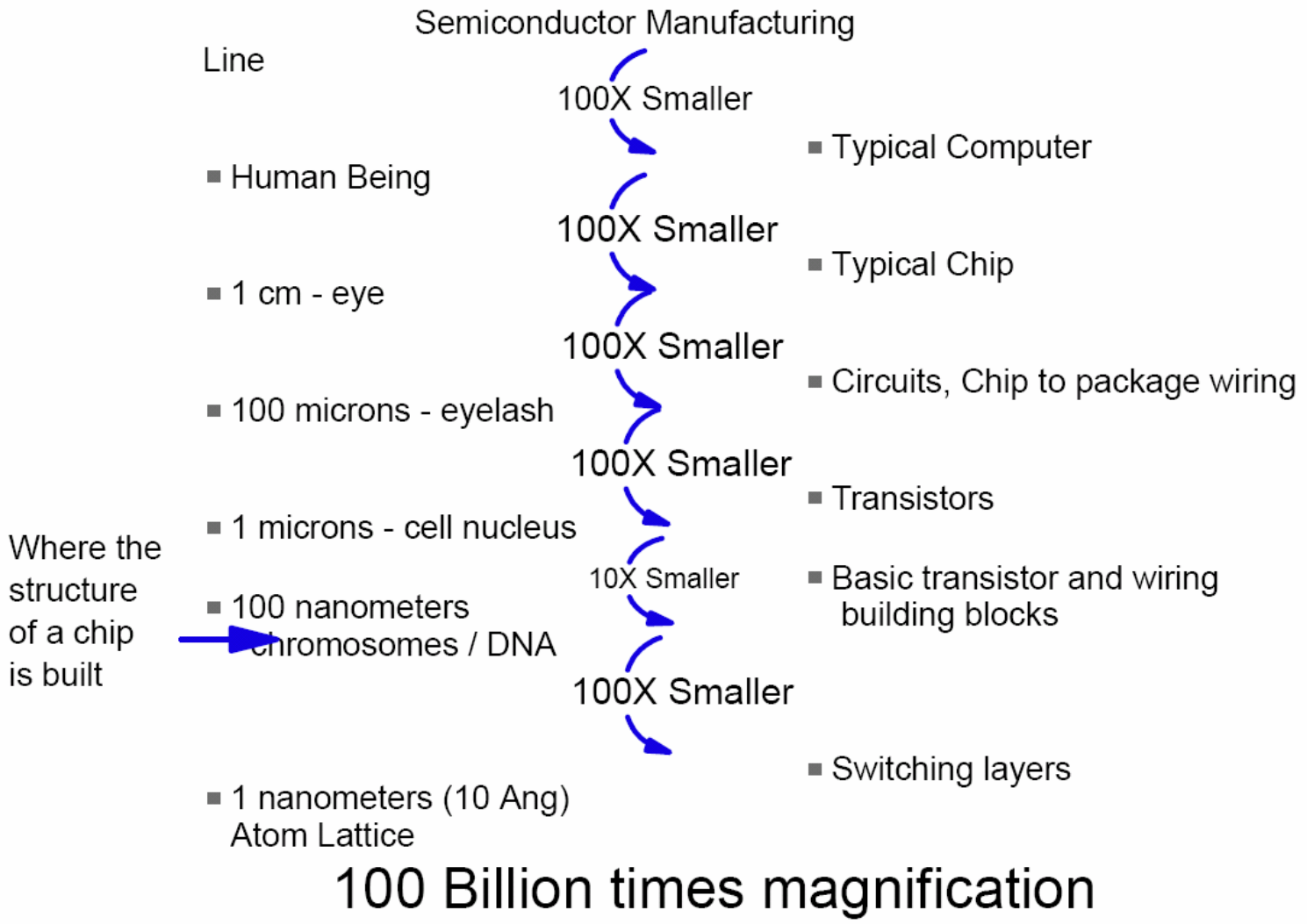
Design Rules: From Restriction to Prescription

Leon Stok

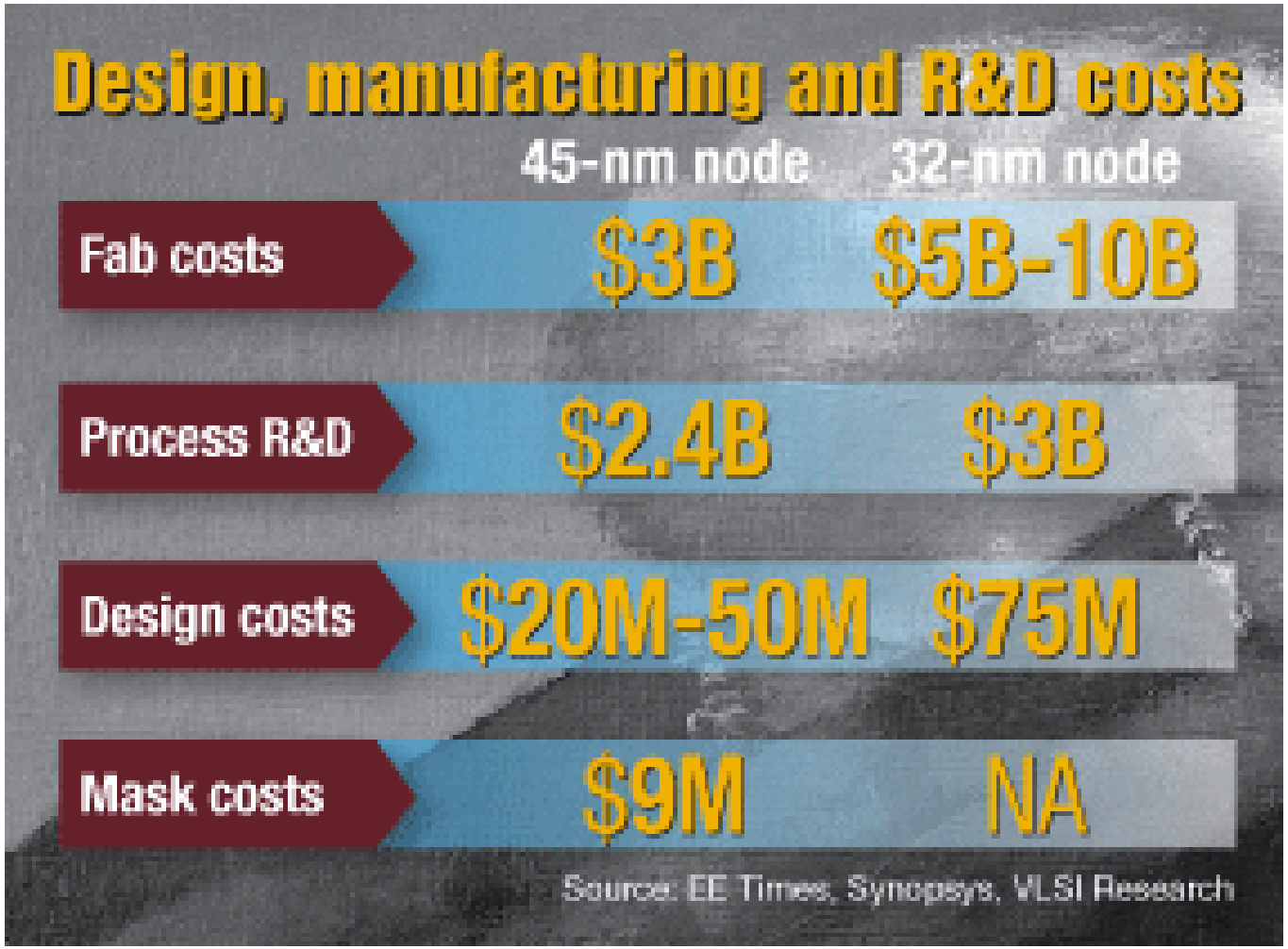
The Dimensions of the Age of Information Technology



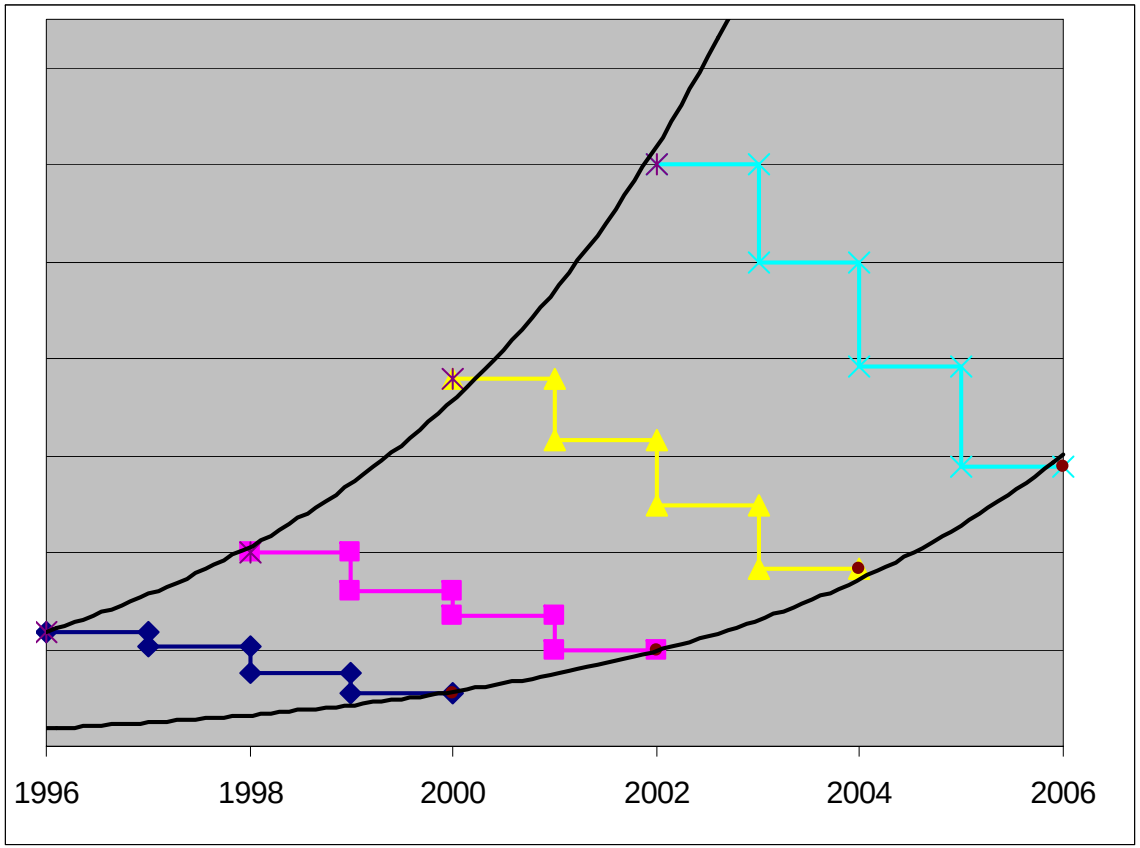
[Russ Lange, IBM]

Design, Manufacturing and R&D costs

- **Cost cast ICs into Darwinian struggle (ISQLED)**

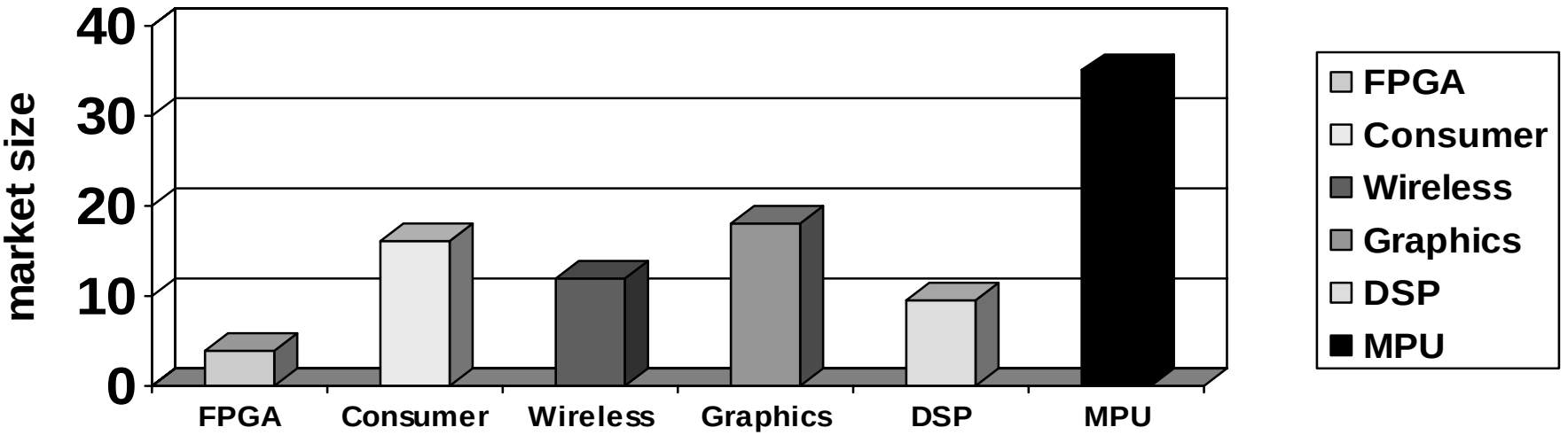


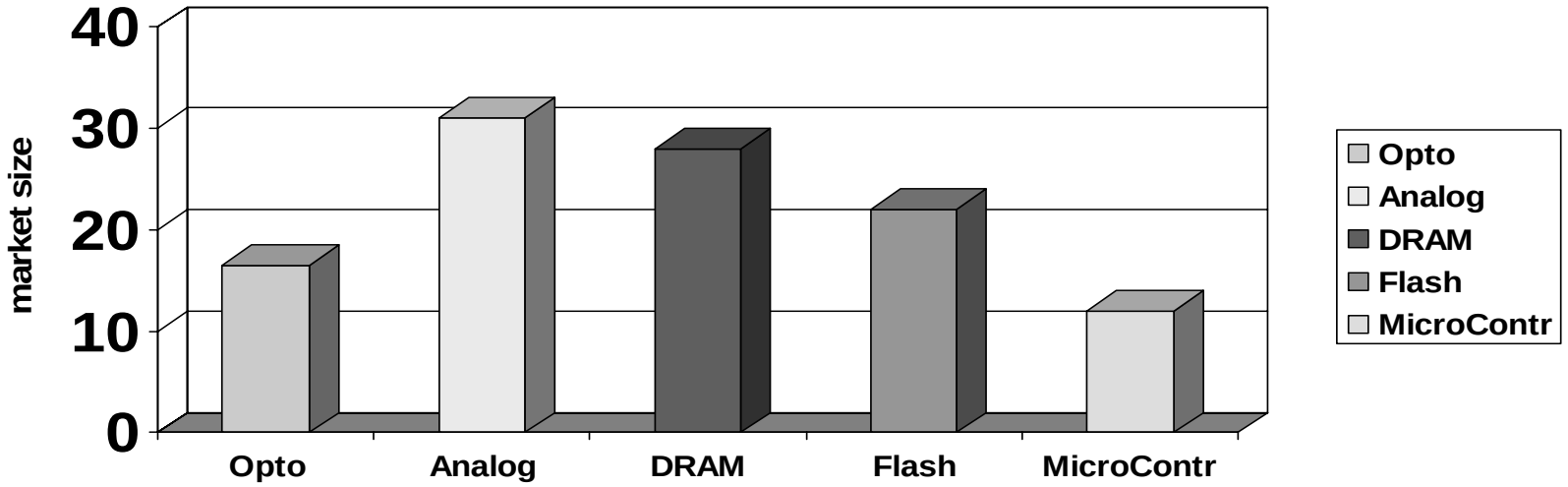
The untold story on Mask Costs



- **Hype on Mask cost does not account for learning.**
- **MASK YIELD ENHANCEMENT is lagging compared to process yields**
- **Better execute current techniques:**
  - Process controls, cleaning, inspection and repair.
- **New techniques and tools:**
  - Aerial imaging mask inspection uses.
  - AFM based repair
  - Multi-layer masks

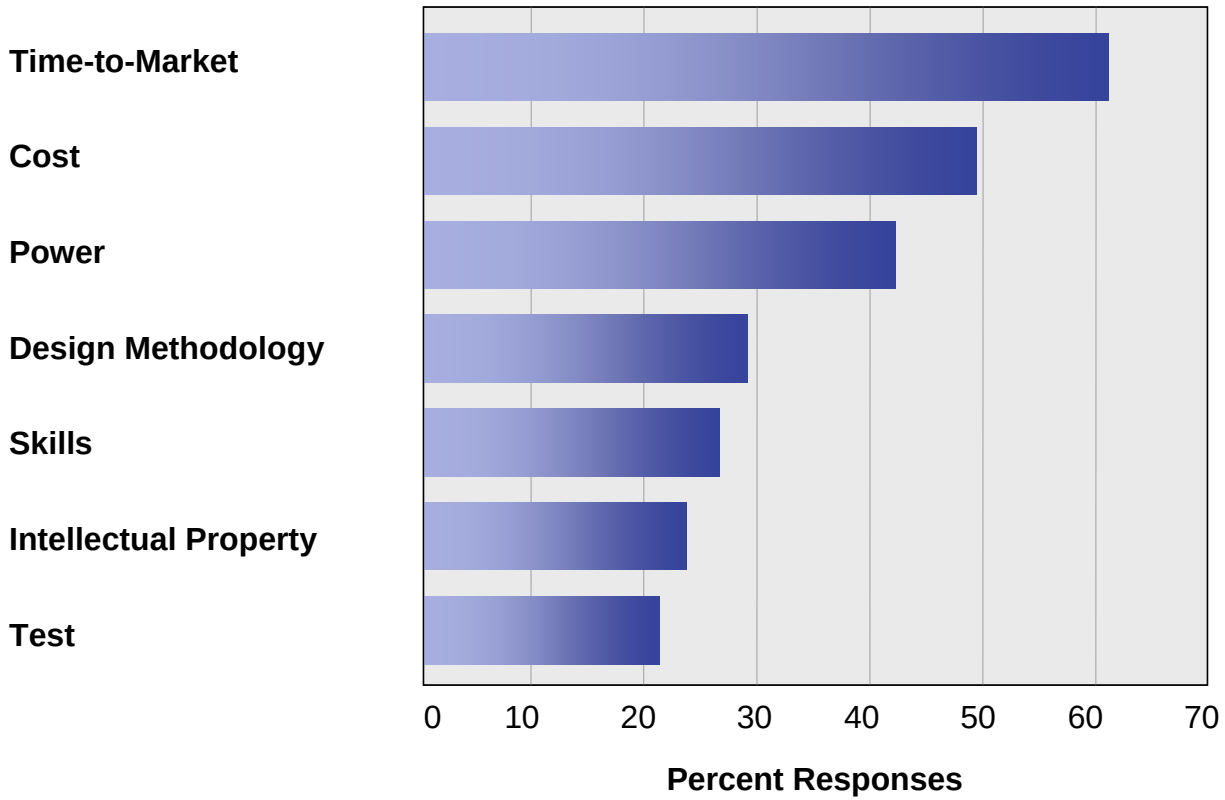
Semiconductor Market



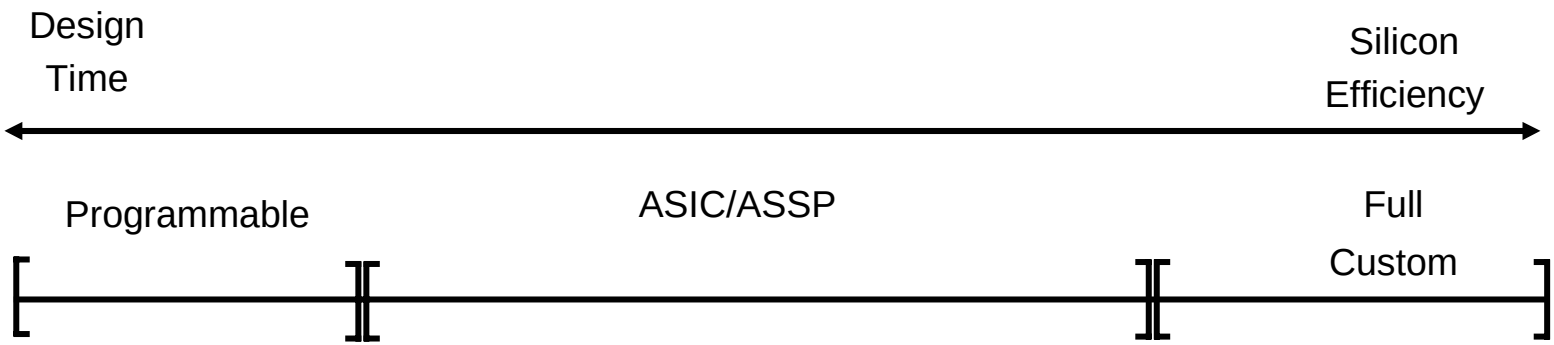


What is on the Customers Mind?

Top industry and business challenges specific to product development



Spectrum of Design Implementations



Markets

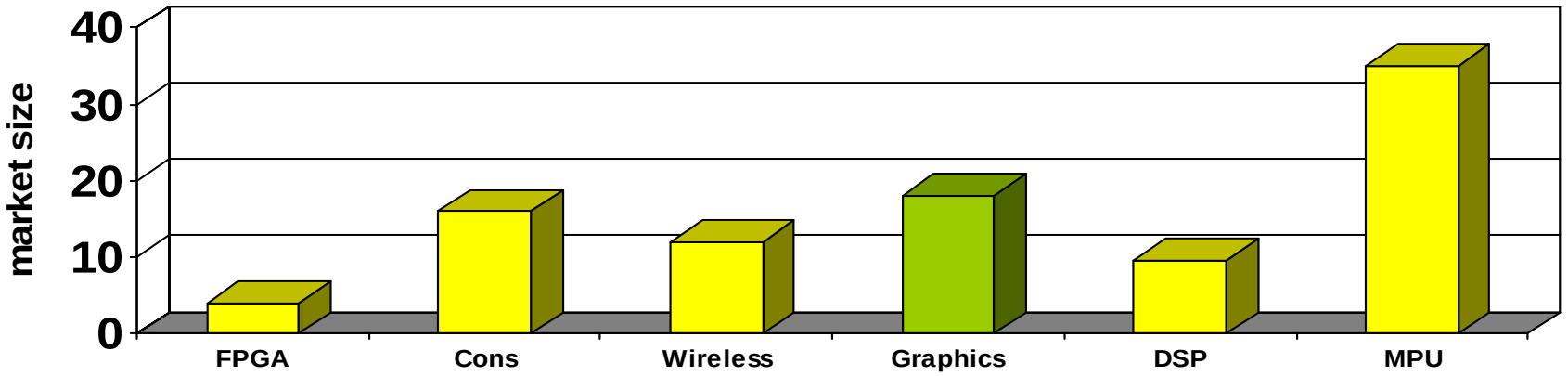
Micro-Processors

DSP

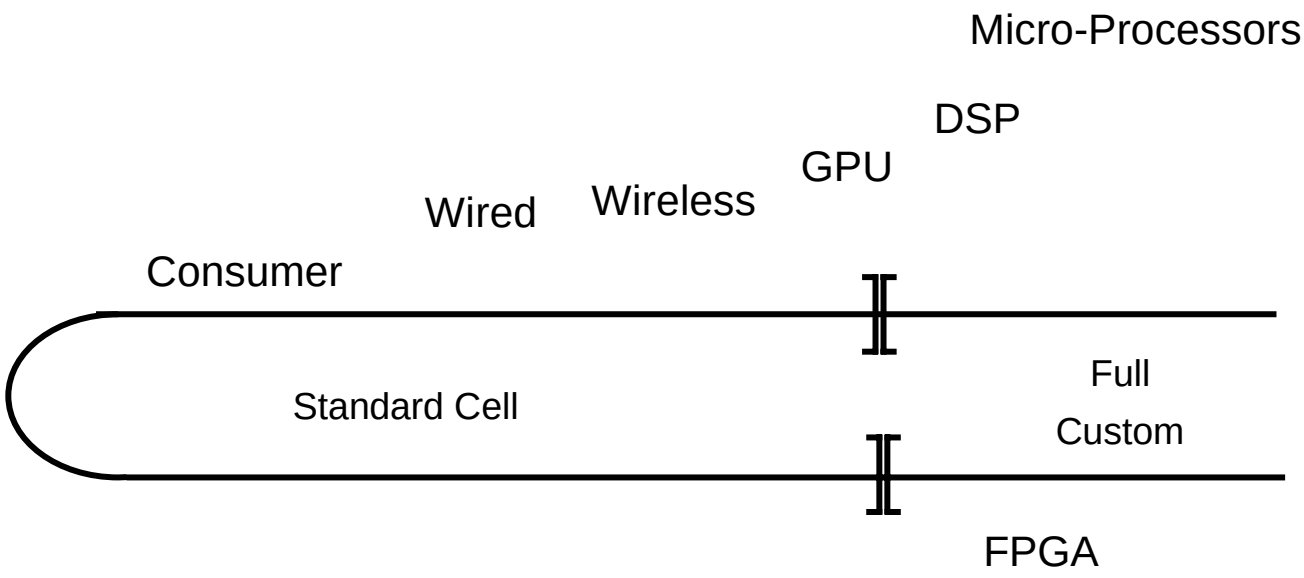
GPU

Wired Wireless

FPGA Consumer

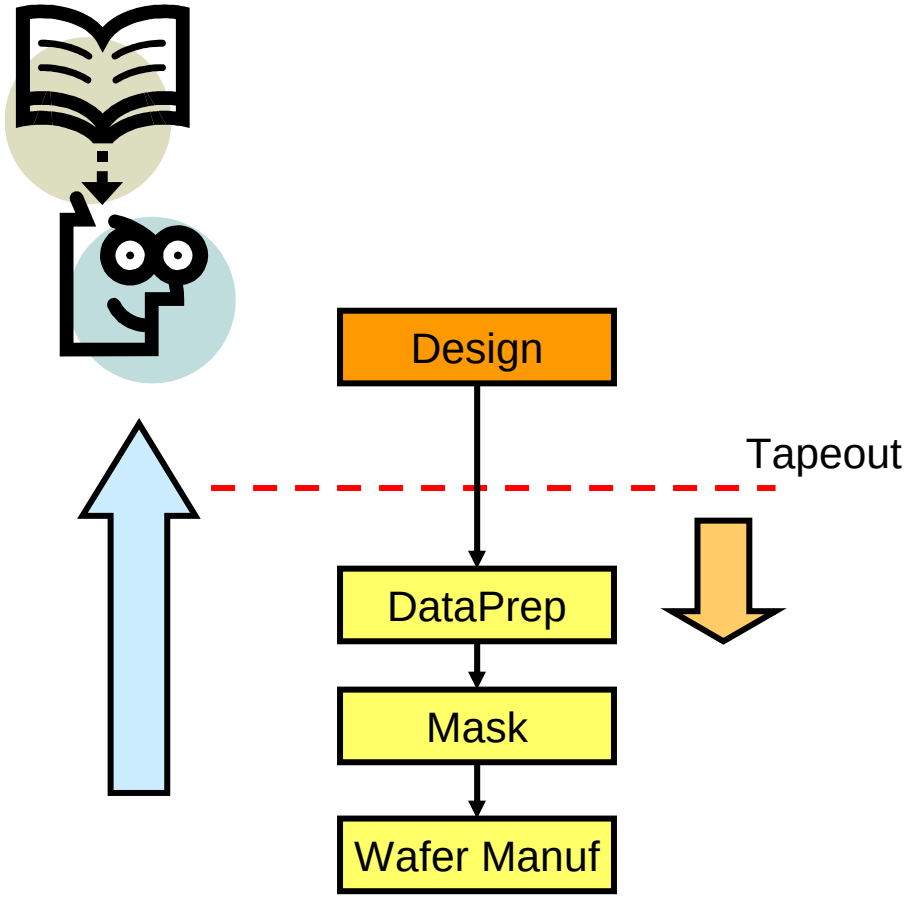


Spectrum of Design Implementations



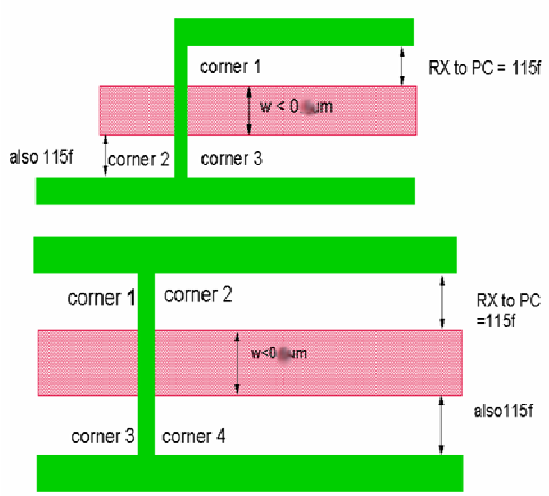
Hand-off Models

- **Design rule manuals**
  - 100-200 rules -> 600-700 rules and subrules
- **DFM == What information to?**
  - Feed backward across the tapeout line
  - Feed forward across tapeout line
- **Who signs on the dotted line?**

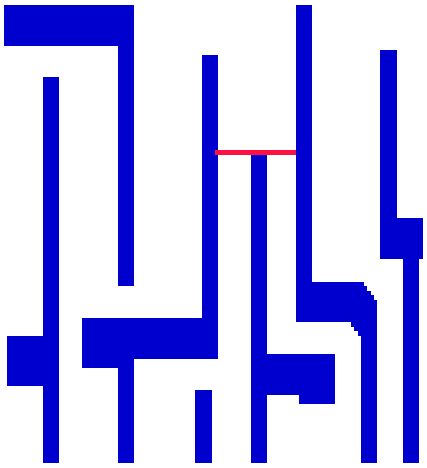


Design Rules

- **Difficult to formulate**
  - Especially early on in the process
- **Difficult to code**
- **Unique to specific environments**
- **Prone to errors**
- **Growing in number**
  - Design rule manual
    - 100-200 rules ->
    - 600-700 rules
  - and still Incomplete

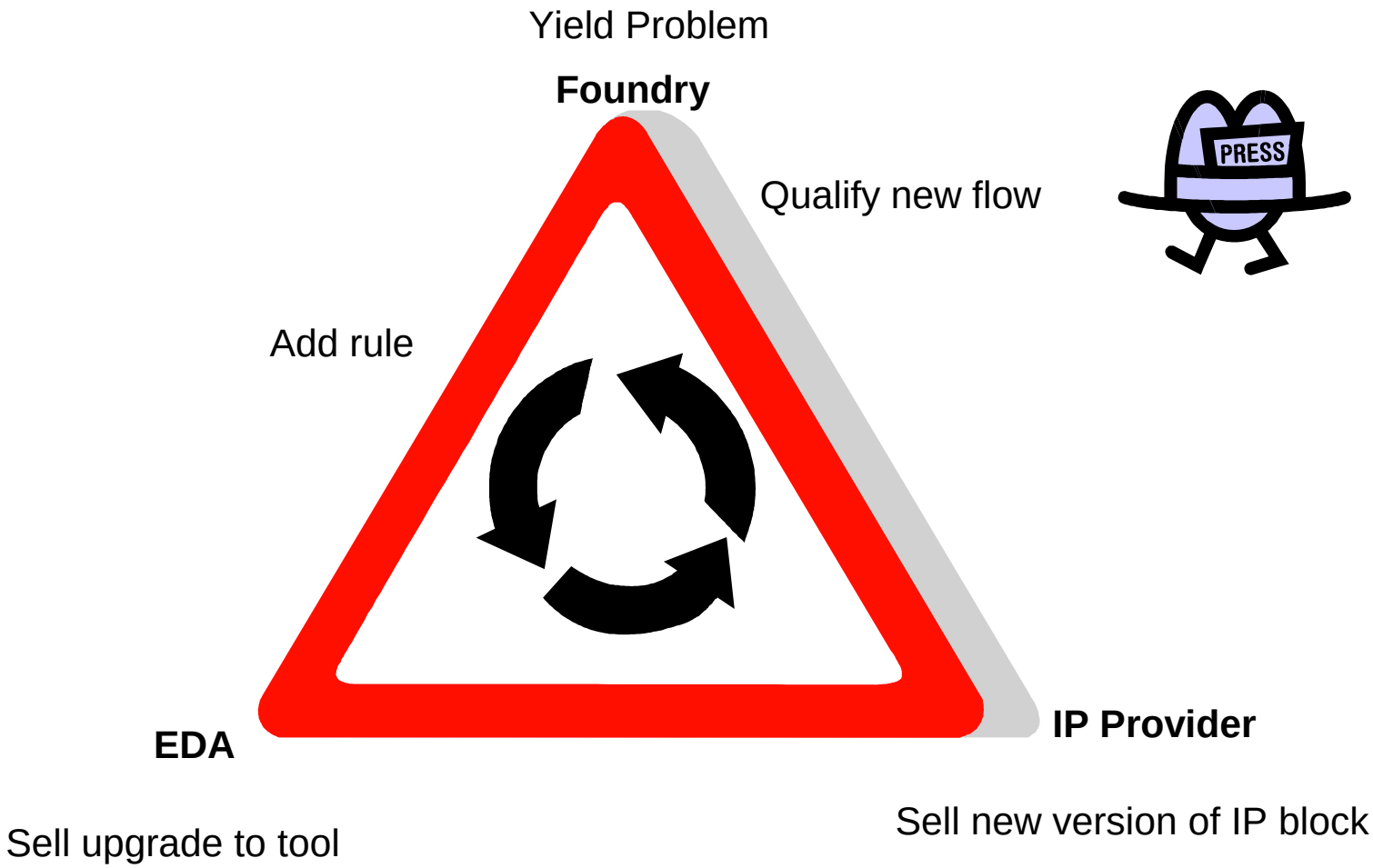


E.g. 115f PC inside corner* to (GATE not DECAP), for device width < 0.xx um and (GATE not DECAP) neighbored by more than 2 PC corners* [115f value determined from minimum device width of 0.yy um. For device width RX >= 0.qq um follow rule 115dd] >= 0.zz.



PS16	For 3 parallel PCc lines in which the middle PCc line-end is not flush with its outer neighbors, the (outer PCc line side) to (outer PCc line side) must be spaced	>=	0.380	need enough space to protect outer lines with block shapes and erase the residual phase transition with a trim opening= 2xBlock (260) + min-Block-Open (120)

Complexity Cycle



RDR

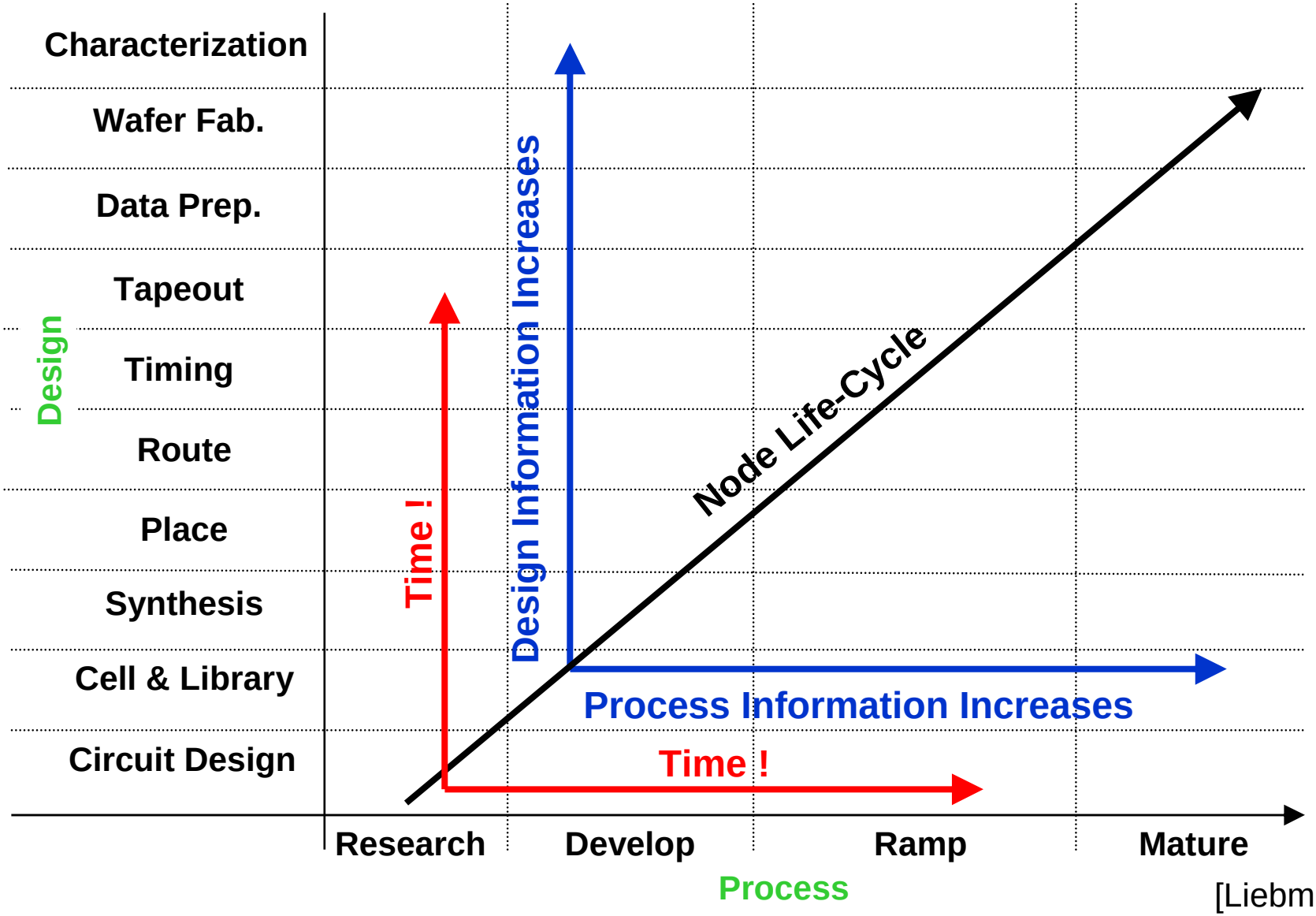
~~RDR = Relaxed Design Rules~~

~~RDR = Recommended Design Rules~~

RDR = Restricted Design Rules
(formerly Radical Design Restrictions)

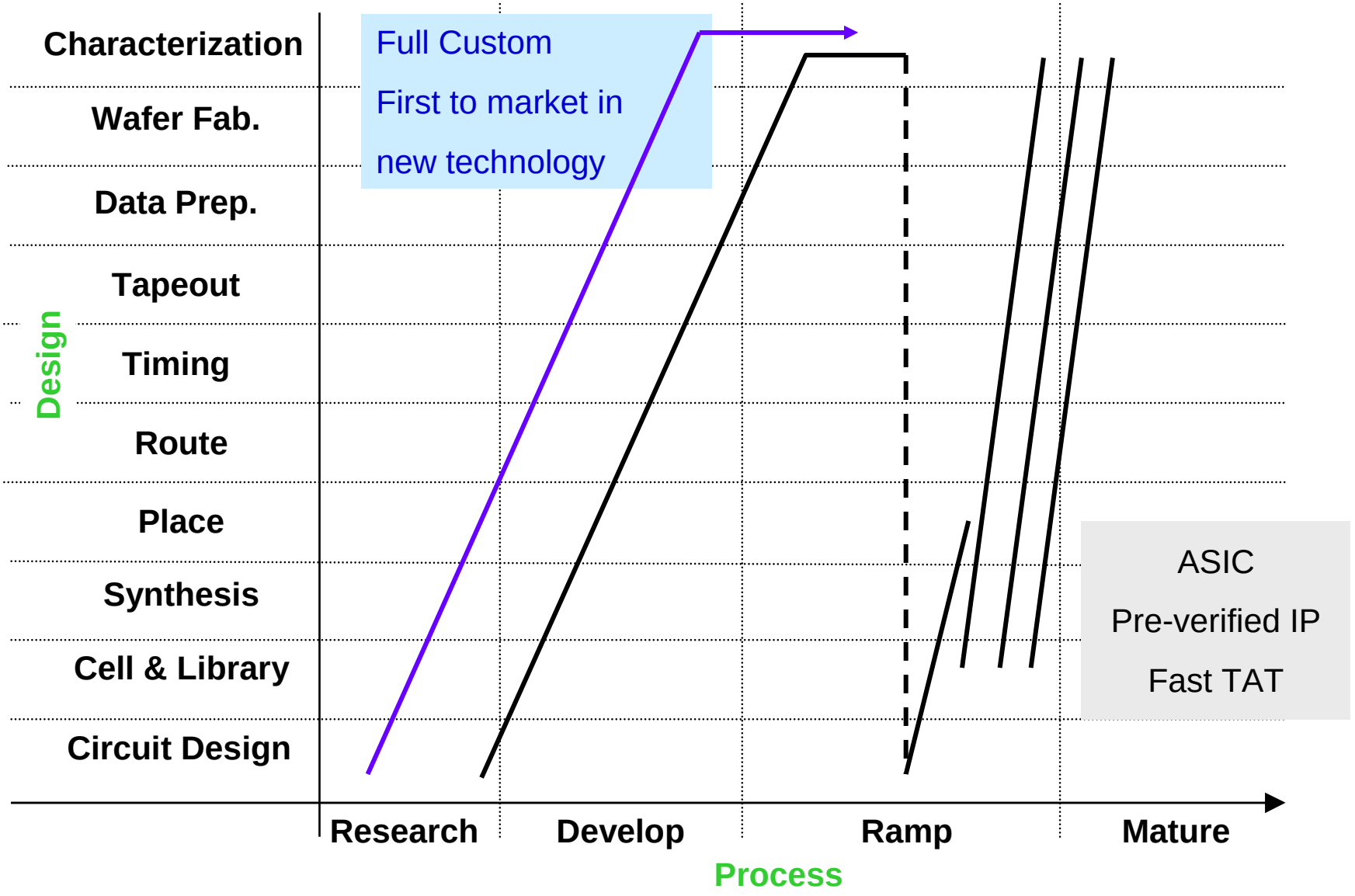
- A **restriction *[ ]*** is a specific type of rule which defines a finite (and generally absolute) boundary defined for a type of process or function
- **Corrollary**
  - Everything that is not explicitly forbidden is still allowed
- **RDRs help**
  - **Bring design rules back to a more manageable number**
  - **Every design rule needs to be verified in its complex and unpredictable worst case scenario**
  - **What DFM information needs to flow across the line ?**

Design Proces Information Plane

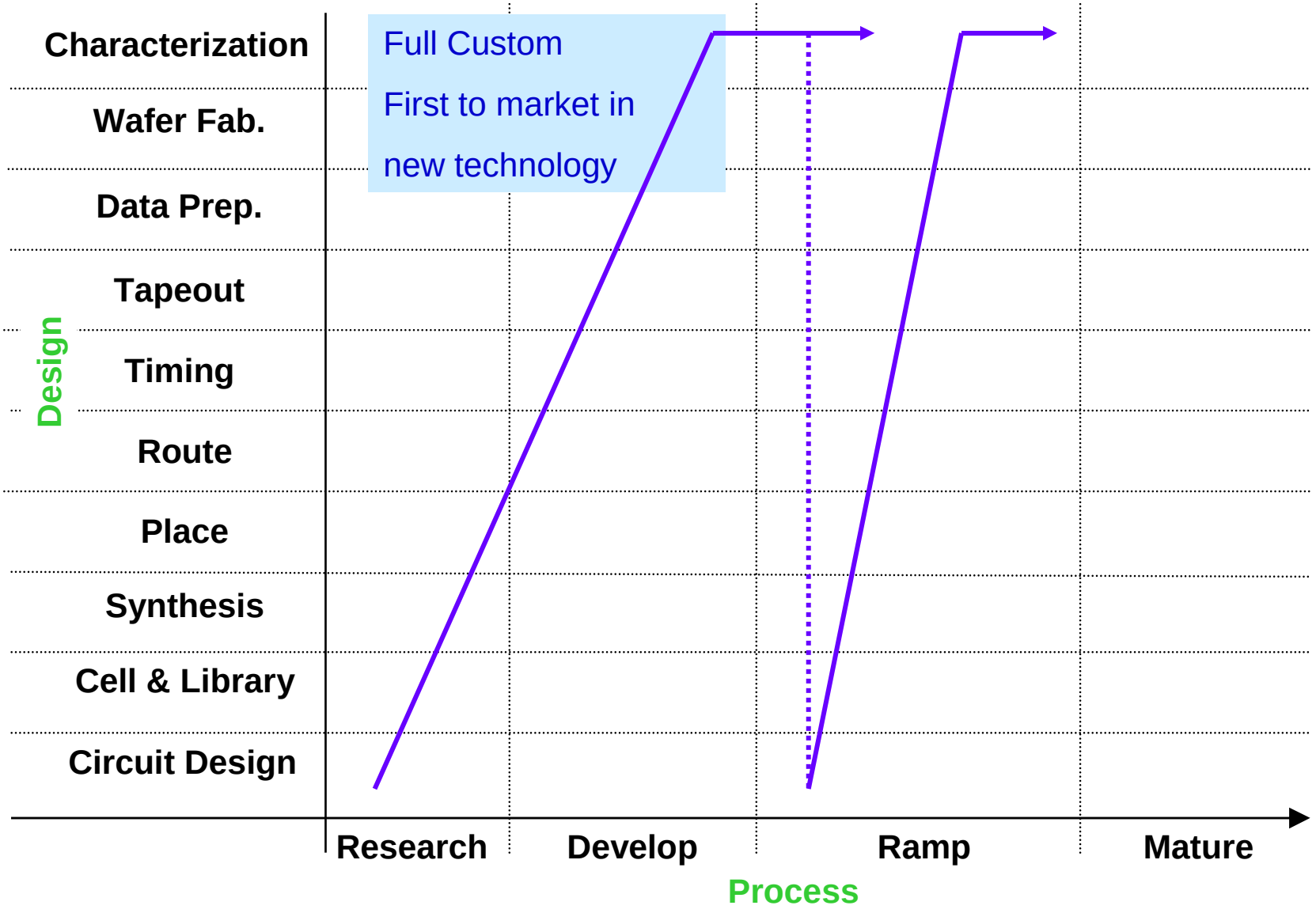


[Liebmann]

Design Proces Information Plane



Design Proces Information Plane



Where does this get us?

- **Many efforts focused on feeding DFM information back to the designer**
  - For the ones who care, it is too unreliable to act
  - For the others, they don't have the time in their design process to deal with it
- **Other efforts focus on feeding DFM information forward in the process**
  - What is critical, what is not, what not too touch ?
  - Optimizations can only operate using very large guard-bands

Prescriptive Methodology

- **What does the designer care about ?**
  - A set of rules that give her
    - The ability to design meaningful circuits at competitive size with high productivity
    - Predictable electrical (power, timing) properties
    - Manufacturable with acceptable yield

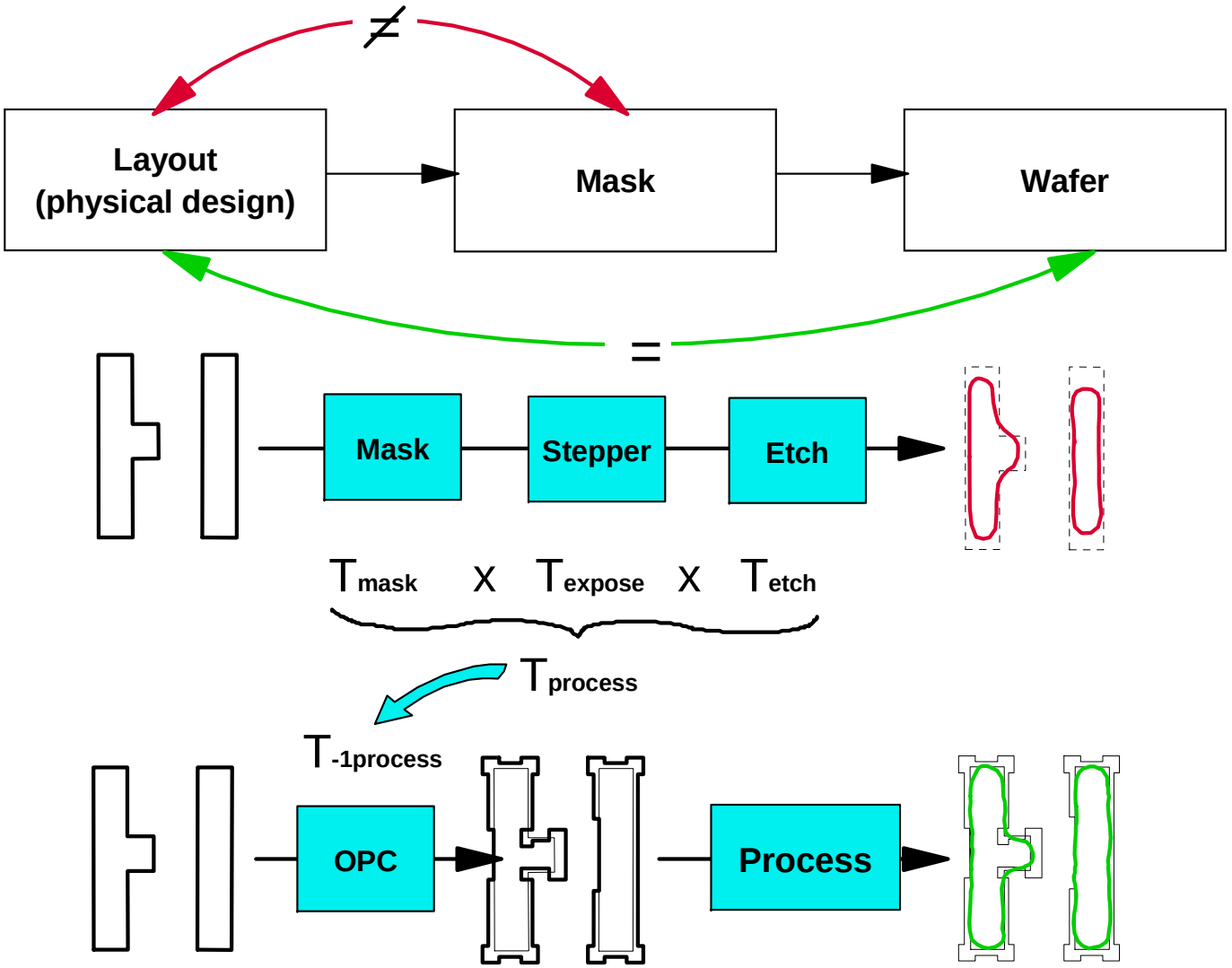
- **Can we give her a Prescriptive CAD methodology ?**
  - Where we have a methodology and set of rules that allow the designer to prescribe what he wants
  - A downstream ‘elaboration’ process that will meet this prescription in conjunction with a specific manufacturing process

Prescription

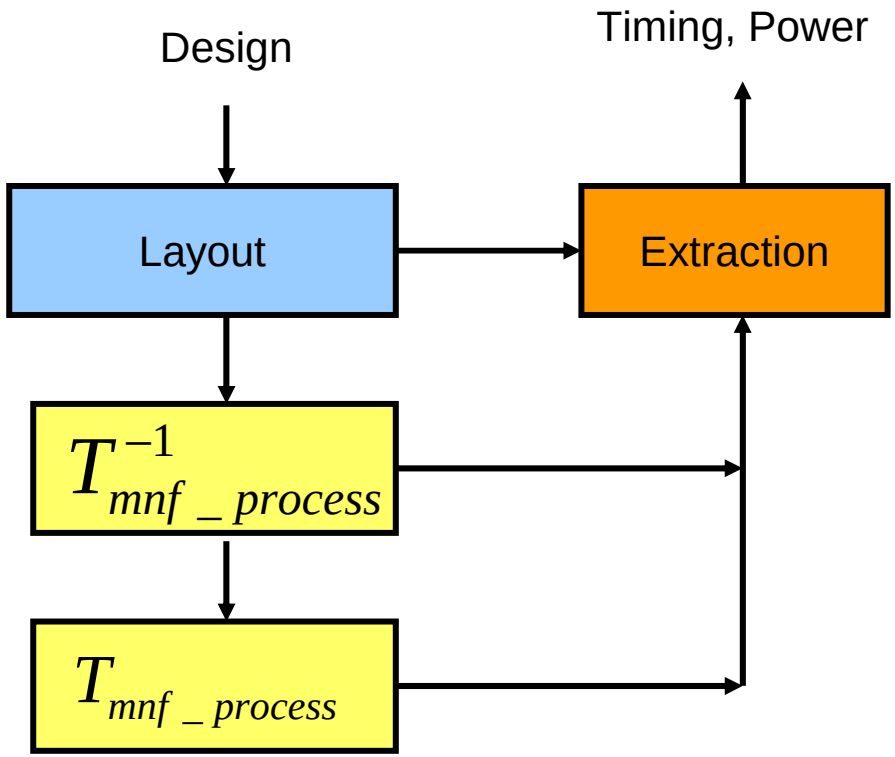
- **pre·scrip·tion**
  - 2. an act of prescribing.

- **pre·scribe**
  - –verb (used with object) 1.to lay down, in writing or otherwise, as a rule or a course of action to be followed; appoint, ordain, or enjoin.

Optical Proximity Correction

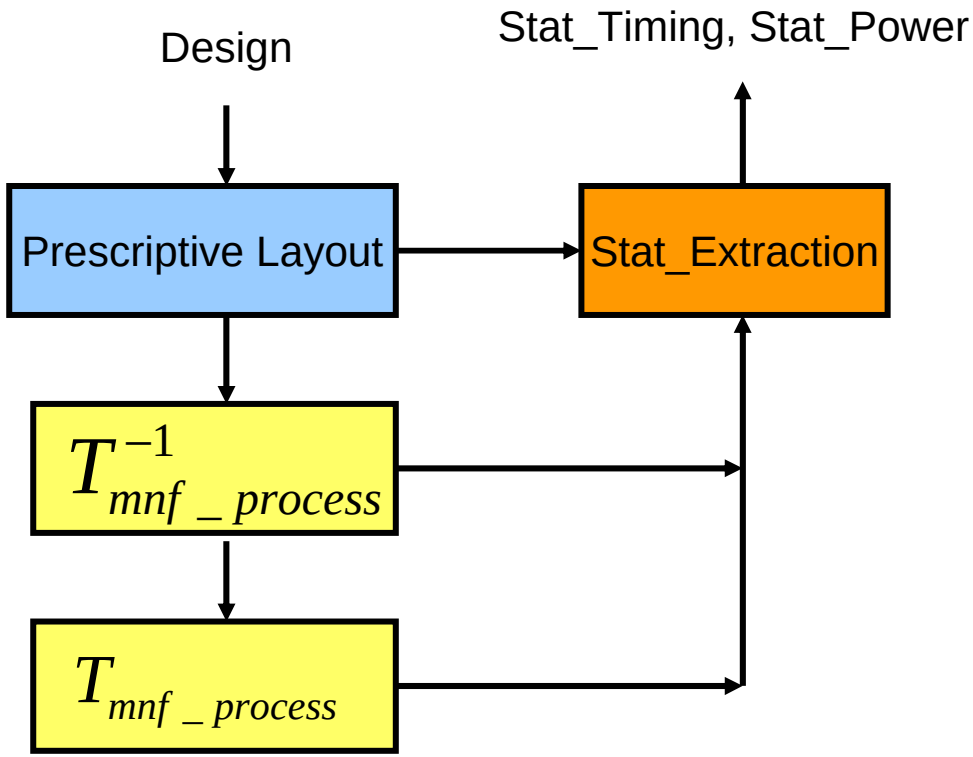


Prescriptive Design



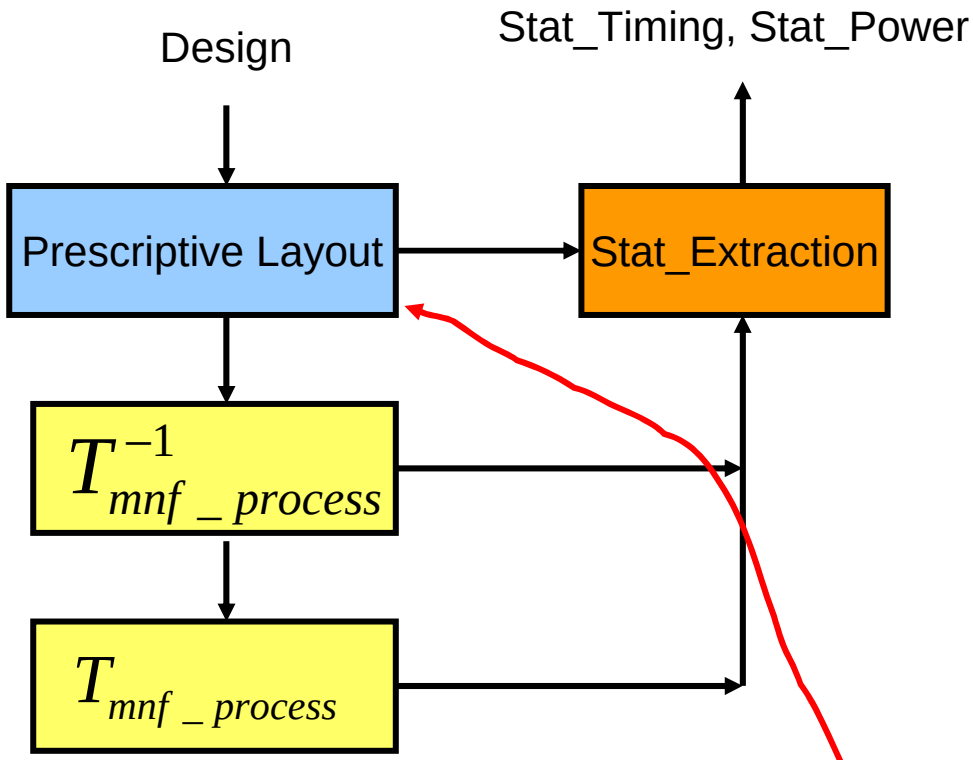
$$\text{Timing}(\text{Extraction}(layout)) = \text{Timing}(\text{T}_{\text{mnf\_process}}(T^{-1}_{mnf\_process}(layout)))$$

Prescriptive Design



$$\text{Stat\_Timing}(\text{Stat\_Extraction}(layout)) = \text{Stat\_Timing}(\text{T}_{\text{mnf\_process}}(T^{-1}_{mnf\_process}(layout)))$$

Prescriptive Design

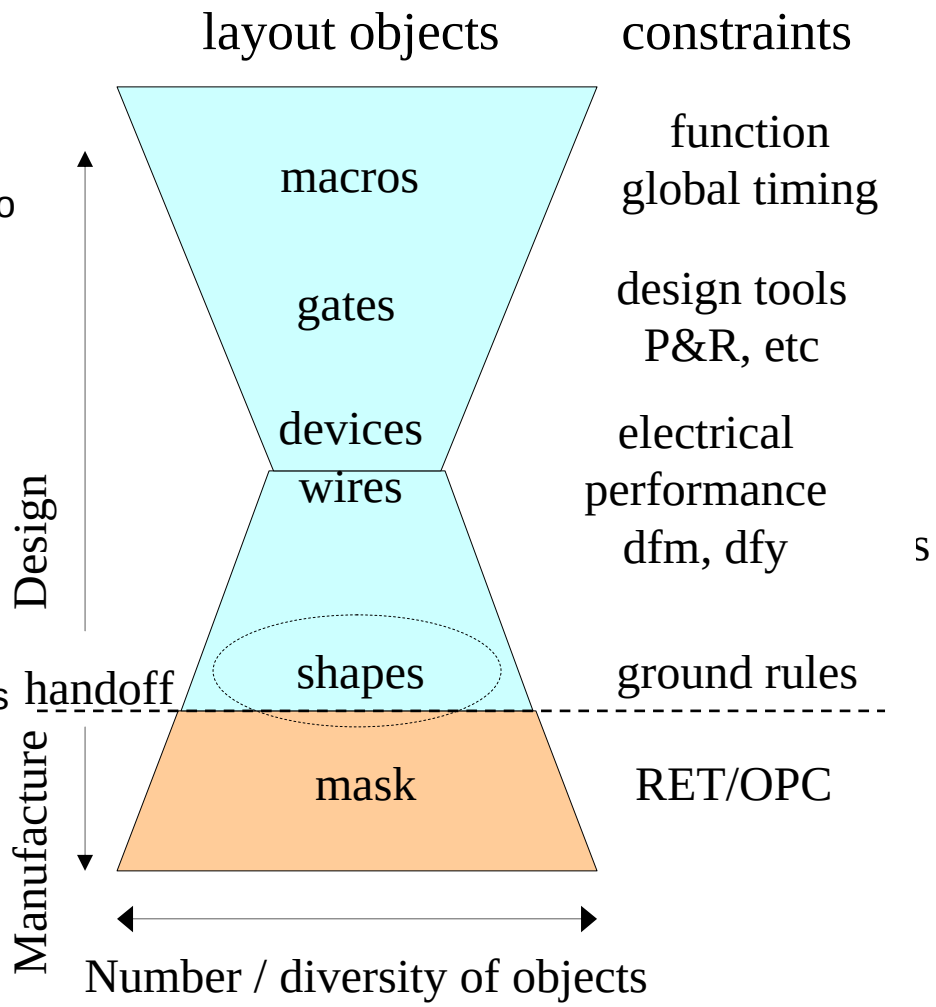


$$\text{Stat\_Timing}(\text{Stat\_Extraction}(layout)) = \text{Stat\_Timing}(\text{T}_{\text{mnf\_process}}(T^{-1}_{mnf\_process}(layout)))$$

Design Variability = f (Process Variability x Layout Variability)

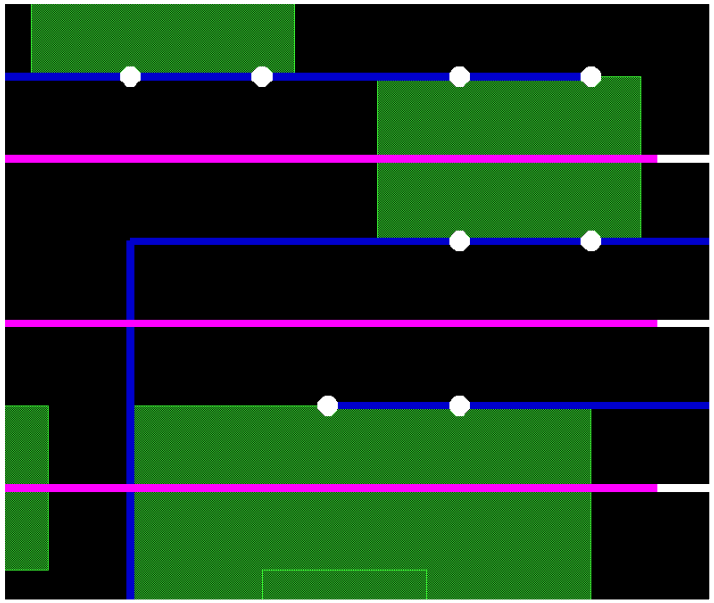
L3GO methodology

- **How?**
  - Introduce L3GO glyph-based representation to visualize designer intent
  - Use elaboration to retain flexibility for technology to select appropriate solutions
  - Use simpler representation to facilitate deeper modeling and improve technology definition and automation
- **Opportunity**
  - Designers are currently asked to overspecify design concerns by giving detailed edges (essentially doing some manufacturing work)
  - Added detail clouds the actual intent, and removes flexibility in technology options
  - Removing detail simplifies the specification between design and technology to the benefit of both.



L3GO elaboration

L3GO glyphs

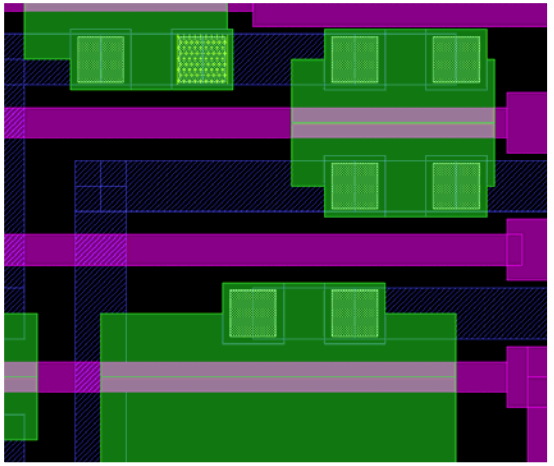


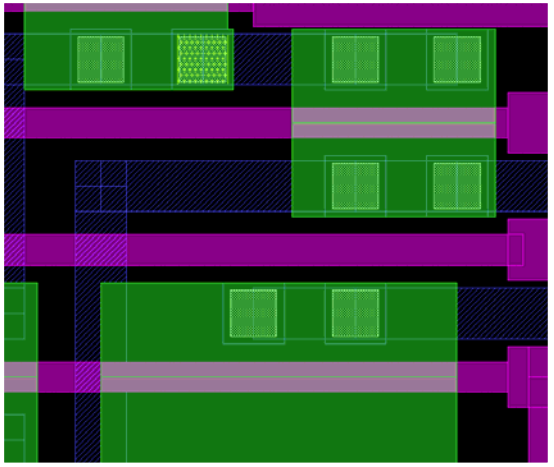
Elaboration

Rule Set 1

Rule Set 2

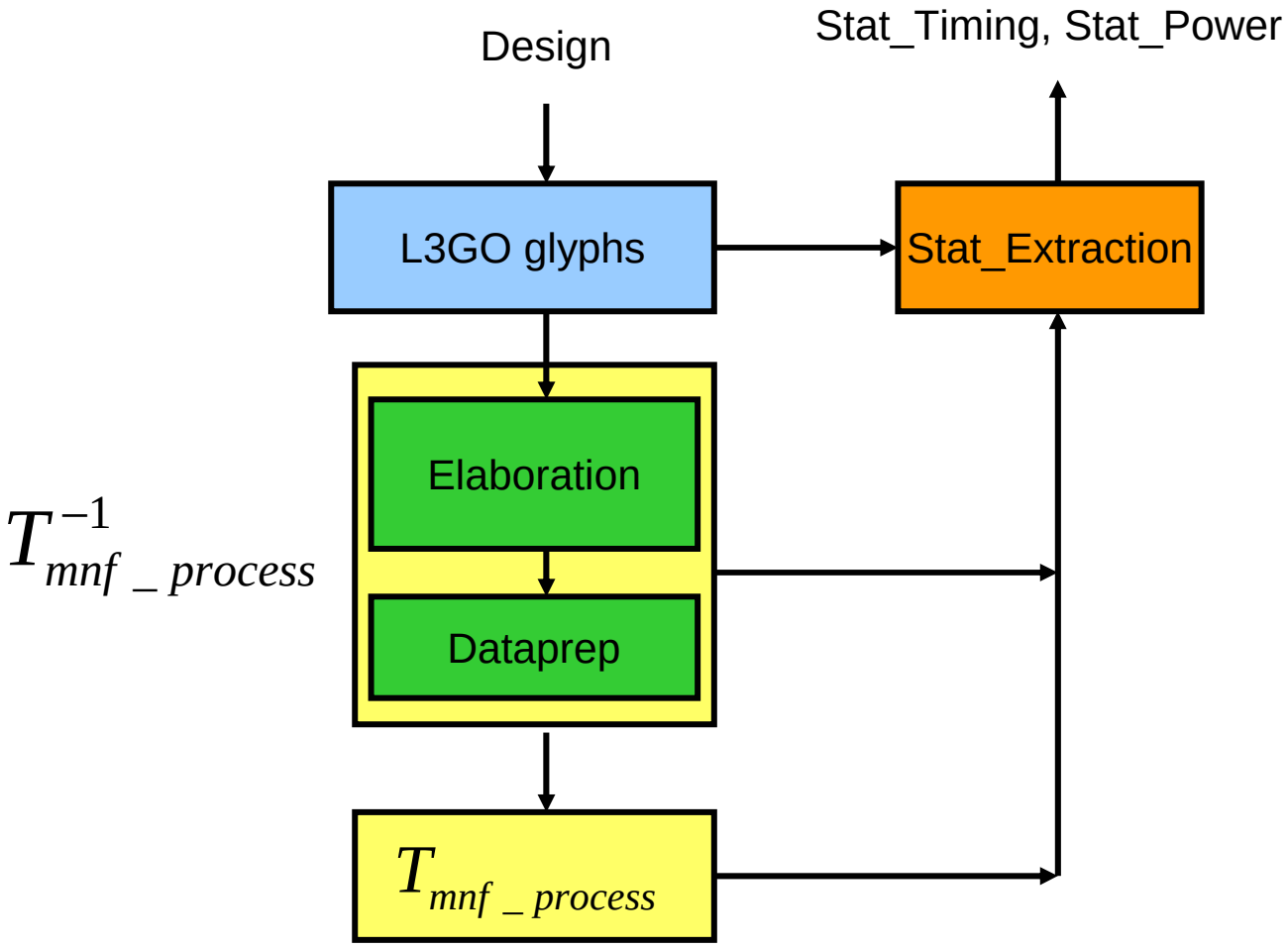
ground rule clean shapes



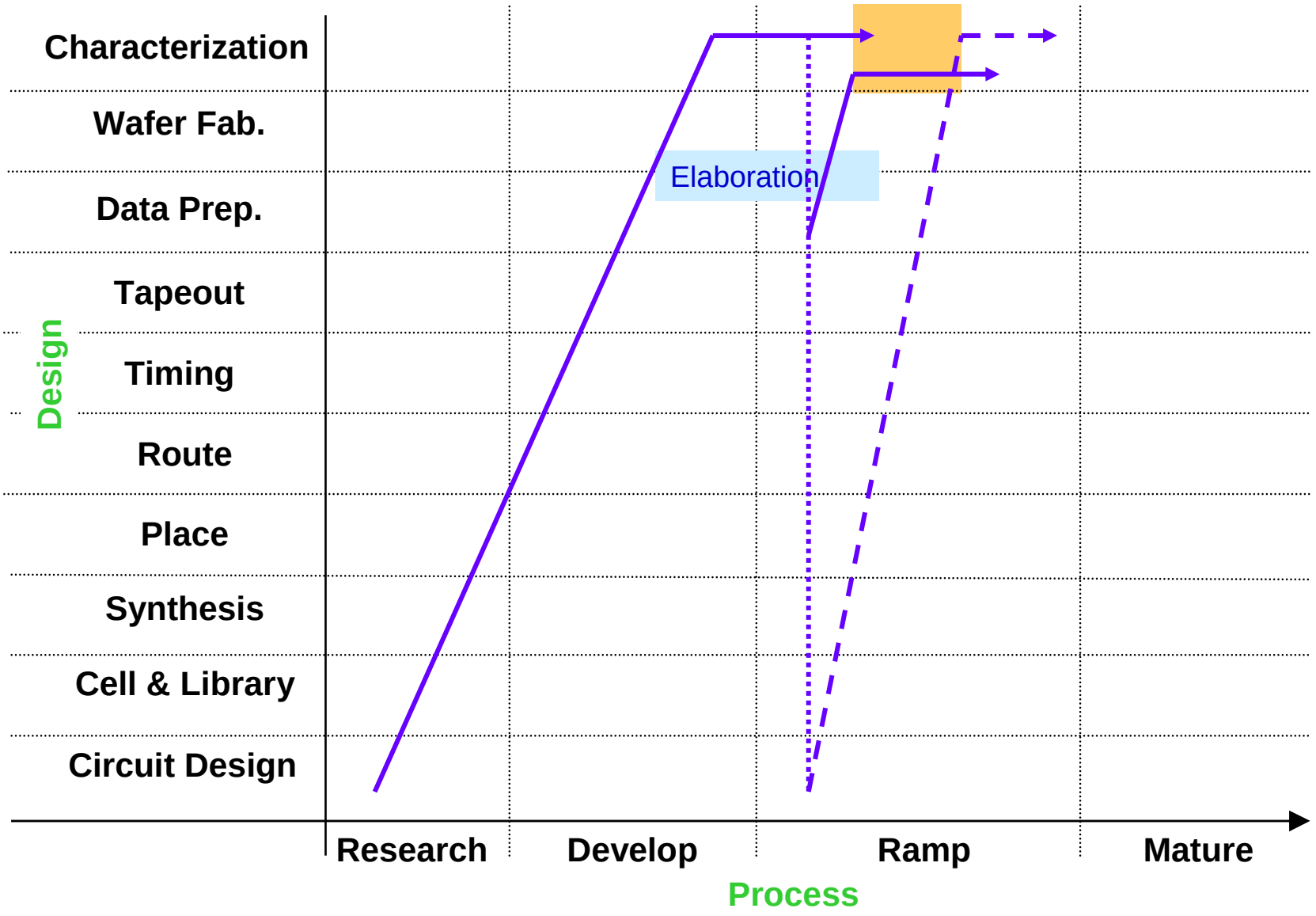


- L3GO abstracts technology details so designers can focus on electrical performance
- **Most technology churn handled by tools.**
- **Elaboration execution time ~= DRC at macro level**
- **Retargeting to new technology, partners, eased via tools.**
- **DFM tweaks with reduced effort.**

L3GO Process



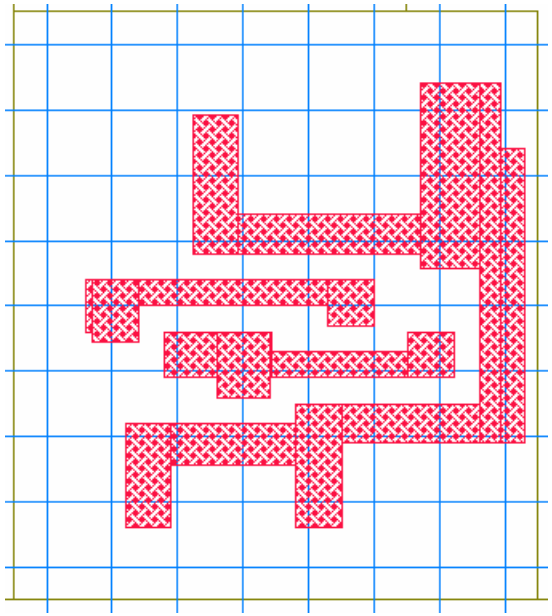
Design Proces Information Plane

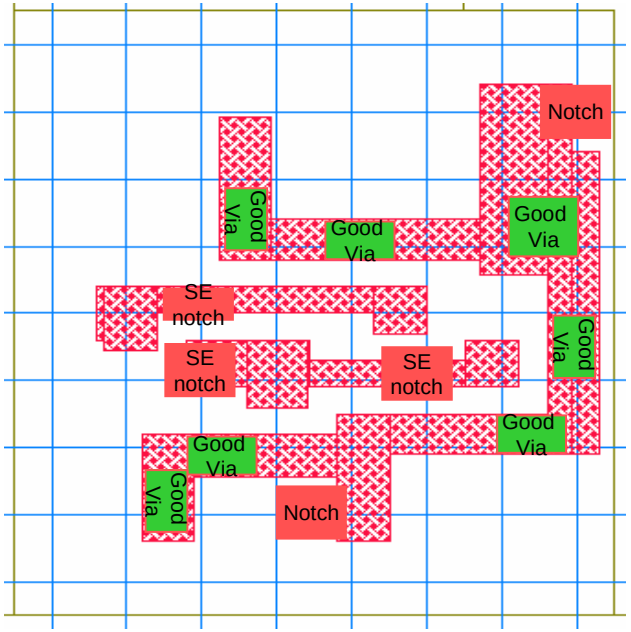


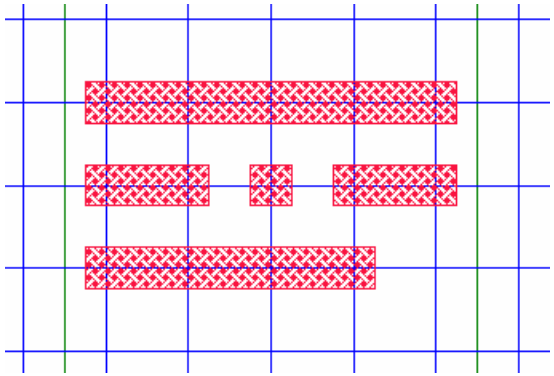
Standard Cell (ASICs, ASSPs)

- **Market**
  - Wants to put 10's millions of cells on a design in a few weeks Turn-Around time?
- **Corrolary**
  - No DFM effect can be exposed outside the "pre-verified" blocks.
  - Need prescriptive routing approach that allows for final "elaboration" and takes DFM effect out of design loop.

Cell / Block Design







Legal Via 

Illegal Via 

Problems:

- Off grid pins
- Many more pin shapes
- Fragmented pin shape allows few legal via positions

Spectrum of design implementations

Markets

Design Problems solved

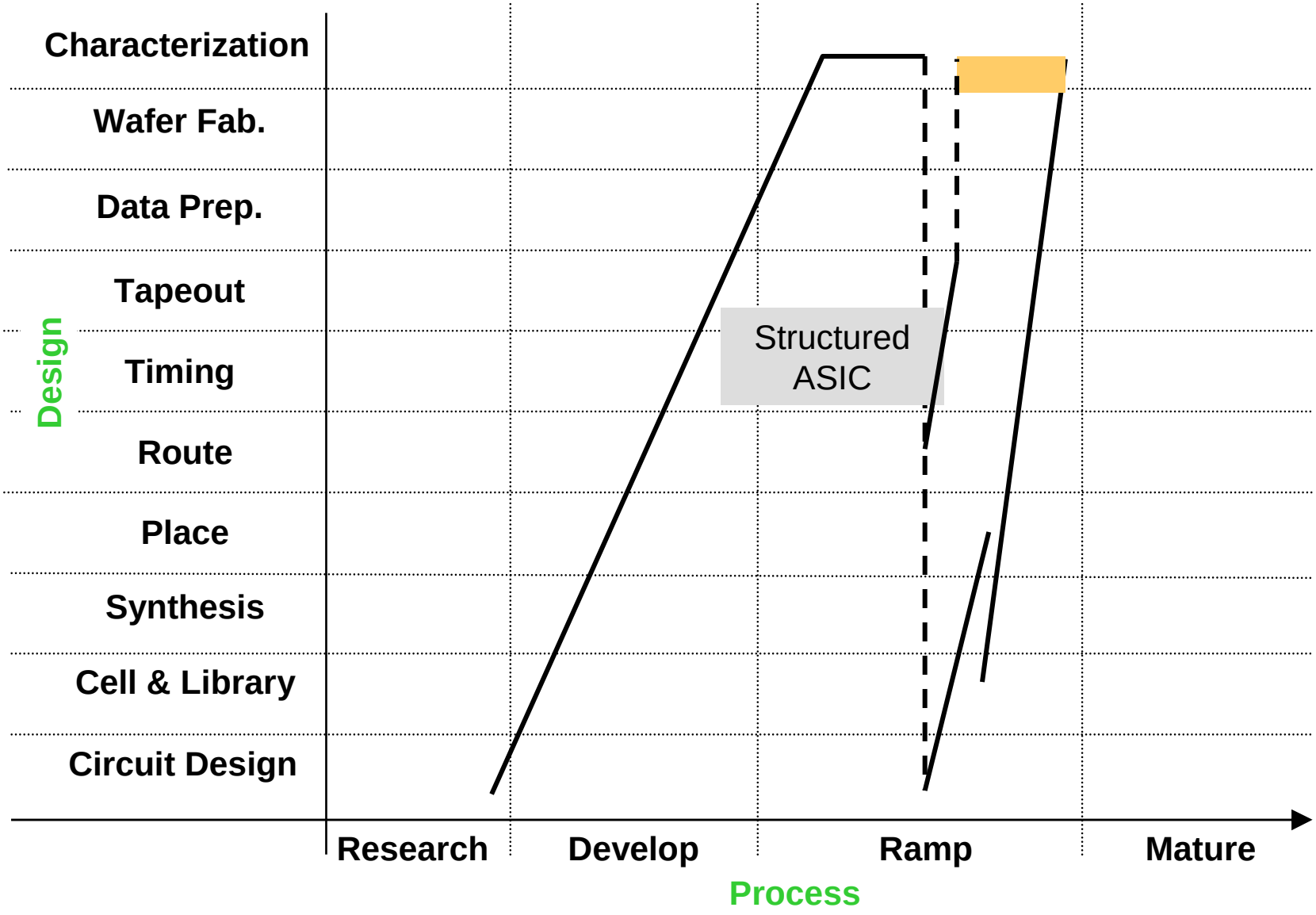
- *Routing*
- *Powergrid*
- *Test*
- *Clock*
- *Signal Integrity*
- *DFM*

Manuf. Problems solved

Two /three metal via layers

Fab Time

Design Proces Information Plane



Spectrum of design implementations

Structured ASICS

Structured (Prescriptive) CAD

Markets

Design Problems solved

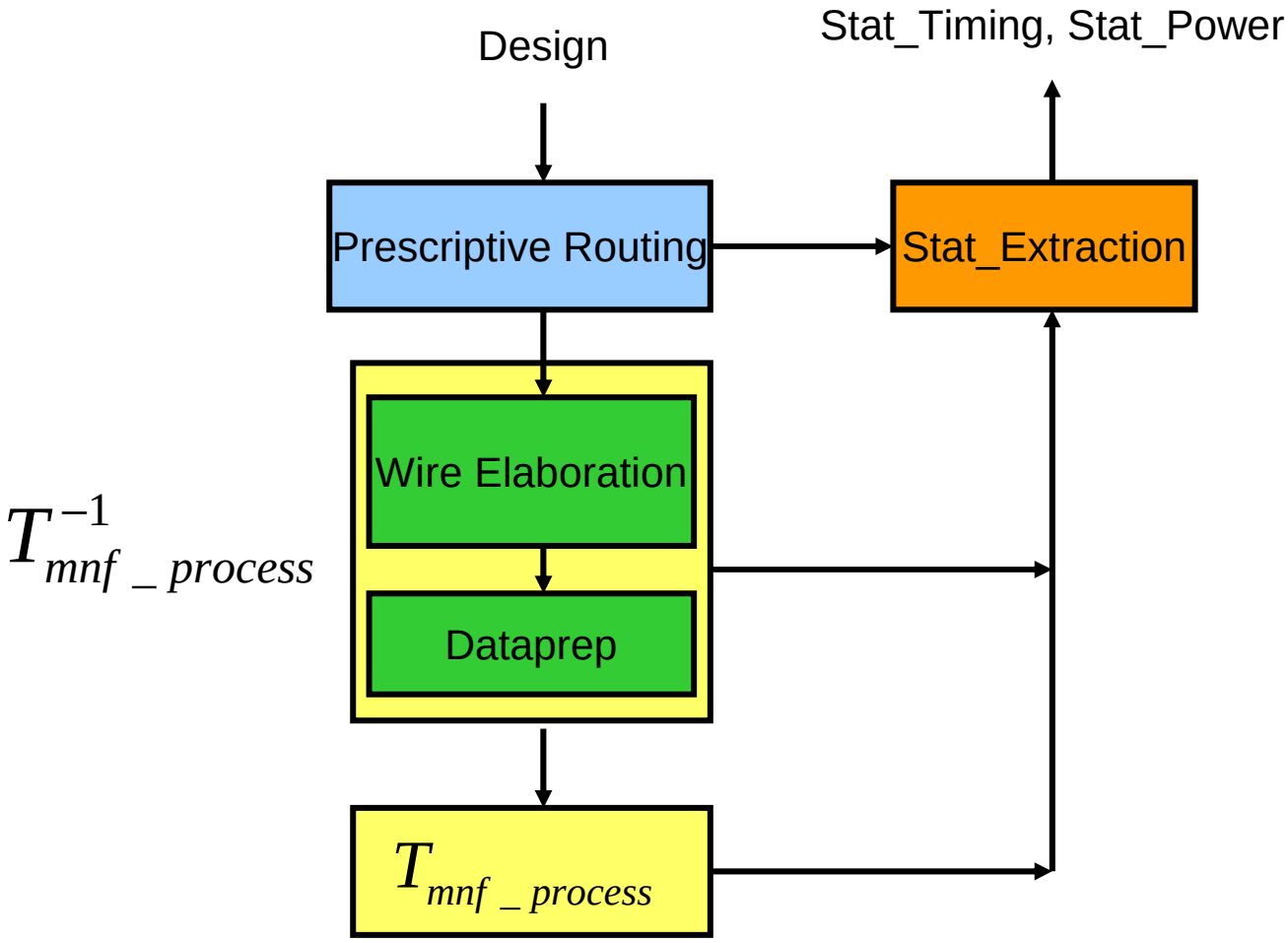
- *Routing*
- *Powergrid*
- *Test*
- *Clock*
- *Signal Integrity*
- *DFM*

Manuf. Problems solved

Two /three metal via layers

Fab Time

Prescriptive Routing



Conclusions

- **Feeding DFM information back to the designer**
  - Too unreliable in early process nodes
  - Too much impact on TAT in more mature processes
- **Feeding DFM information forward in the process**
  - Optimizations can only operate using very large guard-bands

- **Can we get to a Presciptive CAD methodology ?**
  - Where we have a methodology and set of rules that allow us to prescribe what we want
  - A downstream ‘elaboration’ process that will meet this prescription in conjunction with a specific manufacturing process