SOC Design Needs a System Level View

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ABSTRACT

Multicore, multi-processing, multi-threading are all terms that have gained a lot of popularity in the electronics industry in the last few years. Multi-processing and multi-threading are quite well understood in limited contexts within the hardware and software domains. However as with everything else, depending on the context in which these terms are used, they can refer to multiple processing elements on a single chip that are used in the server environment such as the processors from Sun, Intel and AMD or they can refer to SoC devices that operate within a different constraint set. Ultimately, the success or failure of multi-core environments, depend on the design tools and software that surround them. The cost of building an SoC platform has anecdotally been put at $ 1 billion USD. Given this failure is not an option and often times it is the failure of the software that causes the platform to fail. Software most often has failed because designers have forgotten that an SoC is truly a system, both hardware and software and trying to develop these in isolation causes lots of problems especially at the system integration stage. For this reason if not any other, it is necessary to take a System level view of the architecture to solve at least some of the many high level design and manufacturing challenges that have been identified in the latest ITRS roadmap.

The position that this presentation takes is that taking a system level view of SoC design helps to significantly cut verification and validation time while allowing the designer to optimize the power advantages that multi-core design enables. Programmability however is a different issue. The efficiency of multi-core systems lies in their parallelization of sequential tasks. However, parallel programming while a well understood programming discipline in specific applications is not widely used outside of those applications. Given the two major challenges of power and programmability are we ready for the next generation of SoCs?