Blockage Oriented Placement

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Abstract

With the increasing of the size and sophistication of the circuits, and in the presence of the blockage, the old standard-cell oriented placement methods are not working properly. There is a need to consider blockage effect early in the design flow along with standard cells for wirelength minimization purposes. A new wirelength estimation method, having blockage into consideration, is needed to be used in the design flow of large-scale circuits. Using this method, gives us some guidelines where in the chip area to put the blockages. Up to now, wirelength estimation methods either did not consider blockage or estimated wirelength in a flat framework in the presence of blockage which does not work properly for large-scale circuits. Also, for standard cells placement inside the chip area, considering standard cells and their connections are not working any more. We need to consider the effects of blockages parameters such as their place, aspect ratio and area.

In this paper, we propose a methodology for hierarchical derivation of wirelength estimation in the presence of blockage. Our experiments show that the proposed method is well-correlated with the real wirelength in the presence of blockage. By accurately estimating the wirelength, we can get some guidelines to determine area, aspect ratio and displacement from the center of the blockage. In order to minimize wirelength for mixed-size benchmarks, we introduce another step, namely placement planning into the placement flow right before doing placement for standard cells. This step denotes how to determine good boxes based on some measures to place standard cells inside them.

Keywords: Large-scale circuits, Blockage, Hierarchical placement, Wirelength Estimation, Placement Planning

1 Introduction

Since clock frequency, power consumption, and chip size are largely affected by interconnect lengths, total wirelength is frequently used as a measure of quality of the placement [1]. On the other hand, to achieve more efficient design, the computer aided design (CAD) flow is experiencing the trend of combining front end floor-planning and physical placement. In this process a fast and yet accurate estimation of total wirelength is critical.

Early work on total wirelength is based upon an empirical model known as Rent's Rule [3]. Rent's Rule correlates the number of signal input and output terminals T, to the number of gates C, in a random logic network as $T = AC^p$, where A is often called Rent Coefficient, which is the average number of pins per cell. The Rent Exponent P is the feature parameter of the circuit.

Using the Rent's Rule, the first work on wirelength estimation is done by Landman and Russo [5] which later has been improved by Donath [1]. More recent work improves the estimation by considering non-uniform probability [6][8].

Most of the research done on wirelength estimation is based on regularly placed circuits such as standard cell designs. With the trend toward IP-block-based design, macro cells as blockage (sometimes referred to as obstacle), is more likely to be present in the circuit. The presence of the blockage may significantly increase wire lengths and cause congestion [2]. Since the presence of the blockage makes the traditional wirelength estimations far from reality, new methods should be derived to address the problem of wirelength estimation. The first work on wirelength estimation in the presence of obstacle has been done by Cheng et. al. [2, 4]. In that work, the authors identified two distinct effects of obstacles on interconnection length: (1) changes due to the redistribution of interconnect terminals and (2) detours that have to be made around the obstacles. Theoretical expressions of both effects for two-terminal nets with a single obstacle have been derived. Their work, however, lack from having a hierarchical view to the placement problem and hence the average wirelength obtained form this method overestimates the actual wirelength, especially for min-cut placement approaches which are based on hierarchical partitioning.

In the first part of the current paper, starting from Donath's method [1], his approach is extended to be able to consider obstacle in the placement area. It is shown that how to derive a closed form expression for the total wirelength in the presence of obstacles. Simulation results on the medium and large circuits confirm that, in the presence of obstacle, this methodology is very suitable to estimate the wirelength. It provides us some guidelines to determine best area, location and aspect ratio of the blockage based on the requirements of the chip.

One method for design management is floorplanning. Many floorplanning and placement methods have been introduced in the past decade, which assume a fixed netlist consisting of pre-define modules; they try to minimize cost functions, such as area and wirelength. Furthermore, some recent work on

floorplanning tries to place macro blocks of various size simultaneously with small standard cells.

In the second part of this paper, in order to minimize wirelength for mixed-size benchmarks, we introduce another step, namely placement planning into the placement flow right before doing placement for standard cells. This step denotes how to determine good boxes based on some measures to place standard cells inside them. This method provides us some guidelines of the best location to place standard cells when the blockage and its parameters are fixed.

2 Wirelength Estimation considering Blockage

Our methodology to estimate the average wirelength is based on a top-down hierarchical placement of the circuit into a square Manhattan grid in the presence of a single blockage. The circuit is partitioned hierarchically into four sub-circuits. This hierarchical partitioning is continued till the number of standard cells in each of them is equal or less than a predefined constant.

At each level of hierarchy, we deduce the average number n_l of interconnections and the average length r_l of interconnections between each two sub-circuit belonging to the same $(l+1)$ level of hierarchy, but different l level of hierarchy [1].

2.1 Estimated Total Wirelength

Given the above model for the circuit, the feature parameter of the circuit P which is given by Rent's rule, and our placement scheme, we want to estimate the total interconnection length of the circuit. We do this by calculating the average number of interconnections n_h and the average length of the interconnections L_h at every hierarchical level h. The total interconnection length over all hierarchical levels is then obtained from

$$L_{tot} = \sum_{h=0}^{H} n_h L_h \qquad (1)$$

where the average number of interconnections n_h equals to (2) as derived in [1], where P is the Rent exponent of the circuit, C is the total number of cells, A is the average number of terminals per cell and α models the presence of multi-terminal nets and is between 0.5 and 1.

$$n_h = \alpha AC(1-4^{P-1})4^{L(P-1)} \qquad (2)$$

In the presence of the obstacles, the transparent-block wirelength is defined as the wirelength when the obstacle is assumed to be transparent and wires can pass through it. Detour wirelength, is the detour length needed in a routing wire in the presence of obstacles. To obtain the average wirelength, the wirelength is decomposed into three parts, namely transparent-block and detour in X and Y direction such that

$$\overline{L} = \overline{L}_{TB} + \overline{L}_{DT}^{h} + \overline{L}_{DT}^{v} \qquad (3)$$

where $\overline{L}_{DT}^{h}$ and $\overline{L}_{DT}^{v}$ are the average detour in X and Y direction and $\overline{L}_{TB}$ is the average transparent-block wirelength.

In the following, it is shown how to derive expressions for calculating average inter-bin wirelength in the presence of an obstacle for horizontally and diagonally adjacent bins. The case of vertically adjacent bins is similar to horizontally adjacent bins and so omitted from this discussion for brevity.

2.2 Horizontally Adjacent Bins

Horizontally adjacent bins are shown in Figure 1. *N* is the width and *M* is the height of the bins. *a* and *b* show the center of the blockage corresponding to the bottom left corner of the left bin.

In this case, the average transparent-block wirelength can be obtained as

$$\overline{L}_{TB\text{inter}} = \frac{\psi(2N,M,W,H,a,b) - \psi(N,M,W_1,H,a_1,b_1) - \psi(N,M,W_2,H,a_2,b_2)}{(MN-W_1H)(MN-W_2H)} \qquad (4)$$

where W=*W1+W2, b1=b2=b, a1=a-W/2+W1/2,* and *a2=W2/2* and ψ is

$$\psi(N,M,W,H,a,b)=\int\int\int\int_{P_1,P_2\in A-S}\left(|x_1-x_2|+|y_1-y_2|\right)dx_1dx_2dy_1dy_2=\frac{1}{6}(2N^2M^2(N+M)+2W^2H^2(H+W)-$$
$$6NMHW(N+M-2(a+b))-HW(MW^2+NH^2)-12HW(Ma^2+Nb^2)) \quad (5)$$

Basically, ψ is the total Manhattan distance between every two terminal in the non-blocked area, with the assumption that the probability distribution of the terminals is uniform.

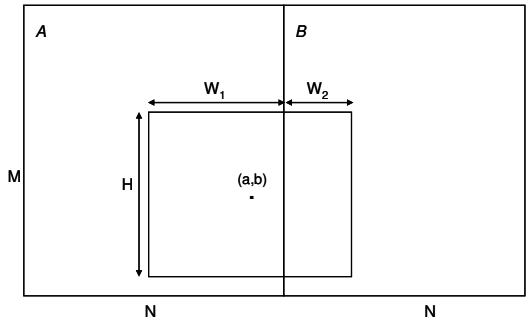

Figure 1: Two horizontal adjacent bins

Formula (4) is the total Manhattan distance between every two terminals which one of them is in the right bin and the other in the left bin. This formula can be obtained by subtracting the case where both of them are either in the left or in the right bins from the case where both of the terminals are in both left and right bins. The average detour wirelength in Y direction can be expressed as

$$\overline{L}^{v}_{DT,\text{inter}}=\Pr^{v}_{DT}.L^{v}_{DT,\text{inter}} \quad (6)$$

where $\Pr^{v}_{DT}$ is the probability of occurring a detour in Y direction, which can be expressed as

$$\Pr^{v}_{DT}=\frac{2H(N-a_1-W_2/2)H(a_1-W_1/2)}{(MN-W_1H)(MN-W_2H)} \quad (7)$$

$L^{v}_{DT,\text{inter}}$ is the average detour length in Y direction given that a detour occurred in this direction. The average detour wirelength in X direction can be found similarly.

Having had $\overline{L}_{TB}$, $\overline{L}^{h}_{DT}$ and $\overline{L}^{v}_{DT}$ the average wirelength of horizontal adjacent bins A and B, can be obtained form (3). Similar formula can be obtained for vertically adjacent bins A and C.

Obtaining the average inter-bin wirelength in the case of two diagonally adjacent bins is somewhat more similar and so omitted here.

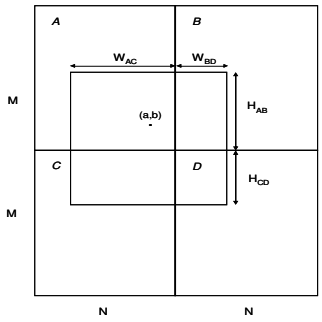

Figure 2: Bins A and D are diagonally and bins B and D are vertically adjacent.

Having had the average inter-bin wirelength for horizontally, vertically and diagonally adjacent bins, the average inter-bin wirelength can be obtained for every level of hierarchy h. For the top level of hierarchy, shown in Figure 2, the average inter-bin wirelength can be written as

$$\overline{L}_{\text{intra},H} = \frac{1}{6}(L^{h}_{\text{intra}}(A,B) + L^{h}_{\text{intra}}(C,D) + L^{v}_{\text{intra}}(A,C) + L^{h}_{\text{intra}}(B,D) + L^{d}_{\text{intra}}(A,D) + L^{d}_{\text{intra}}(B,C)) \qquad (9)$$

where $\overline{L}_{\text{intra},H}$ is the average wirelength in the top level of hierarchy. Moreover, h, v, and d, respectively, denote that the corresponding bins are horizontally, vertically, or diagonally adjacent.

2.4 Experimental Results

To measure the wirelength after the placement, we used Dragon placement tool [7] which is an academic placement tool, based on hierarchical min-cut partitioning approach. The actual wirelength of the circuit consists of two parts. The first part is the half perimeter wirelength (HPWL) obtained from the placement which is a good estimation of the transparent-block part of the actual wirelength, and the second part is the estimated detour wirelength. Basically, the actual wirelength is more than the HPWL and the difference occurs because of the detour wirelength. In order to compensate for this factor, we estimated the

detour of the circuit and added it up to the HPWL of the circuit. This will give us an estimation of the actual wirelength.

For performing the experiments, we considered one medium and two large circuits. In order to verify our theoretical results, on the real-world circuits, we picked Adaptec2 and Adaptec3 circuits from ISPD 2005 placement benchmark suite [9]. To adapt these two circuits to our experimental purpose, we kept the biggest blockage and changed all the other blockages to standard cells.

In the first set of experiments, position of the obstacle is changed, while its area and aspect ratio are kept constant. Table 1 shows the simulation results for this set of experiments.

Observation 1: As shown in Table 1, for our estimation method and actual WL, on average the wirelength is less when the blockage is in the center of the chip area.

In the second set of experiments, the obstacle is fixed at the center of the placement area and its area is kept constant, while its aspect ratio is changing. Figure 3 shows the simulation results for this set of experiments.

Circuit	Obstacle Position	Estimated WL	Actual WL
Test 3	Center	**2.03**	1.46
	Right Center	**2.46**	1.42
	Top Center	**2.31**	1.45
	Top Right Corner	**2.72**	1.48
Adaptec2	Center	**166.8**	121.34
	Right Center	**176.45**	125.54
	Top Center	**171.92**	131.43
	Top Right Corner	**181.78**	128.47
Adaptec3	Center	**266.67**	224.73
	Right Center	**278.56**	234.87
	Top Center	**289.34**	254.33
	Top Right Corner	**293.22**	268.32
Average Error (%)		**38.83**	0.0

Table 1: Total wirelength as a function of the obstacle displacement

Observation 2: As shown in figure 3, as we get further from aspect ratio 1 in both directions, the wirelength increases. This happens because when we

consider a square grid, both detour and transparent-block parts of the wirelength are symmetric functions of the summation of blockage's width and height. Since the product of blockage's width and height is constant, these functions get their extermum (i.e. minimum) when blockage's width and height is equal, which means that the aspect ratio is one.

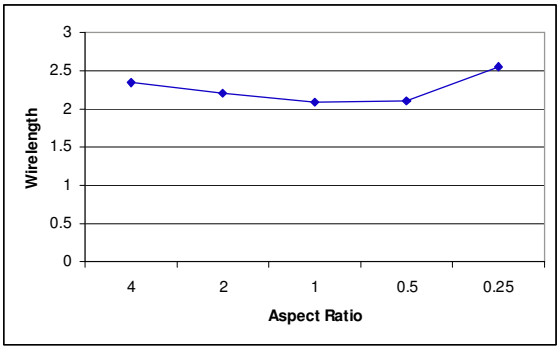

Figure 3. Total wirelength as a function of aspect ratio

In the third set of experiments, the obstacle is fixed at the center of the placement area and its aspect ratio is kept constant, while its area is changing. Table 2 shows the simulation results for this set of experiments.

Circuit	Area Ratio	Estimated WL	Actual WL
Test3	2.5%	**2.6**	1.41
	5.0%	**2.46**	1.42
	12.5%	**2.54**	1.55
Adaptec2	2.5%	**243.24**	198.67
	5.0%	**266.57**	224.73
	12.5%	**297.34**	263.23
Adaptec3	2.5%	**152.11**	118.21
	5.0%	**166.8**	121.01
	12.5%	**178.21**	132.12
Average Error (%)		**34.88**	0.0

Table 2: Total wirelength as a function of the blockage's area

Observation 3: The wirelength increases with the increase of blockage's area. This happens because the transparent-block part of wirelength formula is an increasing function of the blockage area.

3 Placement Planning

In order to minimize the wirelength for mixed-size benchmarks, placement planning is embedded into the placement flow right before doing placement for standard cells. This step denotes how to determine good boxes to place standard cells. The parameters that can be considered to determine a box are connectivity to the fixed I/Os, the utilization of the box, the existence of narrow slivers between the big macro cells, the blockage map inside the box, and the open area in the box.

3.1 Experimental Results

We have analyzed how the starting box for placing standard cells can affect the total wirelength by doing some experiments. We manually did some experiments on ISPD Placement benchmark suit. In order to determine good boxes for placing standard cells, we considered different boxes and did placement for standard cells on those boxes and chose the one which resulted in shortest wirelength. As illustrated in Table 3 the wirelength improvement after placement was about 4.4% on average. For the benchmark Adaptec2 this improvement was about 9%.

Circuit	WL with Placement Planning	WL without Placement Planning
Adaptec1	88.6	83.2
Adaptec2	104.5	95.1
Adaptec4	204.6	203.8
Bigblue1	106.4	103.3
Bigblue4	946.3	903.9

Table 3: Comparison between Dragon wirelength with and without applying placement planning. Bounding box wirelength is in meters.

In order to automatically choose a box the parameters to consider are utilization, box area, blockage map, and narrow slivers. The effect of each of these parameters needs to be analyzed based on exhaustive experiments.

The effects of some of these parameters are intuitively known. For example, the smaller the area of a box, the less the wirelength can be, since total

bounding box is smaller. On the other hand, boxes with lower utilization lead to less congested placement and result in better wirelength when annealing is performed. Therefore, for the boxes with the same area, the ones with less utilization are better. For the boxes with the same utilization, the ones with smaller area are better. The operators for generating different boxes are either changing the aspect ratio of the box or changing the box location by applying a displacement to its center.

The approach we proposed for automatically determining good boxes for placement planning is based on a divide-and-conquer methodology. The whole area of the chip is divided into equal size partitions and the best box is determined in each of the partitions based on the metrics we introduced. We considered box area, and box utilization, which are more known to us. We considered same weight for the effect of these two parameters. Then every four quadric-section partition is merged together and the best box for the whole group is picked based on the boxes for each of them. This process continues until all of the partitions are merged together. In the last step, the best box for the whole design is determined by combining the best boxes for the sub-partitions. Basically, we want to guide the whole process of placement planning to capture different characteristics of each partition and its effect on the location of the best box by using the divide and conquer approach.

The approach to merge two sub-partitions and pick a box for the whole group can either be deterministic or non-deterministic. Deterministic Approach is shown in figure 4. In this approach the best value for width, height, and the displacement of the center of box in terms of the defined cost function are chosen. Two partitions are merged together by refining their box and joining them either horizontally or vertically. If two partitions are merged horizontally, we have to shift their best boxes horizontally so that they become adjacent on the mutual vertical edge. Then the best box for the group contains the best boxes for each partition. The reverse applies when two partitions are merged vertically. The advantage of this method is that it is easy in terms of amount of computations. Its

drawback is that it may lead to bad result at the end, since good boxes for sub-partitions do not necessarily give good boxes for the whole group.

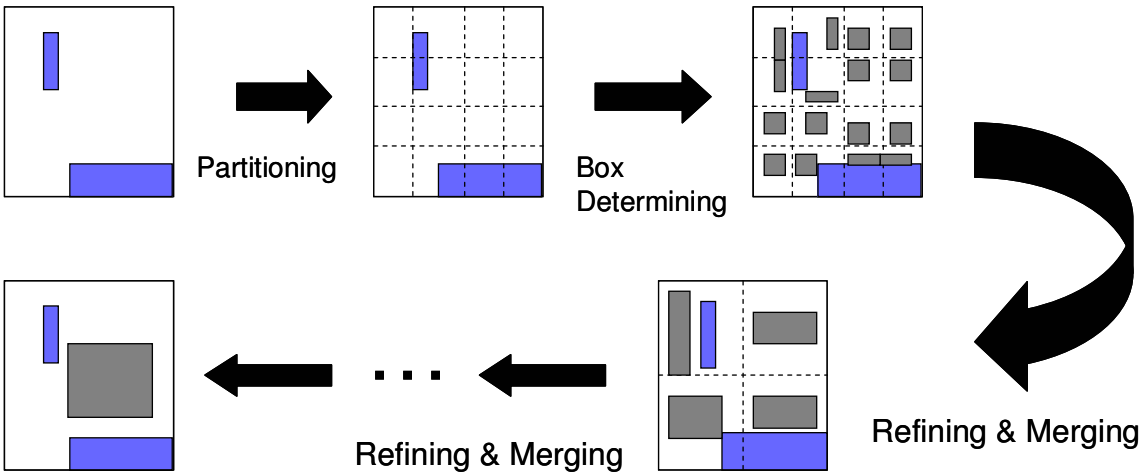

Figure 4: Deterministic Placement Planning

In order to improve this approach, a probability distribution is considered for each block. That means that for a specific area, we exploit a probability distribution for width and height of different boxes, according to the value of the cost function for each box. The probability distribution is in the form of

$$L_i = (w_{i1}, h_{i1}, p_{i1}), \ldots, (w_{im}, h_{im}, p_{im}), \sum_{j=1}^{m} p_{ij} = 1 \qquad (10)$$

The multiplication of each w_i and h_i is the same for each i and equals to the area of the box. A search space is considered for each partition. Each element in this search space represents a box, and its probability. Like the non-deterministic case, the boxes should get refined to merge each other. In order to combine boxes horizontally, the distribution of the width of the result box is the summation of the distribution of the width of two boxes, and the distribution for the height is the maximum of the distribution for the height of two boxes. The reverse holds for the combining boxes vertically.

4 Conclusions

In this paper we proposed a top-down hierarchical methodology for wirelength estimation in the presence of an obstacle. By changing the displacement, aspect ratio, and area of the blockage, their effects have been

studied on total wirelength of test circuits. These studies can be used in early design stages to provide guidelines for determining the location and/or aspect ratios of the IPs to achieve lower wirelength.

We also proposed the process of determining good boxes for placing standard cells in chip area considering blockage effect. We presented a method to do this task considering both the deterministic and statistical placement planning. For this purpose, a combined cost function and different coefficients to exploit effects of different parameters on the placement planning were considered.

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