Blockage Oriented Placement

Taraneh Taghavi
Majid Sarrafzadeh

Computer Science Department, UCLA
Email:{taghavi,majid}@cs.ucla.edu

Motivation

- Placement cannot be blind to obstacles.
- Wirelength estimation methods considering blockage is needed early in design cycle
  - Provides us guidelines to place macro cells.
- Placement should consider obstacle effect for placing standard cells
  - Obstacle parameters: aspect ratio, area, displacement

Background

- Wirelength estimation methods by now:
  - Hierarchical WL estimation, w/o blockage
  - Flat WL estimation, with blockage
- WL estimation method
  - Hierarchical wirelength estimation considering blockage based on Rent's rule
- Placement planning method
  - determine areas to place standard cells

Presentation Outline

- Hierarchical WL estimation method
  - Algorithm
  - Experimentation
  - Guidelines
- Placement planning
  - Algorithm
  - Simulation
- Conclusion

Previous Works

- Landman and Russo[1971], improved by Donath[1979]
- Stroobandt and Campenhout[1996],estimation improvement considering non uniform probability
- Cheng et.al.[2002], flat approach considering blockage
  - Redistribution
  - Detour

Methodology

- Circuit partitioned into four sub-circuit
- Each level of hierarchy:
  - Number of interconnections
  - Average length of interconnections b/w two sub-circuit of same (h+1), different h level
- Wirelength equals to:

$$L_{tot} = \sum_{h=0}^{H} n_h L_h$$

Average Number of Interconnection

- Rent rule for a sub-circuit of K cells:

  $T = AK^P$

- Total of C cells, divided into groups of K

  $T_{total}(K) = AK^P \frac{C}{K} = ACK^{P-1}$

- Number of interconnection among all circuits of size K: $N(K) = \alpha ACK^{P-1}$
- Average number of interconnections:

  $n_h = N(4^h) - N(4^{h+1})$

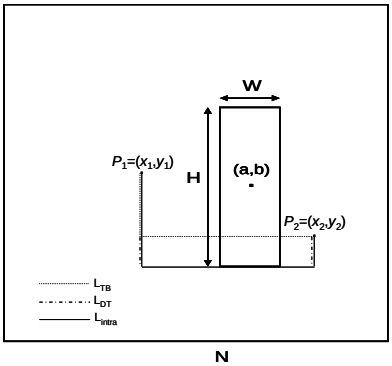
- By substitution we have:

  $n_h = \alpha AC(1-4^{P-1})4^{L(P-1)}$

Average Length of interconnection

- Transparent Block
  - wirelength when the obstacle is transparent
- Detour
  - detour length needed in presence of obstacle

$\overline{L} = \overline{L}_{TB} + \overline{L}^h_{DT} + \overline{L}^v_{DT}$



Average Intra-Bin WL

- No Obstacle:

$$\bar{L}_{\text{intra}} = \frac{\int_0^M \int_0^M \int_0^N \int_0^N \left(|x_1 - x_2| + |y_1 - y_2|\right) dx_1 dx_2 dy_1 dy_2}{\int_0^M \int_0^M \int_0^N \int_0^N dx_1 dx_2 dy_1 dy_2} = \frac{N+M}{3}$$

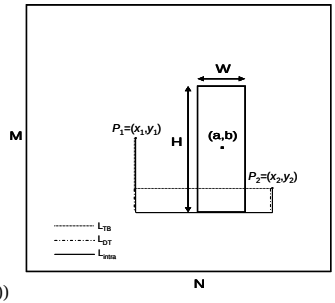
- Single Obstacle:

$$\bar{L}_{TB,\text{intra}} = \psi(N,M,W,H,a,b)/(NM - WH)^2$$

$$\psi(N,M,W,H,a,b) = \iiint\limits_{P_1,P_2 \in A-S} \left(|x_1 - x_2| + |y_1 - y_2|\right) dx_1 dx_2 dy_1 dy_2 =$$

$$\frac{1}{6}(2N^2M^2(N+M) + 2W^2H^2(H+W) -$$

$$6NMHW(N+M-2(a+b)) - \quad HW(MW^2 + NH^2) - 12HW(Ma^2 + Nb^2))$$



Average Inter-Bin WL

- Horizontally Adj.Bins
  - Transparent Block

$$\bar{L}_{TB,\text{inter}} = \frac{\psi(2N,M,W,H,a,b) - \psi(N,M,W_1,H,a_1,b_1) - \psi(N,M,W_2,H,a_2,b_2)}{(MN - W_1H)(MN - W_2H)}$$

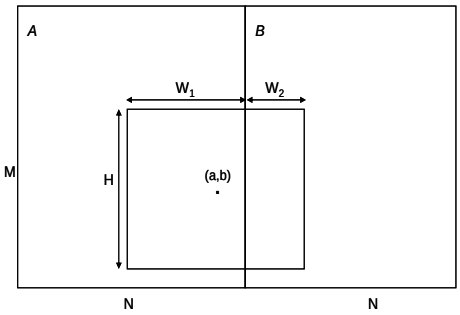
  - Detour, Vertically

$$\bar{L}^v_{DT,\text{inter}} = \text{Pr}^v_{DT} \cdot L^v_{DT,\text{inter}}$$

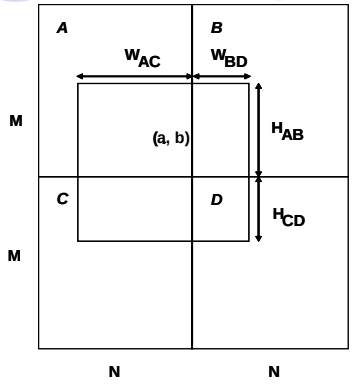
$$\text{Pr}^v_{DT} = \frac{2H(N - a_1 - W_2/2)H(a_1 - W_1/2)}{(MN - W_1H)(MN - W_2H)}$$

$$\bar{L}^v_{DT,\text{inter}} = \frac{1}{3}H\frac{2H(N - a_1 - W_2/2)H(a_1 - W_1/2)}{(MN - W_1H)(MN - W_2H)}$$

  - Detour, Horizontally is similar
- Vertically Adj. and Diagonally Adj. Bins is similar



Average Interconnection Length in Each Level of Hierarchy



$$\overline{L}_{\text{intr},H} = \frac{1}{6}(L^h_{\text{intr}}(A,B) + L^h_{\text{intr}}(C,D) + L^v_{\text{intr}}(A,C) + L^h_{\text{intr}}(B,D) + L^d_{\text{intr}}(A,D) + L^d_{\text{intr}}(B,C))$$

Experimental Setup

- Estimation of wirelength after the placement:
  - Integrate implementation on Dragon placement tool
- Actual wirelength consists of two parts
  - HPWL obtained from the placement
    - estimation of the transparent-block part of the actual wirelength
  - Estimated detour wirelength

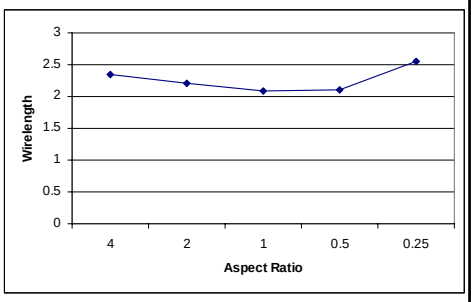
Simulation Result I: Total wirelength as a function of the obstacle displacement

Circuit	Obstacle Position	Estimated WL	Actual WL
Test 3	Center	**2.03**	1.46
	Right Center	**2.46**	1.42
	Top Center	**2.31**	1.45
	Top Right Corner	**2.72**	1.48
Adaptec2	Center	**166.8**	121.34
	Right Center	**176.45**	125.54
	Top Center	**171.92**	131.43
	Top Right Corner	**181.78**	128.47
Adaptec3	Center	**266.67**	224.73
	Right Center	**278.56**	234.87
	Top Center	**289.34**	254.33
	Top Right Corner	**293.22**	268.32
Average Error (%)		**38.83**	0.0

- Observation1:Minimum WL when blockage is in the center

Simulation Result II: Total wirelength as a function of the obstacle aspect ratio

- Observation2: Minimum WL when AR =1
  - WL increasing getting further from AR = 1 in both directions
  - WL is symmetric function of (width + height)



Simulation Result III: Total wirelength as a function of the obstacle area

- Observation3: WL increases with the increase of Blockage area

Circuit	Area Ratio	Estimated WL	Actual WL
Test3	2.5%	**2.6**	1.41
	5.0%	**2.46**	1.42
	12.5%	**2.54**	1.55
Adaptec2	2.5%	**243.24**	198.67
	5.0%	**266.57**	224.73
	12.5%	**297.34**	263.23
Adaptec3	2.5%	**152.11**	118.21
	5.0%	**166.8**	121.01
	12.5%	**178.21**	132.12
Average Error (%)		**34.88**	0.0

Presentation Outline

- Hierarchical WL estimation method
  - Algorithm
  - Experimentation
  - Guidelines
- Placement planning
  - Algorithm
  - Simulation
- Conclusion

Placement Planning

- Placement Planning embedded into the placement flow right before doing placement for standard cells
- Denotes how to determine good boxes to place standard cells

Experimental Result

- Manually consider different boxes
- placement for standard cells on those boxes
- chose the one which resulted in shortest wirelength
- wirelength improvement after placement was about 4.4% on average.
  - For Adaptec2 around 9%

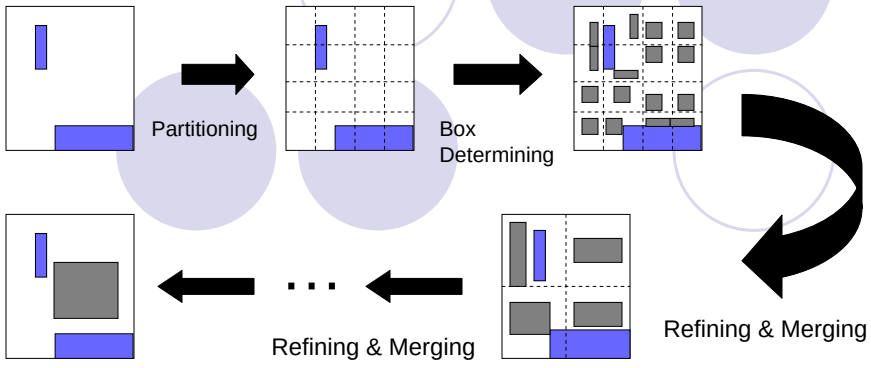
Circuit	WL with Placement Planning	WL without Placement Planning
Adaptec1	88.6	83.2
Adaptec2	104.5	95.1
Adaptec4	204.6	203.8
Bigblue1	106.4	103.3
Bigblue4	946.3	903.9

Placement Planning Automation

- Different parameters
  - Connectivity to the fixed I/Os
  - Utilization of the box
  - Effect of narrow slivers between the big macro cells
  - Blockage map inside the box
  - Open area in the box

Placement Planning Automation (Cont.)

- Deterministic Approach



Deterministic Vs. Non-Deterministic approaches

- Advantage
  - Easy to implement
- Drawback
  - Local improvement may not lead to global improvement
- Solution
  - Non-deterministic approach

Non-Deterministic Approach

- Considering Probability Distribution for each box
  - Specific area
  - Different probabilities for width and height of different boxes

$$L_i = (w_{i1}, h_{i1}, p_{i1}), \ldots, (w_{im}, h_{im}, p_{im}), \sum_{j=1}^{m} p_{ij} = 1$$

- Considering search space for each partition
- Refining like deterministic case
- Assigning probability distribution for merging

Presentation Outline

- Hierarchical WL estimation method
  - Algorithm
  - Experimentation
  - Guidelines
- Placement planning
  - Algorithm
  - Simulation
- Conclusion

Conclusions

- Hierarchical Technique for WL estimation
- Average error of 30-40%
- Study of effects of displacement, aspect ratio and area of blockage
- Application: early design stage
  - Guidelines for determining location and/or aspect ratio of IP blocks
- Placement Planning to determine location of standard cells on chip area


Thank You!