# Stochastic Power/Ground Supply Voltage Analysis via Moment and Correlation Computation by Statistical Transient Toggling Analysis

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## Abstract

Power/ground supply voltage degradation has significant effect on nanometer VLSI design system performance. Conventional techniques find over-pessimistic worst case supply voltage degradation of little occurrence probability. Stochastic supply voltage analysis models an RLC power/ground delivery network as a linear system for given stochastic supply currents. In this paper, we complement stochastic P/G network analysis and form a complete stochastic supply voltage analysis flow. We propose statistical transient toggling analysis (STTA), which computes statistical supply current moments and correlations by extending the probabilistic signal toggling analysis technique in power estimation to time domain transient analysis. Our experimental results on ISCAS test cases show that STTA achieves better accuracy and orders of magnitude of speedup compared with Monte Carlo simulation.

## 1 Introduction

Power/ground (P/G) supply voltage degradation is becoming increasingly severe in nanometer VLSI designs. This is because: (1) technology scaling implies decreased wire widths and increased interconnect resistance along a P/G supply network, (2) an increased device density leads to an increased supply current density on a chip, and (3) a higher clock frequency leads to more significant inductance effect. On the other hand, technology scaling implies a decreasing supply voltage and a decreasing noise margin for signal transition, which makes a transistor more vulnerable to supply voltage degradation. A degraded supply voltage leads to performance degradation or even malfunction. For example, a 10% supply voltage degradation could be responsible for 10% transistor performance degradation, and the effect is super-linear [15]. Therefore, P/G supply network design in a nanometer VLSI system is critical to system performance and functionality.

A power supply network is an RLC interconnect network, which can be reduced by model order reduction techniques [21] to frequency domain transfer functions for improved analysis efficiency. Maximum current waveform envelopes [2] bound dynamic supply current excitations, and allow application of conventional static timing analysis techniques. However, a power supply network is difficult to analyze due to its complex topology, large instance size, and large input/output numbers. A number of techniques have been proposed for efficiency and scalability improvement of power supply network analysis, which include multigrid-like [6, 12], hierarchical [20], random walk [14], etc.

Supply currents vary with input vectors and system operation mode, and have a significant effect on supply voltage statistics. Supply currents are also a major factor in determining power consumption. For worst case power consumption, maximum supply currents can be found by solving weighted maximum-satisfiability[3], integer linear programming[5], or relaxed linear programming for an upper bound[16]. More scalable algorithms include a greedy algorithm which assigns signal transitions in decreasing order of interconnect capacitance, followed by justification, i.e., ATPG-like backtracing and implication [17], a genetic algorithm which assigns signal transitions in decreasing order of the product of interconnect capacitance and maximum possible signal toggling rate [4], and application of the extreme order statistics and maximum likelihood theory for reduced number of input patterns for worst case supply currents [18].

These methods are pessimistic, i.e., they compute an upper bound of maximum supply current excitation which has little probability to occur. In practice, one is more interested in obtaining an "expected" maximum supply voltage degradation with certain confidence level. Such an expected prediction is obtained by applying an empirical scaling factor in some industry practices. Accurate prediction of expected maximum supply voltage drop needs stochastic techniques.

A stochastic P/G supply voltage analysis approach is proposed in [13], which takes an RLC power supply network as a linear system, and computes power supply voltage degradation moments (e.g., means and standard deviations) for given stochastic supply currents. However, it is not presented in [13] on how to compute supply current moments and correlations, which are inputs of stochastic supply voltage estimation.

In this paper, we extend the probabilistic signal toggling computation technique in power estimation, and propose statistical transient toggling analysis (STTA), which efficiently com-

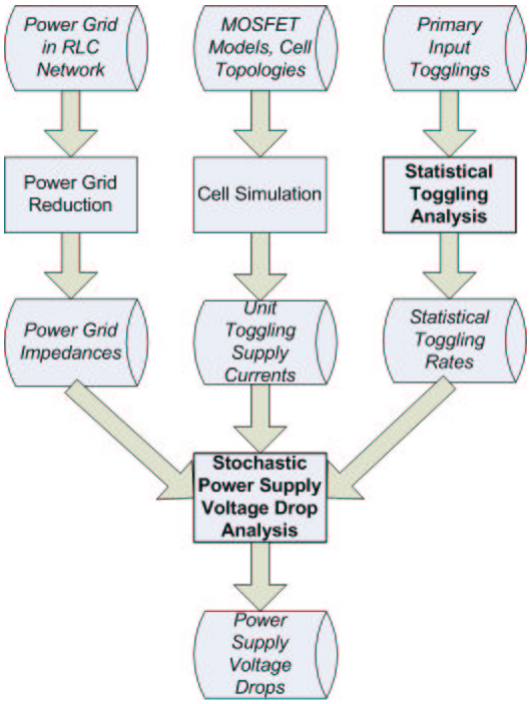


Figure 1: A stochastic P/G supply voltage analysis flow. We propose statistical transient toggling analysis (STTA) and complete this flow.

pute statistical signal toggling means and standard deviations, and spacial and temporal correlations between signal togglings for different gates at different time steps. We combine our proposed statistical signal toggling analysis with the stotastic P/G analysis technique in [13] for a complete flow of stochastic P/G supply voltage analysis.

The rest of the paper is organized as follows. We introduce the overall stochastic P/G supply voltage analysis flow in Section 2, followed by the stochastic P/G network analysis technique in Section 3, and the probabilistic signal toggling analysis technique in power estimation in Section 4. We propose statistical transient toggling analysis (STTA) for stochastic supply current moments and correlations in Section 5, which completes the stochastic P/G supply voltage anlaysis in Section 6. We present a numerical example in Section 7 and our experimental results in Section 8, before concluding in Section 9.

## 2 Stochastic Supply Voltage Analysis Problem Formulation

A P/G supply network connects P/G sources to active components in a VLSI design through inherent or parasitic resistors, capacitors and possible inductors. A signal transition at a gate injects a current into the P/G supply network, and results in voltage variations across the P/G supply network.

Such power supply voltage degradation leads to circuit performance degradation or even logic malfunction, and must be save-guarded, e.g., as follows.

$$\Delta V_p \leq U \quad \forall p \in N \tag{1}$$

An RLC power supply network is a linear system. For a linear system, its transfer function between each input and output nodes is given or can be reduced by moment order reduction techniques to a linear function, e.g., $h_{pj}(t)$ between two nodes $p$ and $j$. Also for a linear system, the contribution of each input can be summed up to give the response in the presence of multiple inputs. This gives time domain supply voltage of a P/G node $p$ as follows.

$$V_p(t) = \sum_j \int_0^\infty I_j(t-\tau) h_{pj}(\tau) d\tau \tag{2}$$

The effects of supply currents are more difficult to estimate. A gate draws supply current when it goes through a signal transition or toggling. This unit toggling supply current can be obtained by circuit simulation, e.g., using SPICE. However, the number of signal togglings of a gate in a unit time depends on the primary inputs, the combinational logics, and the sequential status of the circuit, and is difficult to obtain.

In power estimation [9], signal toggling rate or the number of signal togglings of a gate per unit time is computed in a netlist. However, no time domain analysis is available in this signal toggling rate computation. In statistical static timing analysis, signal arrival(toggling) time is a statistical variable given in a probability density function. This probability density function results from a input-vector-independent static analysis, where a signal toggling is assumed for each gate in a clock cycle, i.e., the accumulation of the probability density gives one. Further, no time domain correlation is available in a signal arrival time pdf.

In this paper, we extend signal toggling rate in power estmation to transient signal toggling rate, and present closed form formulas for transient signal toggling rate computation, and give means, variances, and spacial and temporal co-variances of the supply currents for a complete stochastic supply voltage analysis flow.

We formulate the stochastic power supply voltage drop analysis problem as follows.

**Problem 1** *Given*

1. *an RLC P/G supply network,*
2. *transistor models and transistor level netlist for each gate,*
3. *primary input signal togglings and gate level netlist,*

*find the stochastic supply voltage at node p in the P/G network.*

Fig. 1 gives the flow of stochastic supply voltage analysis, which includes: (1) power supply network model order reduction for transfer function $h_{pj}(t)$ between two nodes, (2) circuit simulation for unit toggling gate supply current $\hat{I}_j$, (3) statistical transient toggling analysis for the means, the variances, and the spacial and temporal correlations of signal togglings in the design, and (4) stochastic P/G network analysis. Algorithm 1 summarizes stochastic supply voltage analysis.

**Algorithm 1: Stochastic Supply Voltage Analysis**

**Input:** P/G supply network $G$,
transistor models and netlist for each gate,
primary input signal togglings and gate level netlist,
**Output:** Stochastic supply voltage for each node $p$ in $G$

1. Compute $Z_{pj}$ by model order reduction for P/G network $G$
2. Compute $\hat{I}(t)$ by circuit simulation for each gate
3. Statistical transient toggling analysis (STTA)
4. Stochastic P/G network analysis

In the next sections, we present the stochastic P/G network analysis technique in Section 3, the signal toggling analysis techniques in power estimation in Section 4, and propose stochastic transient toggling analysis (STTA) in Section 5 which completes the stochastic supply voltage analysis flow in Section 6.

# 3 Stochastic P/G Network Analysis

Stochastic analysis approach has been proposed for power supply voltage drop analysis [13]. In stochastic P/G supply voltage analysis, supply currents are modeled as stochastic processes, their statistical characteristics, e.g., means and correlations, are extracted. An RLC power supply network is a linear system. Therefore, its stochastic outputs, i.e., power supply voltage drops, are computed based on given stochastic inputs, i.e., supply currents.

For example, the mean of a supply voltage drop $V_p$ is given by the mean of each supply current $I_j$ and the corresponding power grid transfer function $h_{pj}(t)$ between $V_p$ and $I_j$ as follows.

$$\begin{aligned}\bar{V}_p &= E(\sum_j \int_0^\infty I_j(t-\tau)h_{pj}(\tau)d\tau) \\ &= \sum_j \int_0^\infty E(I_j(t-\tau))h_{pj}(\tau)d\tau = \sum_j \bar{I}_j \int_0^\infty h_{pj}(\tau)d\tau \quad (3)\end{aligned}$$

Basic statistics theory gives the variance of a power supply voltage drop as follows.

$$\sigma^2(V_p) = \bar{V}_p^2 - (\bar{V}_p)^2 \quad (4)$$

We have

$$\begin{aligned}\bar{V}_p^2 &= E(\sum_j \sum_k \int_0^\infty I_j(t-\tau)h_{pj}(\tau)d\tau \cdot \int_0^\infty I_k(t-\tau)h_{pk}(\tau)d\tau) \\ &= \sum_j \sum_k \int_0^\infty \int_0^\infty R_{jk}(\tau_1-\tau_2)h_{pj}(\tau_1)h_{pj}(\tau_2)d\tau_1 d\tau_2 \quad (5)\end{aligned}$$

where

$$\begin{aligned}R_{jk}(\tau_1-\tau_2) &= E(I_j(\tau_1)I_k(\tau_2)) \\ &= cov(I_j(\tau_1), I_k(\tau_2)) + \bar{I}_j(\tau_1)\bar{I}_k(\tau_2)\end{aligned}$$

since the covariance between supply currents $I_j$ and $I_k$ is defined as

$$cov(I_j(\tau_1), I_k(\tau_2)) = E((I_j(\tau_1)-\bar{I}_j(\tau_1))(I_k(\tau_2)-\bar{I}_k(\tau_2)))$$

However, it is not presented in [13] on how to compute signal toggling correlations in a design. A straightforward signal togging correlation computation approach is to extract the logic between every two gates in a circuit, e.g., based on BDD construction and computation. However, such an approach would still be too computationally expensive to be practical. In the following sections, we review the existing power estimation literature for probabilistic signal toggling computation techniques, and propose statistical transient signal toggling analysis, which computes means and variances of signal togglings, and correlations between signal togglings of different gates at different time steps in a circuit.

# 4 Signal Toggling Analysis in Power Estimation

Signal toggling analysis plays an important role in dynamic power estimation [10]. There are two categories of methods: simulation based and probabilistic. Simulation based method is input pattern dependent and less efficient. Probabilistic signal toggling analysis is appealing in its efficiency at the cost of an acceptable accuracy loss.

There are two important concepts in probabilistic signal toggling analysis.

**Definition 1** Signal probability $P(j)$ *of a net* $j$ *is the probability for the net to obtain a logic one status.*

Signal probability $P(j)$ can be computed efficiently across each Boolean component in a netlist. For example, for a NAND gate with output $j = l_1 \cdot l_2$, basic probability theory applies to give $P(j) = P(l_1)P(l_2)$. In general, signal probabilities can be computed by using BDD representation of Boolean functions. For a Boolean function $j = f(l_1,...,l_n)$, if the inputs $l_i$ are independent, then the signal probability of $f$ can be obtained in linear time of its BDD representation as follows.

$$P(j) = P(l_1)P(f_{l1}) + P(\bar{l_1})P(f_{\bar{l1}}) \quad (6)$$

where $f_{l1} = f(1,l_2,...,l_n)$ and $f_{\bar{l1}} = f(0,l_2,...,l_n)$ are cofactors of $f$ with respect to $l_1$. Therefore, a single traversal of a netlist gives signal probabilities for each net.

**Definition 2** Signal toggling rate $f_j$ *is a statistical variable of the number of signal togglings per unit time for a gate* $j$.

The signal toggling rate $f_j$ at the output of a gate $j$ is given by the sum of input signal toggling rates $f_{l_i}$, each weighted by the occurrence probability for the path between the input and the output to be enabled. A path between an input $l_i$ and the output $j$ is enabled if the Boolean difference function $\frac{\partial j}{\partial l_i}$ is true [9].

$$\begin{aligned}f_j &= \sum_i P(\frac{\partial j}{\partial l_i}) f_{l_i} \\ \frac{\partial j}{\partial l_i} &= j\,|_{l_i=1} \oplus j\,|_{l_i=0} \quad (7)\end{aligned}$$

where $\oplus$ denotes the exclusive-or operation.

For given signal probabilities in (6) in a netlist, Boolean difference probabilities and signal toggling rates in (7) can be computed efficiently in a single traversal of the netlist.

As is given in (7), signal toggling rate of the output is a weighted sum of the input signal toggling rates, and the Boolean differences for each input of the component can be computed based on signal probabilities. Statistics theory gives the mean, the variance, the co-variance and the correlation of a linear function as follows [1, 8].

$$\begin{aligned}
\bar{f_j} &= \sum_i P(\frac{\partial j}{\partial l_i})\bar{f_{l_i}} \\
\sigma^2(f_j) &= \sum_i P^2(\frac{\partial j}{\partial l_i})\sigma^2(f_{l_i}) \\
&+ 2\sum_{i,h} P(\frac{\partial j}{\partial l_i})P(\frac{\partial j}{\partial l_h})cov(f_{l_i}, f_{l_h}) \\
cov(f_j, f_k) &= \sum_i P(\frac{\partial j}{\partial l_i})cov(f_{l_i}, f_k) \\
corr(f_j, f_k) &= \frac{cov(f_j, f_k)}{\sigma(f_j)\sigma(f_k)} \qquad (8)
\end{aligned}$$

where correlation $corr(f_j, f_k) = 0$ for independent random variables $f_j$ and $f_k$, and $corr(f_j, f_k) = 1$ if $f_j$ and $f_k$ are in a linear function relationship.

This method efficiently computes mean signal toggling rates for each gate, as well as signal toggling correlations between any two gates, in a single traversal of the netlist. Signal correlations in a netlist come from two sources: (1) correlations between primary inputs, and (2) the presence of fanout nets in a netlist. This method takes into consideration of both signal correlation sources.

# 5 Statistical Transient Toggling Analysis (STTA)

We extend the statistical signal toggling analysis in power estimation to transient signal toggling rate, which allows us to compute means, variances, spacial and temporal co-variances of supply currents for a complete stochastic supply voltage analysis.

We define transient signal toggling rate as follows.

**Definition 3** Transient signal toggling rate $f_j(t)$ *is a statistical variable of the number of signal togglings per unit time for a gate* $j$ *at time* $t$.

Transient signal toggling rate $f(t)$ is an extension of signal toggling rate $f$, in that it divides the time domain and provides a statistical variable for signal toggling at each time $t$. A direct advantage of transient signal toggling analysis is that it computes temporal supply current co-variances, which are needed for a complete stochastic supply voltage analysis.

The mean, the variance, the co-variance and the correlation of transient signal toggling rate at the output of a gate $j$ of delay $d_j$ are given as follow.

$$\begin{aligned}
\bar{f_j}(t) &= \sum_i P(\frac{\partial j}{\partial l_i})\bar{f_{l_i}}(t-d_j) \\
\sigma^2(f_j(t)) &= \sum_i P^2(\frac{\partial j}{\partial l_i})\sigma^2(f_{l_i}(t-d_j)) \\
&+ 2\sum_{i,h} P(\frac{\partial j}{\partial l_i})P(\frac{\partial j}{\partial l_h}) \\
&\cdot cov(f_{l_i}(t-d_j), f_{l_h}(t-d_j)) \\
cov(f_j(t_1), f_k(t_2)) &= \sum_i P(\frac{\partial j}{\partial l_i})cov(f_{l_i}(t_1-d_j), f_k(t_2)) \\
corr(f_j(t_1), f_k(t_2)) &= \frac{cov(f_j(t_1), f_k(t_2))}{\sigma(f_j(t_1))\sigma(f_k(t_2))} \qquad (9)
\end{aligned}$$

The moments and correlations of a transient signal toggling rate can be represented in polynomials for run time and memory space efficiency, and the linear operations in (9) give the moments and correlations of transient signal toggling rates in polynomials during propagation. Computing the moments and the correlations of a transient signal toggling rate takes constant time by applying (9), and a single traversal of the netlist gives all moments and correlations of transient signal toggling rates.

# 6 Applying STTA in Stochastic Supply Voltage Analysis Flow

Given transient signal toggling rate $f_j(t)$, a unit toggling supply current $\hat{I}_j(t)$ is translated into a stochastic supply current $I_j(t)$ by convolution as follows.

$$I_j(t) = \int \hat{I}_j(t-\tau) f(\tau) d\tau \qquad (10)$$

Stochastic supply current $I_j(t)$ is a statistical variable of the supply current of gate $j$ which is observed at time $t$. For a pulse function of unit toggling supply current $\hat{I}_j(t) = |I_j|\delta(t)$, $I_j(t) = |I_j| f_j(t)$.

This stochastic supply current $I_j(t)$ is then applied to (3), (4), and (5) for means, variances, and covariances of transient supply currents.

We summarize statistical transient toggling analysis for stochastic P/G supply voltage analysis in Algorithm 2.

**Algorithm 2: Applying Statistical Transient Toggling Analysis in Stochastic Supply Voltage Analysis**

**Input:** $P(i), \bar{f_i}(t), \sigma^2(f_i(t)), cov(f_i(t_1), f_j(t_2)), \forall i, j \in PI$
$h_{pj}(t), \hat{I}_j(t), \forall j \in N$

**Output:** $\bar{V_p}$, $\sigma^2(V_p)$

1. Traverse the netlist, for each gate $j$ at each time step $t$
2. Compute output signal probability $P(j)$ by (6)
3. Compute $\bar{f_j}(t)$, $\sigma^2(f_j)(t)$, and $cov(f_i(t_1), f_j(t_2))$ by (9)
4. Compute stochastic supply current $I_j(t)$ by (10)
5. Compute $\bar{V_p}$ and variance $\sigma^2(V_p)$ by (3), (4) and (5)

# 7 Numerical Example

Consider a simple instance with two supply current sources, which each has 50% probability to output a unit supply current, so that the mean of each supply current is $\mu_1 = \mu_2 = 0.5$, the variance is $\sigma_1^2 = \sigma_2^2 = 0.25$. Assuming unit transfer functions $\int_0^\infty h_1(\tau)d\tau = \int_0^\infty h_2(\tau)d\tau = 1$ for the two supply current sources to cause supply voltage drop $V_p$, based on (3), (4), (5), and (9), we have

$$\begin{aligned} \bar{V_p} &= \bar{I_1} + \bar{I_2} = 0.5 + 0.5 = 1 \\ \bar{V_p^2} &= \sum_{j=1}^{2}\sum_{k=1}^{2} R_{jk} = \sum_{j=1}^{2}\sum_{k=1}^{2} cov(I_1, I_2) + \bar{I_1}\bar{I_2} \end{aligned} \quad (11)$$

and

$$\sigma^2(V_p) = \begin{cases} 1 & corr(I_1, I_2) = 1 \\ 0.5 & corr(I_1, I_2) = 0 \\ 0 & corr(I_1, I_2) = -1 \end{cases} \quad (12)$$

I.e., if the two supply currents are independent, $corr(I_1, I_2) = 0$, and $\sigma^2(V_p) = 0.5$; if the two supply currents are identical, $corr(I_1, I_2) = 1$, and $\sigma^2(V_p) = 1$; if the two supply currents are exclusive, i.e., only one of them takes place at a time, $corr(I_1, I_2) = -1$, and $\sigma^2(V_p) = 0$ which gives a constant supply voltage drop.

# 8 Experiment

In the following experiments, we validate our proposed statistical transient toggling analysis for stochastic P/G supply voltage analysis, by comparing with Monte Carlo simulation results.[1]

We implement a logic simulator based on the five-value logic, i.e., logic one, logic zero, rising signal transition, falling signal transition, and uncertainty. We further enhance the five-value logic simulator by taking signal glitches into account. E.g., a controlling logic value at an input of a gate blocks any signal glitch in the other inputs of the gate to propagate to the output of the gate, while a rising or falling signal transition has 50% probability to be a controlling logic value of the gate and block any signal glitch in the other inputs to propagate to the output of the gate. The 50% probability corresponds to the timing of the two signal transitions. For example, a rising and a falling signal transition at the inputs of a two-input NAND gate have 50% probability to generate a glitch at the output of the NAND gate. The exact glitch count needs to be given by a dynamic timing analyzer.

We conduct our experiments based on the ISCAS benchmark test cases. These test cases have 124 to 561 gates, with an average of 20.0% of the nets are fanout nets. We regard these ISCAS benchmark test cases as part of a large design, e.g., the cell instances are connected by a power strip, with $0.2\Omega$ power strip resistance between each two adjacent cell instances, and $0.05mA$ unit toggling supply current for each cell instance, as in $90nm$ technology. For each test case, we apply our statistical transient toggling analysis and the five-value logic simulation. In the first part of the experiment, we assign logic one, logic zero, rising signal transition, and falling signal transition to the primary inputs of a test case, with 10% probability for a signal transition to occur, and equal occurrence probabilities for logic one and logic zero. Correspondingly, in statistical transient toggling analysis, the primary inputs have 0.5 signal probability, 0.1 mean signal toggling rate, and 0.09 variance of signal toggling rate. In the second part of the experiment, we assign logic one, logic zero, rising signal transition, and falling signal transition with equal occurrence probabilities to the primary inputs. Correspondingly, in statistical transient toggling analysis, the primary inputs have 0.5 signal probability, 0.5 mean signal toggling rate, and 0.25 variance of signal toggling rate. In both cases, we keep the primary inputs independent to each other, such that there is zero covariance of signal toggling rate between any two primary inputs. We compute the mean and the variation of a supply voltage drop $V_p$ based on (3), (4), and (5).

Table 1 shows the means and the standard deviations of a supply voltage drop obtained by statistical signal toggling analysis, 10,000 runs, and 100 runs of Monte Carlo logic simula-

Table 1: Power supply voltage drop ($mV$), its standard deviation ($mV$), and runtime ($s$) given by (1) statistical transient toggling analysis, (2) 10,000 Monte Carlo simulation runs, and (3) 100 Monte Carlo simulation runs, while the primary inputs have (I) 0.5 signal probability, 0.1 mean signal toggling rate, and 0.09 variance of signal toggling rate, or (II) 0.5 signal probability, 0.5 mean signal toggling rate, and 0.25 variance of signal toggling rate.

| (I) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| test | STTA | | | $10K\times$ Monte Carlo | | | $100\times$ Monte Carlo | | |
| case | $V_{dr}$ | $\sigma(V_{dr})$ | CPU | $V_{dr}$ | $\sigma(V_{dr})$ | CPU | $V_{dr}$ | $\sigma(V_{dr})$ | CPU |
| s208 | 5.13 | 5.17 | 0.00 | 4.73 | 5.40 | 6.04 | 4.06 | 4.51 | 0.16 |
| s298 | 9.19 | 7.70 | 0.00 | 8.98 | 8.96 | 8.20 | 8.04 | 8.23 | 0.21 |
| s344 | 22.13 | 14.55 | 0.00 | 20.50 | 22.57 | 13.02 | 20.87 | 25.13 | 0.36 |
| s349 | 21.04 | 16.07 | 0.01 | 20.32 | 22.92 | 12.59 | 22.97 | 27.92 | 0.37 |
| s382 | 17.32 | 12.53 | 0.01 | 14.70 | 13.07 | 12.91 | 16.24 | 14.04 | 0.36 |
| s386 | 13.35 | 13.31 | 0.01 | 14.95 | 16.32 | 12.25 | 14.50 | 14.49 | 0.32 |
| s526 | 21.79 | 14.73 | 0.01 | 20.28 | 17.12 | 19.01 | 19.26 | 16.76 | 0.52 |
| s1196 | 127.51 | 102.02 | 2.57 | 113.01 | 97.98 | 103.00 | 97.02 | 91.15 | 3.25 |
| s1238 | 120.07 | 96.78 | 2.47 | 108.59 | 93.01 | 95.59 | 102.47 | 97.04 | 3.29 |
| (II) | | | | | | | | | |
| test | STTA | | | $10K\times$ Monte Carlo | | | $100\times$ Monte Carlo | | |
| case | $V_{dr}$ | $\sigma(V_{dr})$ | CPU | $V_{dr}$ | $\sigma(V_{dr})$ | CPU | $V_{dr}$ | $\sigma(V_{dr})$ | CPU |
| s208 | 25.65 | 8.62 | 0.00 | 23.75 | 9.50 | 6.04 | 22.66 | 8.53 | 0.16 |
| s298 | 45.97 | 12.83 | 0.00 | 43.35 | 14.26 | 8.20 | 41.09 | 13.53 | 0.21 |
| s344 | 110.64 | 24.25 | 0.00 | 95.35 | 32.15 | 13.02 | 94.86 | 36.51 | 0.36 |
| s349 | 105.21 | 26.79 | 0.01 | 93.87 | 32.85 | 12.59 | 94.13 | 36.89 | 0.37 |
| s382 | 86.62 | 20.88 | 0.01 | 73.21 | 22.38 | 12.91 | 71.75 | 21.17 | 0.36 |
| s386 | 66.74 | 22.18 | 0.01 | 68.63 | 24.32 | 12.25 | 71.73 | 24.68 | 0.32 |
| s526 | 108.95 | 24.54 | 0.01 | 102.54 | 28.99 | 19.01 | 98.74 | 28.69 | 0.52 |
| s1196 | 600.36 | 161.25 | 2.57 | 538.90 | 152.67 | 103.00 | 512.44 | 133.65 | 3.25 |
| s1238 | 637.54 | 169.99 | 2.47 | 564.82 | 160.94 | 95.59 | 540.41 | 141.38 | 3.29 |

[1] In power estimation literature, techniques are in two categories: probabilistic and Monte Carlo simulation based. Since our statistical transient toggling analysis is an extension of the probabilistic methods, we compare with Monte Carlo simulation method.

tion. We observe significant variability of power supply voltage drop, e.g., the standard deviations are close to the means of power supply voltage drop in most cases in our experiment. Our Monte Carlo simulation gives increasingly accurate estimates of power supply voltage drop. However, we do not observe fast convergence of Monte Carlo simulation for these ISCAS benchmark test cases, and large numbers of runs are needed for more accurate Monte Carlo simulation results. Our proposed statistical toggling analysis gives accurate estimates with orders of magnitude of runtime speedup.

# 9 Conclusion

Power supply voltage drop needs to be addressed by a stochastic analysis approach given the probabilistic distributions of supply currents, for pessimism reduction in the presence of increased variability in nanometer VLSI designs.

Existing stochastic power supply voltage drop analysis did not provide computation method for supply current spacial and temporal correlations. We extend the probabilistic signal toggling analysis techniques in power estimation, and propose statistical transient toggling analysis (STTA), which efficiently computes means and variances of, and spacial and temporal correlations between supply currents in a design. Our proposed statistical transient toggling analysis technique complements the stochastic P/G network analysis technique and forms a complete stochastic P/G supply voltage analysis flow, and achieves better accuracy and orders of magnitude of speedup compared with Monte Carlo simulation.

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