Revamping Electronic Design Process to Embrace Interconnect Dominance

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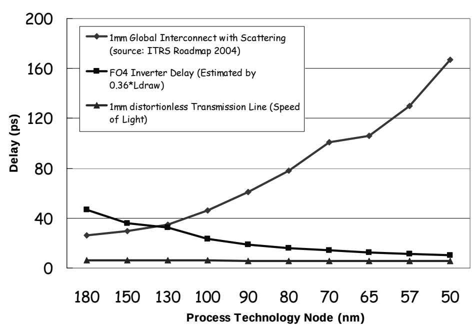
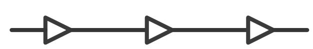
Interconnect Dominance





Goals: Speed, Power, Cost

Constraints: Area, Current, Skew

Challenges: PVT Variations, Signal Integrity

Outlines

- *Interconnect Technologies*
  - *Buffers, Pitches, Circuit Styles*
- *Geometrical Planning*
  - *Wire Orientations, Chip Shapes*
- *Interconnect Networks*
  - *Topologies, Wire Styles*
- *Power and Clock Distributions*
- *Functional Modules*
  - *Adders, Shifters*
- *Conclusion*

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Interconnect Technologies

- *RC Wires*
  - *Wire Pitch, Width, Separation*
  - *Buffer Size, Buffer Interval*
- *Transmission Line*
  - *RLCG*

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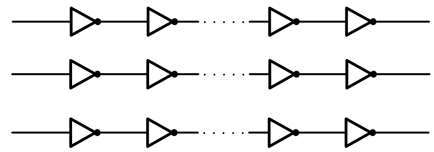
Interconnect Technologies

Coupling capacitance:



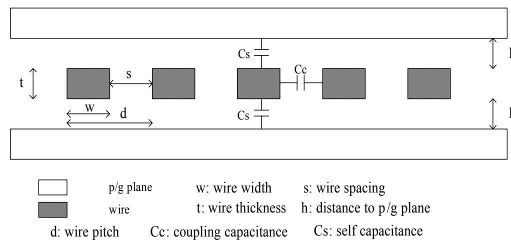
$$\frac{C_c^a}{\varepsilon} = \frac{t}{s}\left(1 - 1.5e^{\frac{t}{2.5s}} e^{-\frac{h}{0.31s}} + 1.5e^{-\frac{h}{0.08s}} - 0.13e^{-\frac{t}{1.3s}}\right)$$

$$\frac{C_c^{fr}}{\varepsilon} = \left(\frac{h}{s}\right)^{0.2}\left(1.53 - 0.98e^{-\frac{w}{0.35h}}\right)\cdot e^{-\frac{s}{0.65h}} + 0.01$$

Self capacitance:

$$\frac{C_s^{fr}}{\varepsilon} = \left(1.05 + 0.63e^{-\frac{t}{s}} - e^{-\frac{s}{1.2h}}\right)\cdot\left(\frac{s}{s+2h}\right)^{0.05}\left(\frac{t}{h}\right)^{0.25} + 0.063$$

$$\frac{C_s^a}{\varepsilon} = \frac{w}{h}$$



Total wire capacitance:

$$C_w = \frac{C_c^a}{\varepsilon} + \frac{C_c^{fr}}{\varepsilon} + \frac{C_s^a}{\varepsilon} + \frac{C_s^{fr}}{\varepsilon}$$

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Interconnect Technologies

SRC Roadmap 2005

Year (On-Chip)	*2005*	*2010*	*2015*
$r_n c_n$ (ps)[T40]	*0.870*	*0.400*	*0.180*
$r_w c_w$ (ps/mm)[T80] metal 1	*440*	*1792*	*5951*
interval (um)	*136*	*45.7*	*16.8*
delay (ps/um)	*0.120*	*0.164*	*0.200*

$$Int = \sqrt{\frac{2(1+f)r_n c_g}{r_w c_w}}, \quad Delay(l_{tr})/l_{tr} = (2+\sqrt{2(1+f)})\sqrt{r_n r_w c_g c_w}$$

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Interconnect Technologies

Design metrics: $delay_n$ $bandwidth$ $bandwidth / power$

Objective functions: $delay_n$ $delay_n \times power_n$ $delay_n^2 \times power_n$

For each pitch,
- For each objective function
  - Find wire width w, buffer size s_{inv} and buffer interval l_{inv}
  - Calculate the metrics

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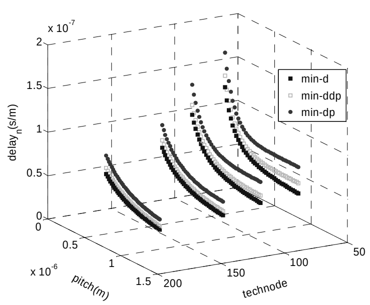
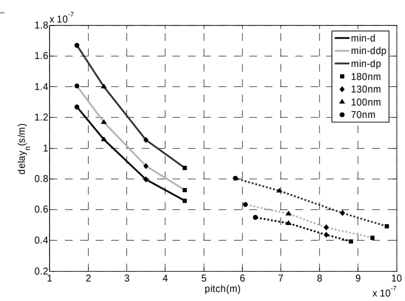
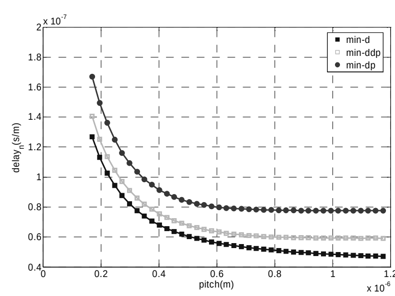
Experimental Results – normalized delay







Top left: Overview
Top right: at different pitches (solid lines: min-pitch; dash lines: saturating pitch)

Bottom right: at 70*nm* technology

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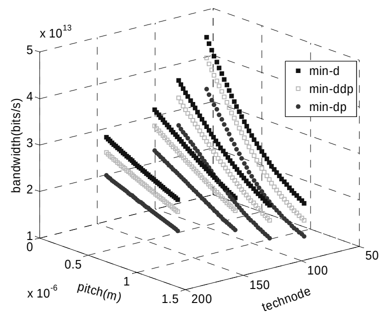
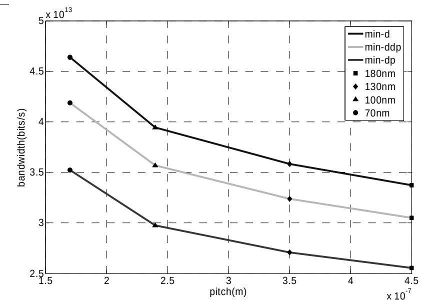
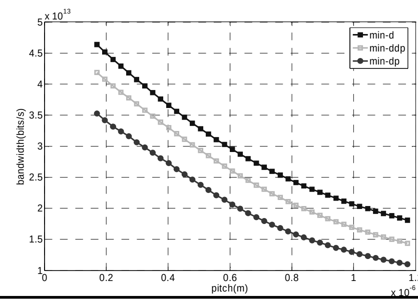
Interconnect Tech. -- bandwidth

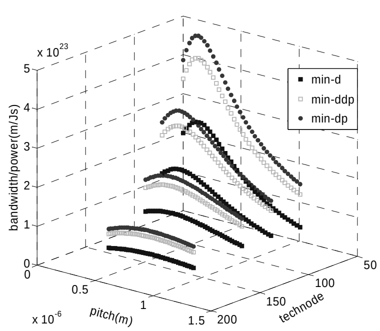


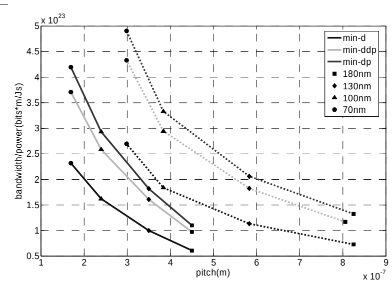


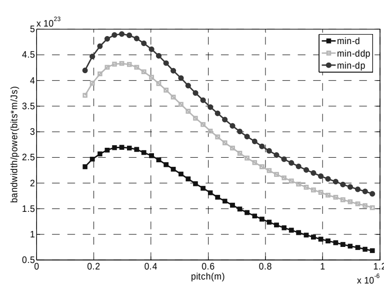


Top left: Overview
Top right: at min-pitches
Bottom right: at 70*nm* technology

Interconnect Tech. – bandwidth/power







Top left: Overview
Top right: at different pitches (solid lines: min-pitch; dash lines: optimal pitch)

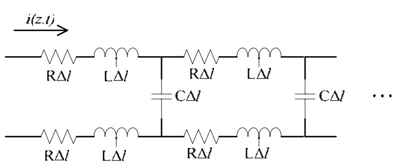
Bottom right: at 70*nm* technology

Interconnect Tech.: Transmission Line

- *Speed-of-the-light on-chip communication*
  - *< 1/5 Delay of Traditional Wires*
- *Low Power Consumption*
  - *< 1/5 Power Consumption*
- *Robust against process variations*
  - *Short Latency*
  - *Insensitive to Feature Size*

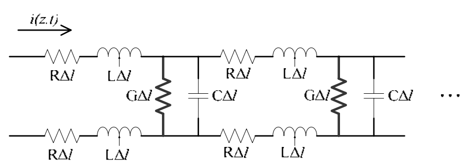
Interconnect Tech.: Transmission Line

Differential Transmission Line



- Serial resistance causes voltage loss.
- Speed and attenuation are frequency dependent.

Surfliner



- Shunt conductance compensates voltage loss: R/G = L/C.
- Flat from DC Mode to Giga Hz
- Telegraph Cable: O. Heaviside in 1887.

Theory (Telegrapher's Equation)

- *Telegrapher's equation:*

$$\frac{dV(z,t)}{dz} = -RI(z,t) - L\frac{dI(z,t)}{dt}$$
$$\frac{dI(z,t)}{dz} = -C\frac{dV(z,t)}{dt} - GV(z,t)$$

- *Propagation Constant:*

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta$$

- *Wave Propagation:*

$$V(z) = V_0 e^{-\alpha z - j\beta z}$$

- *Alpha and Beta corresponds to speed and phase velocity. Both are frequency dependant*

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Theory (Distortionless Line)

- *Set G=RC/L*
- *Frequency Independent speed and attenuation:*

$$\alpha = R/\sqrt{L/C}, \qquad \beta = \omega\sqrt{LC}$$

- *Characteristic impedance: (pure resistive)*

$$Z_0 = \sqrt{L/C}$$

- *Phase Velocity (Speed of light in the media)*

$$v = 1/\sqrt{LC} = c$$

- *Attenuation:*

$$A(z) = e^{-\frac{R}{Z_0}z}$$

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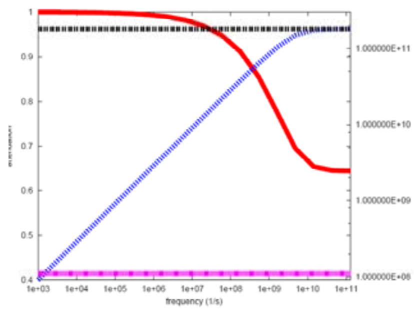
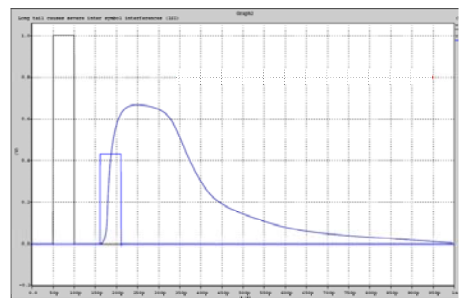
Digital Signal Response



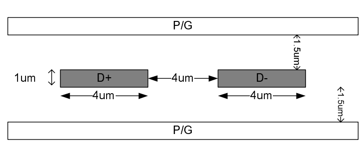
(a) frequency dependency of attenuation and phase velocity

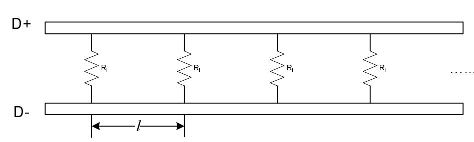


(b) Time domain pulse response of typical on-chip wire and distortionless transmission line

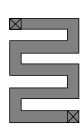
Interconnect Tech.: Transmission Line

- *Add shunt conductance between differential wires*

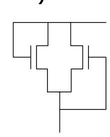




- *Resistors realized by serpentine unsilicided poly, diffusion resistors, or high resistive metal*



(a) unsilicided poly resistor



(b) diffusion resistor

Geometrical Planning

- *Wire Orientations*
  - *Manhattan, Hexagonal, Octagonal, Euclidean*
- *Die Shapes*
  - *Rectangle, Diamond, Hexagon, Octagon, Circle*

Average Radius of Unit-Circle Area

lambda geo. Shape	*Man.*	*Y-Arch*	*X-Arch*	*Euclid.*
Square	*1.329*	*1.122*	*1.070*	*1.017*
Diamond	*1.253*	*1.121*	*1.070*	*1.017*
Hexagon	*1.276*	*1.100*	*1.058*	*1.003*
Octagon	*1.272*	*1.104*	*1.054*	*1.001*
Circle	*1.273*	*1.103*	*1.055*	*1.000*

Throughput : concurrent flow demand

lambda geo. Shape	Man.	Y-Arch	X-Arch*
M: Square	1.000	1.225	1.346
M: Diamond	1.195		
Y: Hexagon		1.315	
X: Octagon*			1.420

*ratio of 0-90 planes and 45-135 planes is not fixed

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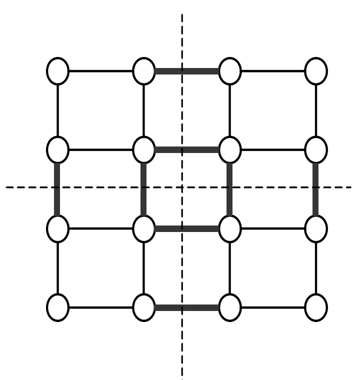
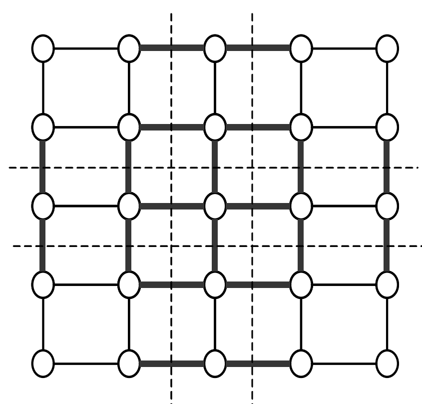
Flow congestion map for uniform 90 Degree meshes





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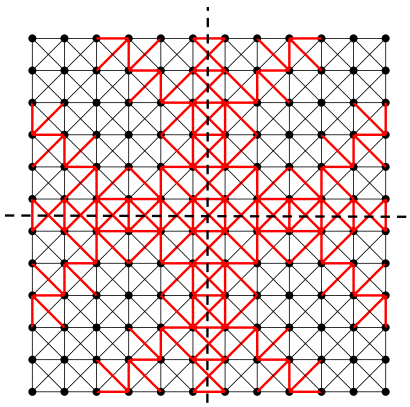
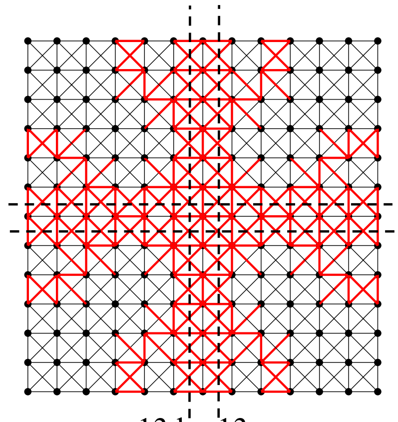
Congestion map of square chip using X-architecture



12 by 12



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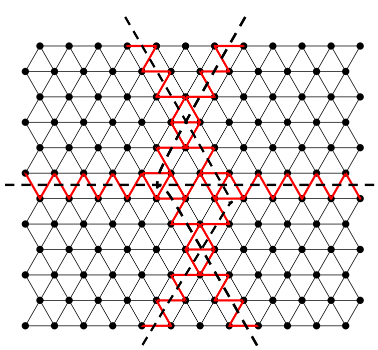
Y-architecture + Square Chip



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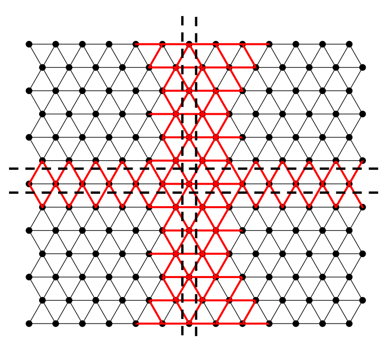
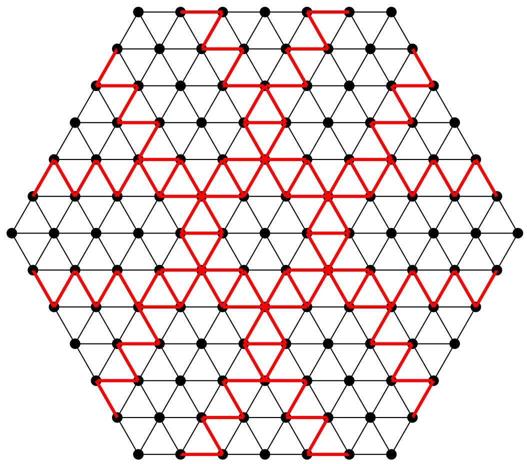
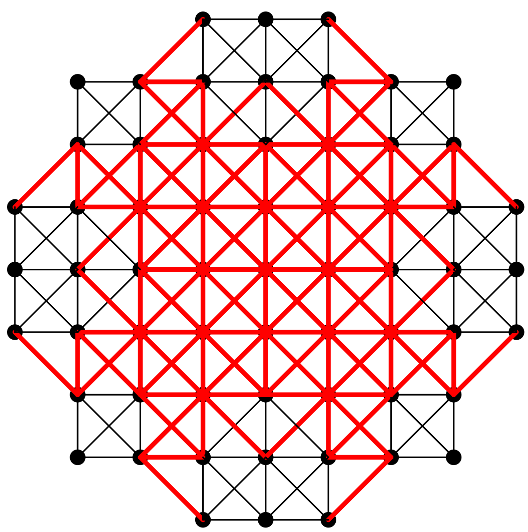


13 by 13

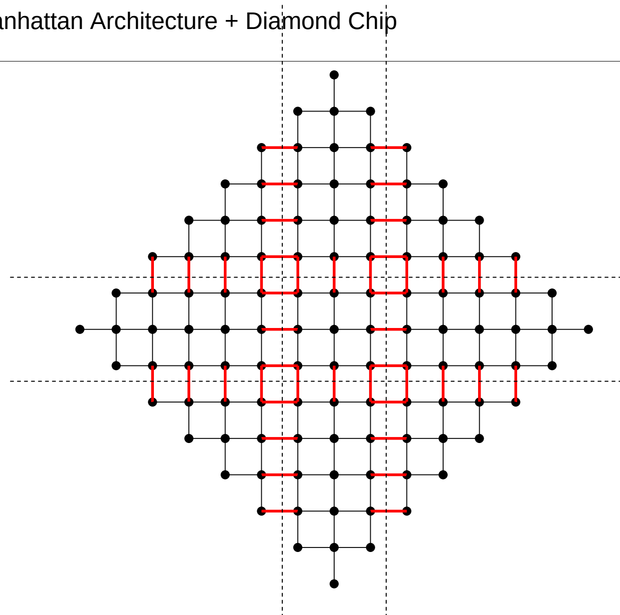
Y Architecture + Hexagonal Chip



X-Architecture + Octagonal Chip

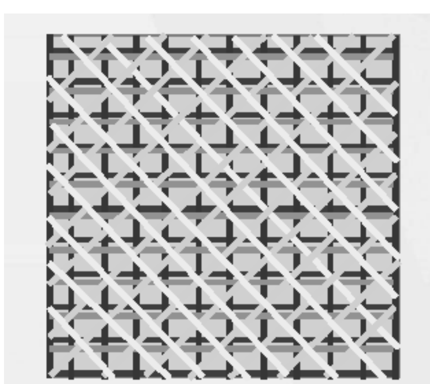


Manhattan Architecture + Diamond Chip

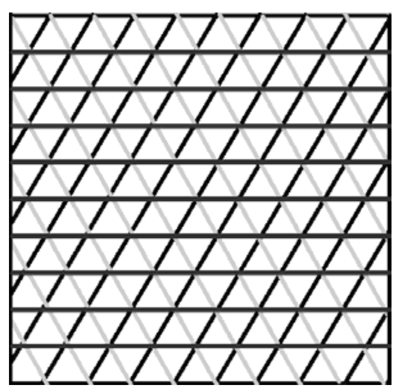


Routing Grids

X-Architecture



Y-Architecture



(http://www.xinitiative.org/img/062102forum.pdf)

Interconnect Networks

- *Optimized Interconnect Architecture*
  - *Data Bus, Control Signals*
- *Shared Interconnect*
  - *Packet Switching*
  - *Circuit Switching*
  - *RTL Level Partition*

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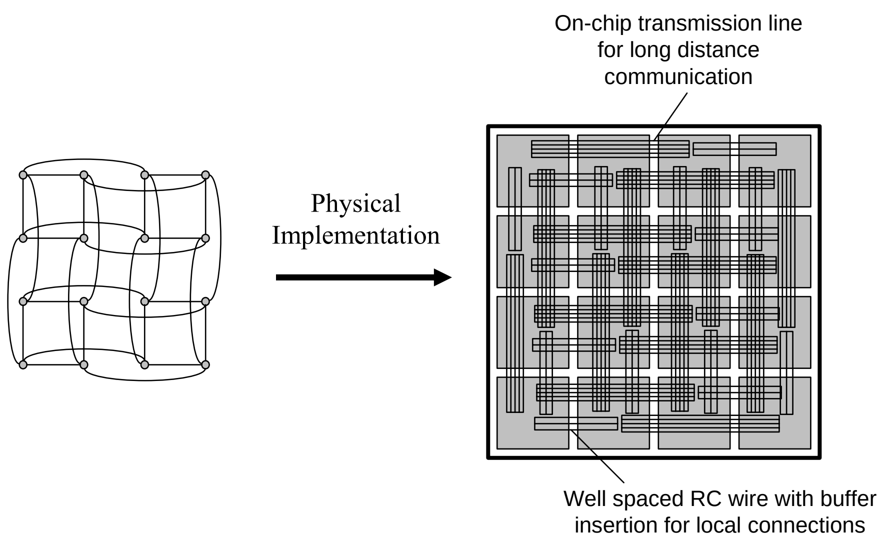
Interconnect Networks



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Interconnect Networks

- *Obj: Power, Latency*
- *Constraints:*
  - *Routing Area, Bandwidth*
- *Design Space:*
  - *Topology*
  - *Wire Styles, Switches*
- *Model:*
  - *Traffic Demand*
  - *Data Bus, Control Signals*

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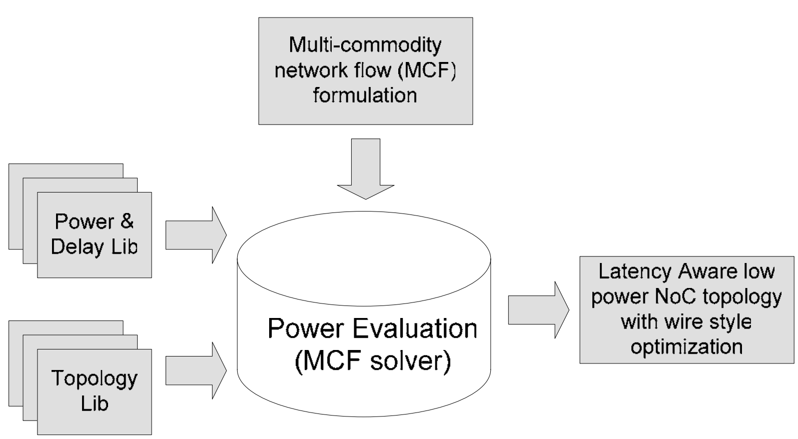
Interconnect Networks: Design Flow



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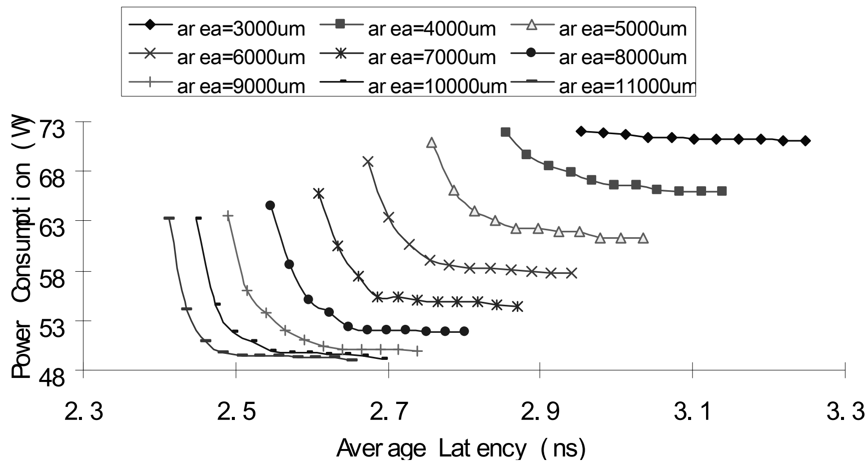
Power and Latency Tradeoffs for Optimal 8x8 Topologies



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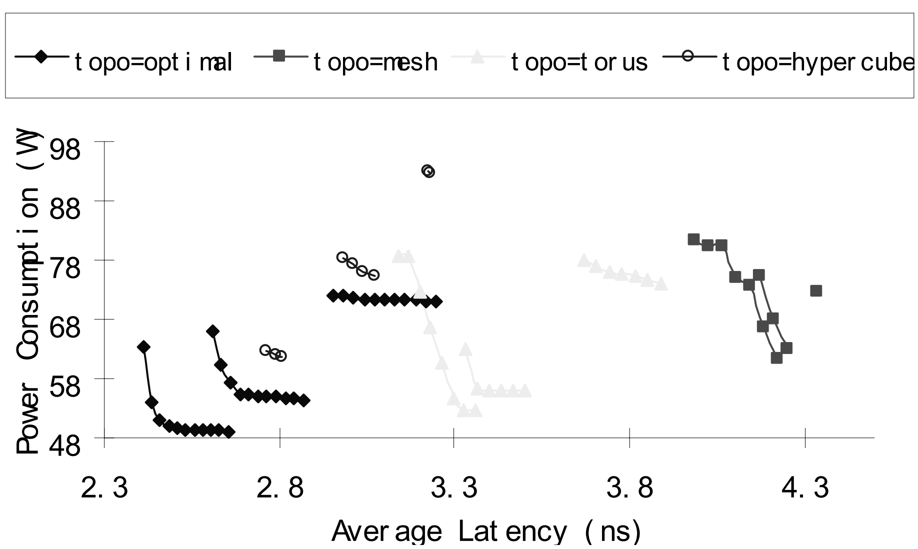
Topology Selection (Latency, Power, BW)



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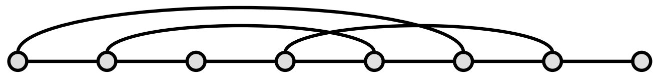
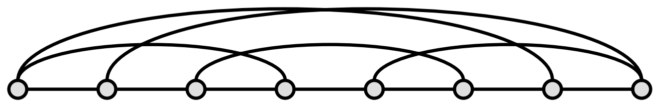
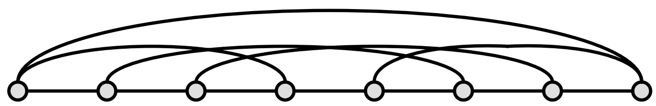
Topology Selection (Latency, Power, BW)



(a) Optimal topology when area = 3000um



(b) Optimal topology when area = 7000um



(c) Optimal topology when area = 11000um

Optimal 8-node topologies vs area resources

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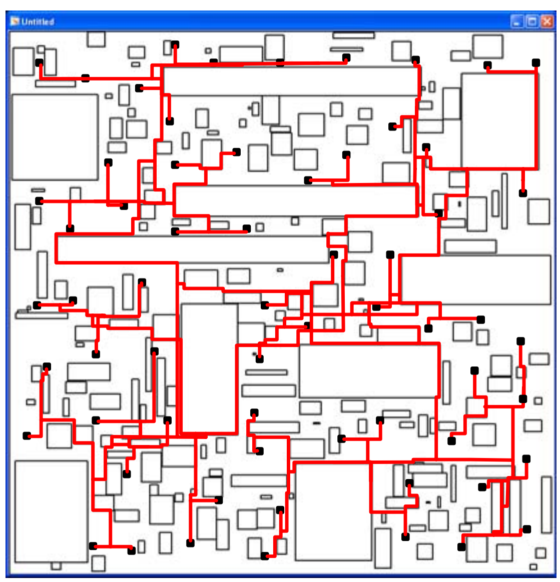
Clock Distributions



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Clock: Linear Variations Model

- *Process variation model*
  - *Transistor length*
  - *Wire width*
  - *Linear variation model*

$$d = d_0 + k_x x + k_y y$$

- *Power variation model*
  - *Supply voltage varies randomly (10%)*

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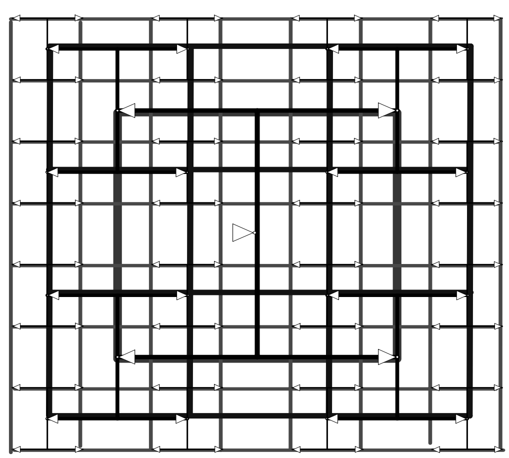
Clock: RC Model

Input: an n level meshes and h-trees
Constraint: routing area, parameter variations
Objective: skew



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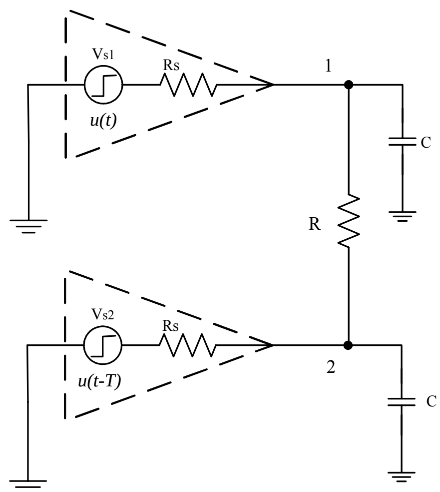
Simplified Circuit Model



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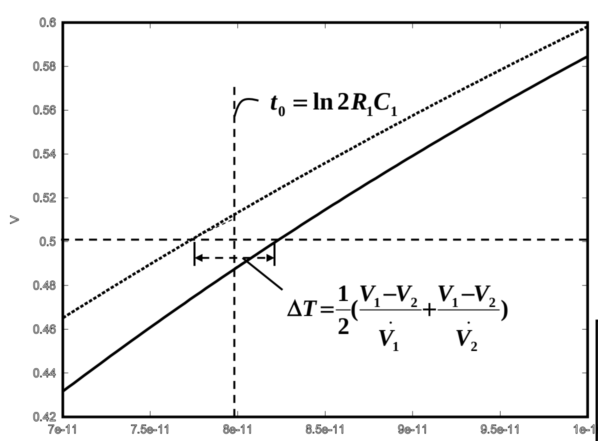
Skew Expression



Assumptions:

1. $T << R_s C$
2. $R_s / R << R_s C/T$

Using first order

Taylor expansion
$e^x = 1 + x$,

Skew function :

$$\Delta T = T \exp(-2 \ln 2 \times \frac{R_s}{R})$$

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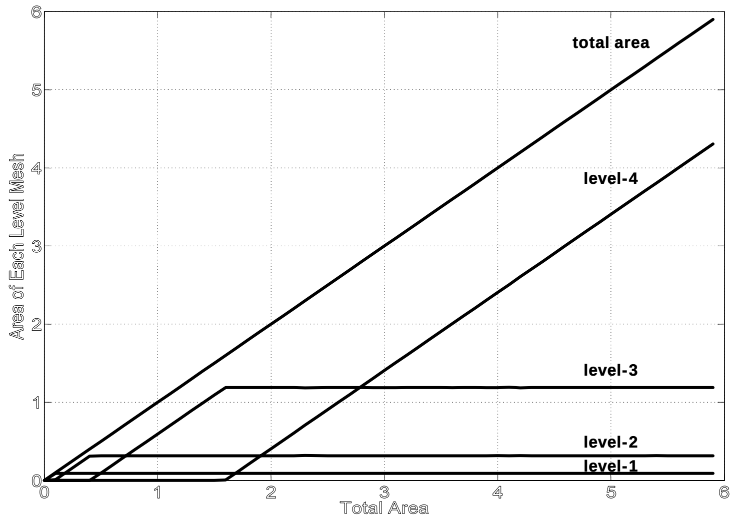
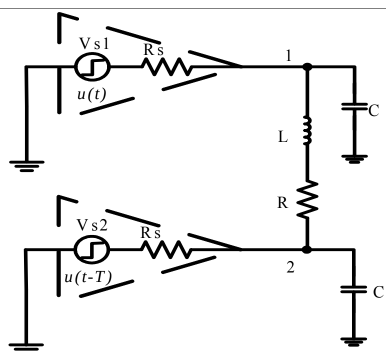
Optimal Routing Resources Allocation



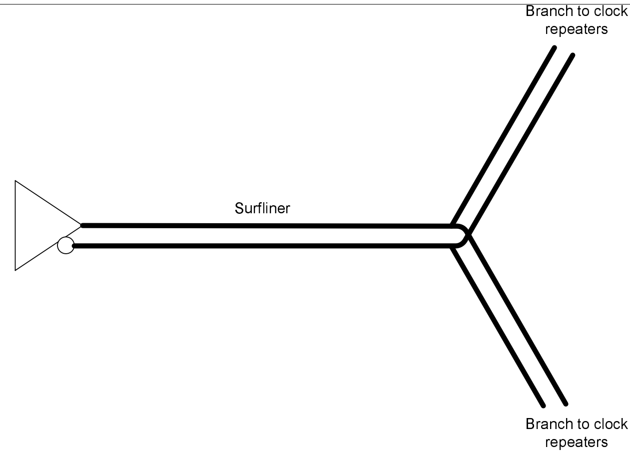
Inductance Diminishes Shunt Effects



- 0.5um wide 1.2 cm long copper wire
- Input skew 20ps

f(GHz)	*0.5*	*1*	*1.5*	*2*	*3*	*3.5*	*4*	*5*
skew(ps)	*3.9*	*4.2*	*5.8*	*7.5*	*9.9*	*13*	*17*	*26*

Clock Distributions



Surfliner

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Functional Modules (Data Path)

- *Arithmetic*
- *Algorithms*
- *Logic*
- *Logic Styles*
- *Placement*

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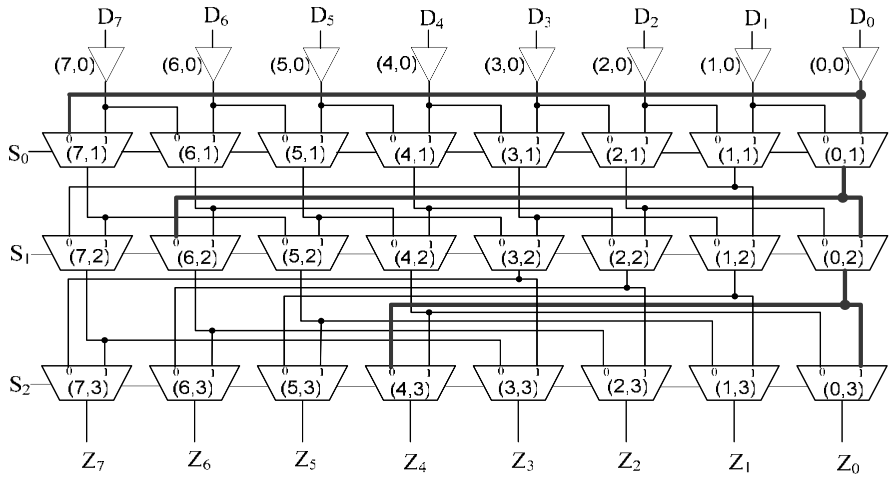
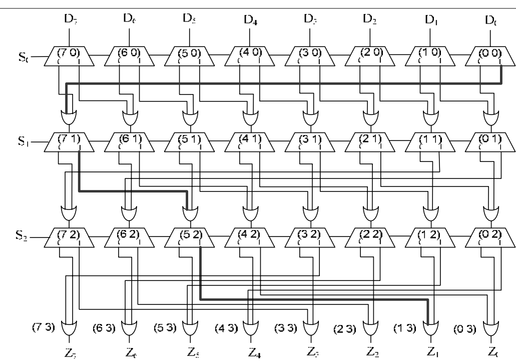
Cyclic Shifter

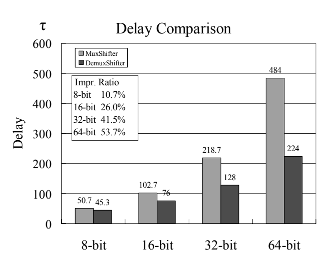
Delay: nlogn, Power: ¼ n^2

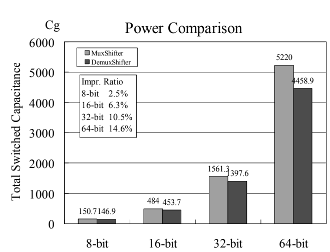


Fan-out Splitting



Delay: n
Power: 3/16 n^2

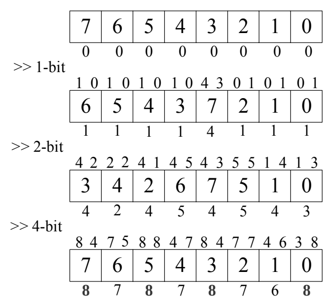




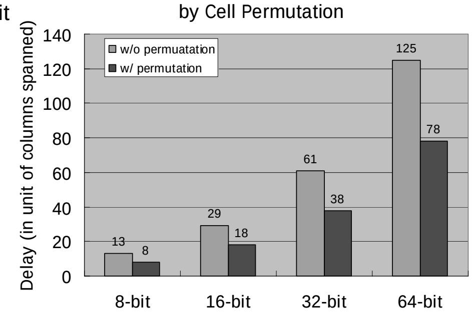
Cell Permutation

- *Fix the input/output stage, permute cells of intermediate stages to further improve delay.*
- *Formulate as an ILP problem and solve by CPLEX.*
  - *Optimal solution in terms of delay*
  - *Delay/Power tradeoff*

Optimal Timing solution for 8-bit



Additional Delay Reduction by Cell Permutation



Conclusion

- *Interconnect Technologies*
- *Geometrical Planning*
- *Interconnect Networks*
- *Power and Clock Distributions*
- *Functional Modules*

Interconnect Technologies

Example: w= 85nm, t= 145nm

r_n= 10Kohm,c_n=0.25fF,c_g=2.34xc_n=0.585fF
r_w=2ohm/um, c_w=0.2fF/um

Optimal interval

$$l = \sqrt{\frac{2(1+f)r_n c_g}{r_w c_w}} \approx 242\mu m$$

Optimal buffer size

$$s = \sqrt{\frac{r_n c_w}{r_w c_g}} \approx 41$$

Optimal delay

$$Delay(l_{tr})/l_{tr} = (2+\sqrt{2(1+f)})\sqrt{r_n r_w c_g c_w} \approx 194\, fs/\mu m = 194\, ps/mm$$

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Experiments—Optimized Skew

total area	skew		
	s-mesh(s)	m-mesh(s)	ratio
0.00	2.92E-11	2.92E-11	100.0%
0.25	2.79E-11	2.60E-11	93.2%
0.40	2.71E-11	2.45E-11	90.4%
1.00	2.42E-11	1.98E-11	81.8%
3.00	1.70E-11	1.24E-11	73.2%
5.00	1.24E-11	8.72E-12	70.5%

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Robustness Against Supply Voltage Variations

total area	mutli-level mesh		single-level mesh	
	ave	worst	ave	worst
0.00	2.10E-11	2.91E-11	2.10E-11	2.91E-11
1.00	8.38E-12	1.14E-11	8.26E-12	1.43E-11
2.00	2.71E-12	4.42E-12	6.18E-12	1.11E-11
3.00	1.89E-12	3.33E-12	4.83E-12	8.73E-12
4.00	1.45E-12	2.48E-12	3.88E-12	6.96E-12
5.00	1.16E-12	2.02E-12	3.18E-12	5.64E-12