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Title: "**Layout Printability Verification and Physical Design Regularity: Roadmap Enablers for the next decade**"

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ABSTRACT:

The past decade has experienced a remarkable synergy between Resolution Enhancement Technologies (RET) in Optical Lithography and Optical Proximity Correction (OPC). This heterogeneous array of patterning solutions ranges from simple rule-based to more sophisticated model-based corrections, including sub-resolution assist features, partially transmitting masks and various dual mask approaches.
A survey of the evolutionary development from the early introduction of the first OPC engines in 1996 to the debut of Immersion Lithography in 2006 reveals that the convergence of RET and OPC has also enabled a progressive selection and fine-tuning of Geometric Design Rules (GDR) at each technology node, based on systematic adoption of lithographic verification.
This paper describes the use of "full-chip" lithography verification engines in current Design For Manufacturing (DFM) practices and extends the analysis to identify a set of key technologies and applications for the 45, 32 and 22 nm nodes.
A major paradigm shift in Optical Lithography has been achieved by the integration of fast optical and resists simulators within a geometric verification environment. OPC production requirements for accuracy and predictability, for 90 and 65 nm, across a wide range of layout configurations, coupled with software flexibility and extensibility through embedded scripting (Tcl, Perl, Python, etc.) allow for the implementation of novel family of verification and yield-enhancement techniques. For example, Parametric Test Patterns, i.e. programmable layout instantiations, are used for both validation of GDR and, most importantly, for identification of process-window limiters (in conjunction with specific RET and OPC selections).
As OPC-derived tools enter the stage of maturity, from a software standpoint, their use-model is being greatly broadened from the back-end mask tape-out flow, upstream directly integrated into physical design verification. While "classical" optical lithography simulations can readily identify the fundamental 1-D pitch limiter for a given technology, the grand challenge for the next 3 nodes (down to the physical scaling limit of the CMOS device) is represented by the 2-D layout configurations which must be patterned. The inherent practical impossibility of defining all possible "forbidden 2-D design rules" in the standard form of sets of geometric constraints requires the additional step of (lithography-driven) DFM-closure.
Lithography awareness into the physical design environment, mediated by these new DFM verification tools and flows, is driving various forms of manufacturable physical layout implementation: from Restricted Design Rules and Flexible Design Rules to Regular Circuit Fabrics. As new lithography solutions, such as immersion lithography and EUV, will have to be deployed within a complex technology framework, the paper also examines the trend towards "layout design regularization" and its implications for patterning and next generation lithographies.