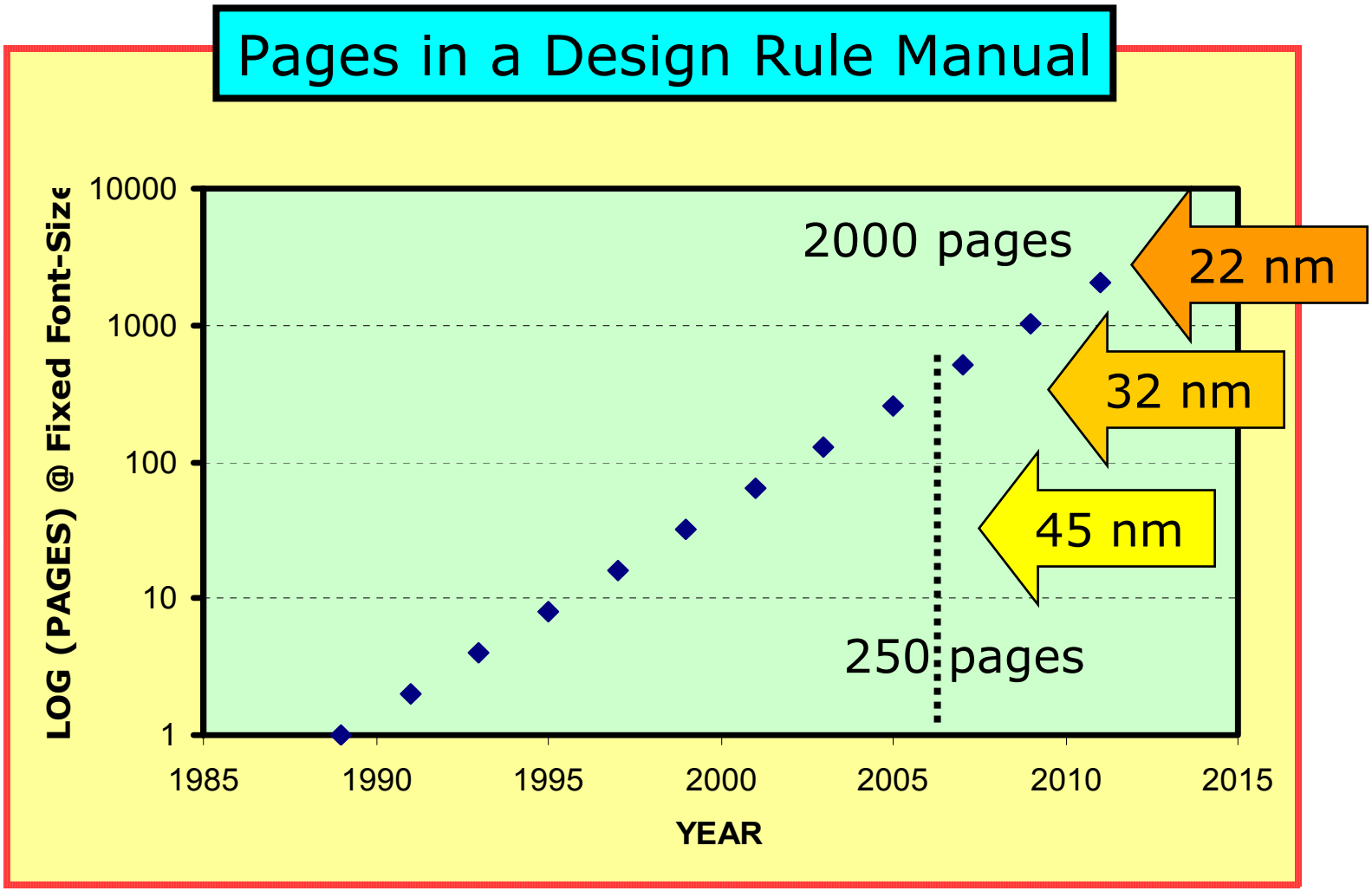
AMD

Layout Printability Verification and Physical Design Regularity: Roadmap Enablers for the next decade

Luigi Capodieci, Ph.D.

The "real" Technology Roadmap



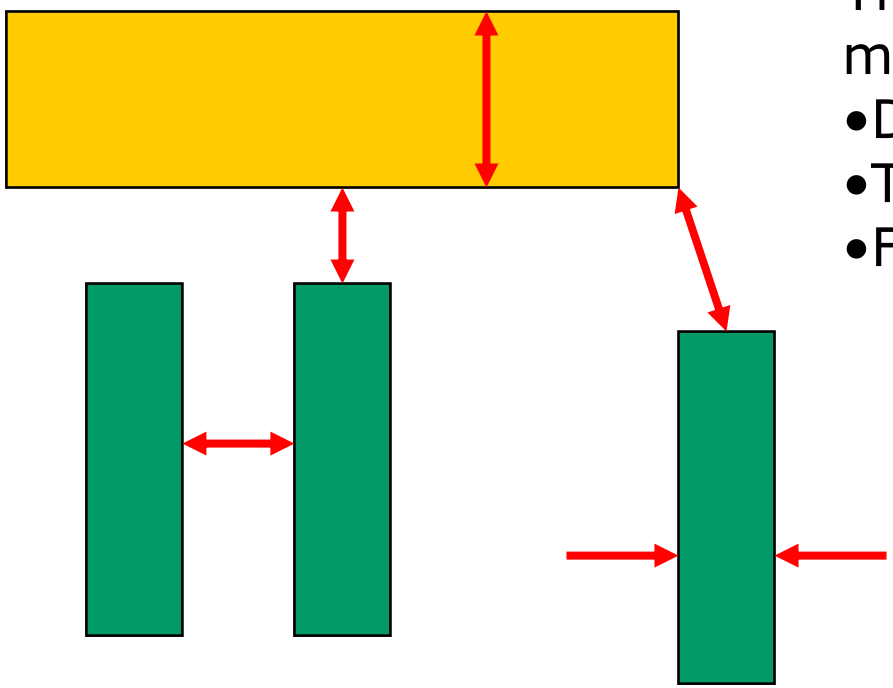
Outline

- A brief history of DFM
- Yield and Design Rules at 45, 32 and 22 nm
- Design For Manufacturing (DFM)
  - Layout Printability Verification (across PW)
- Holistic Design Rules Selection/Optimization
- Towards Design Layout Regularity
- Layout Analysis by Pattern Matching
- Conclusions: enabling 45 nm and below

A Brief (Evolutionary) History of DFM [I]

- Traditional Design Rules

  Set of **geometrical constraints**, necessary to guarantee yield, defined over polygonal shapes and edges in the layout



The Design Rule Manual mediates among:

- DESIGN
- TECHNOLOGY
- FAB

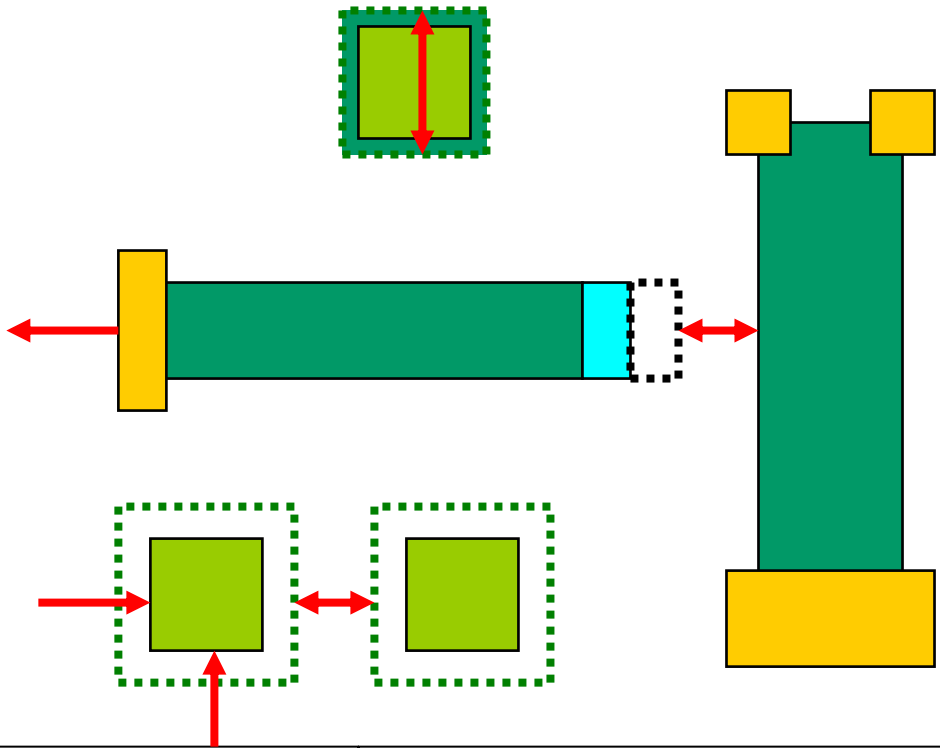
Two Types of DR:

1. Restrictive
2. Prescriptive

250nm, 180 nm, …

A Brief (Evolutionary) History of DFM [II]

- Rule-Based Optical Proximity Correction
  - **Tables** of "corrections" (edge movements, polygon addition and subtraction) to pre-compensate for fabrication effects and distortions, functions of (**DISTANCE** and **SIZE**)

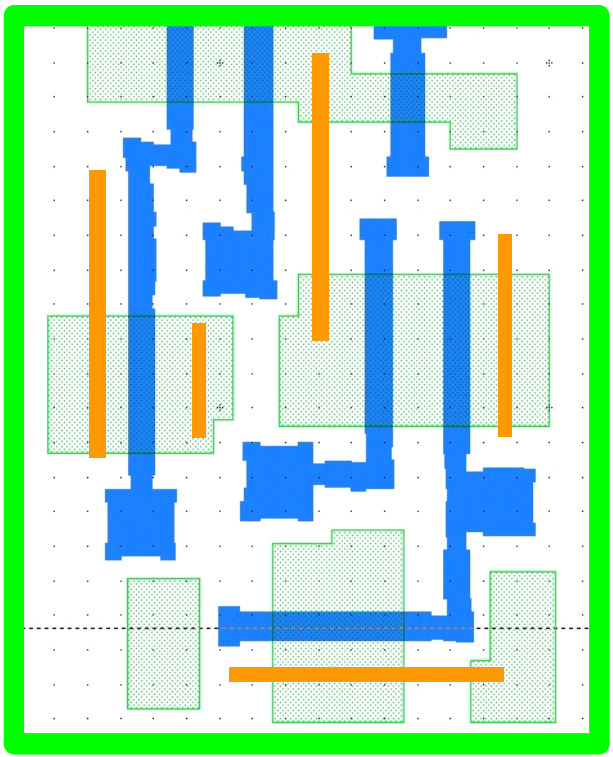


Although NOT coded in the Design Rule Manual RB-OPC is conceptually analogous to Design Rules and also implemented using **same** DRC engines

180 nm, 130 nm, …

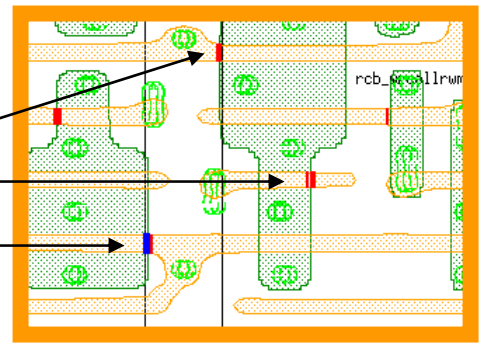
A Brief (Evolutionary) History of DFM [III]

- Model-Based Optical Proximity Correction



(1) - Edge Fragmentation/Segmentation
(2) - Iteratively:
(3) – Local Process Simulation
(4) - Edge Movement (Correction)
(5) – Evaluate Edge Placement Error(s)

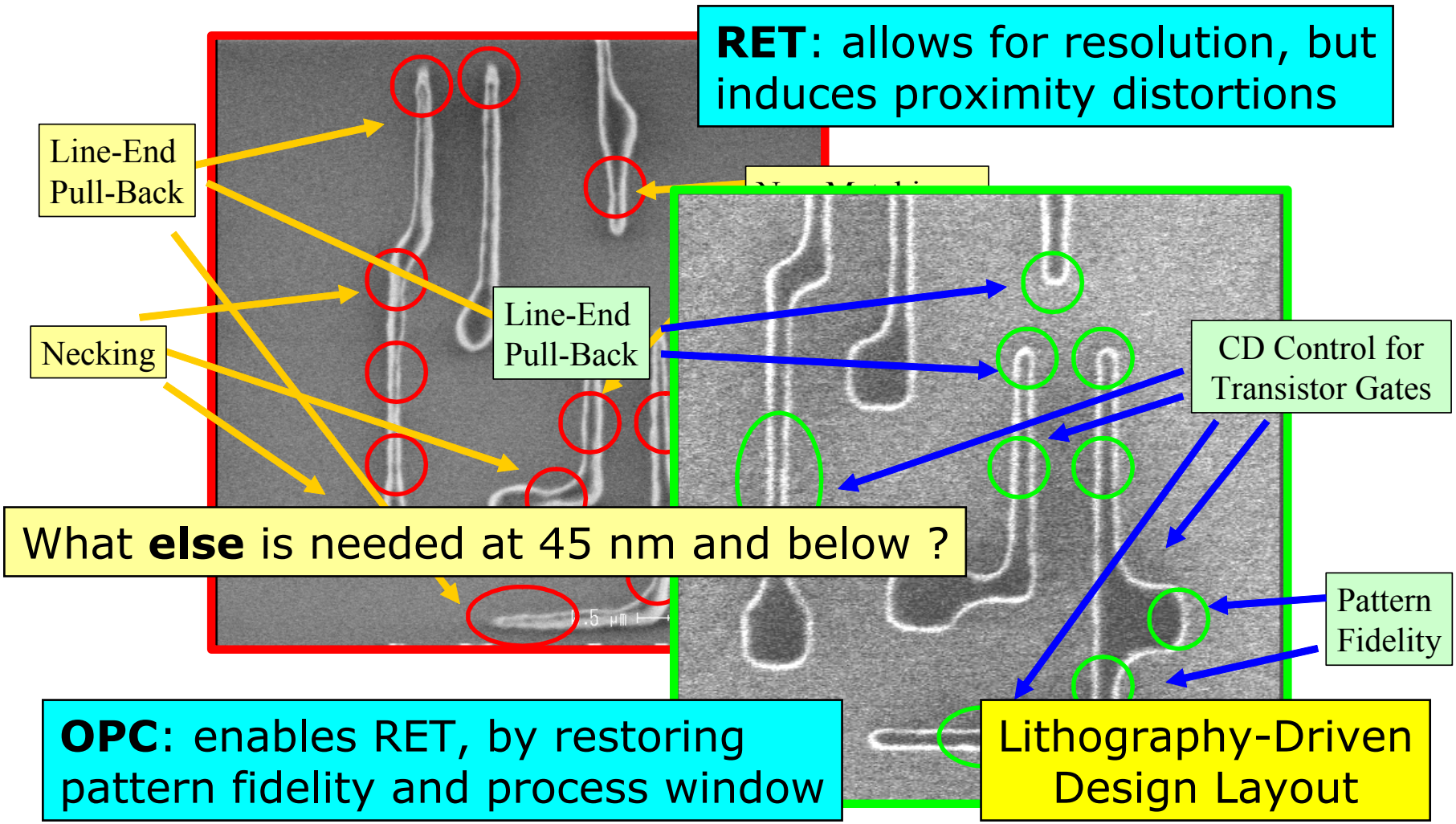
Both Model Based
And Rule-Based
(geometrical) Checks



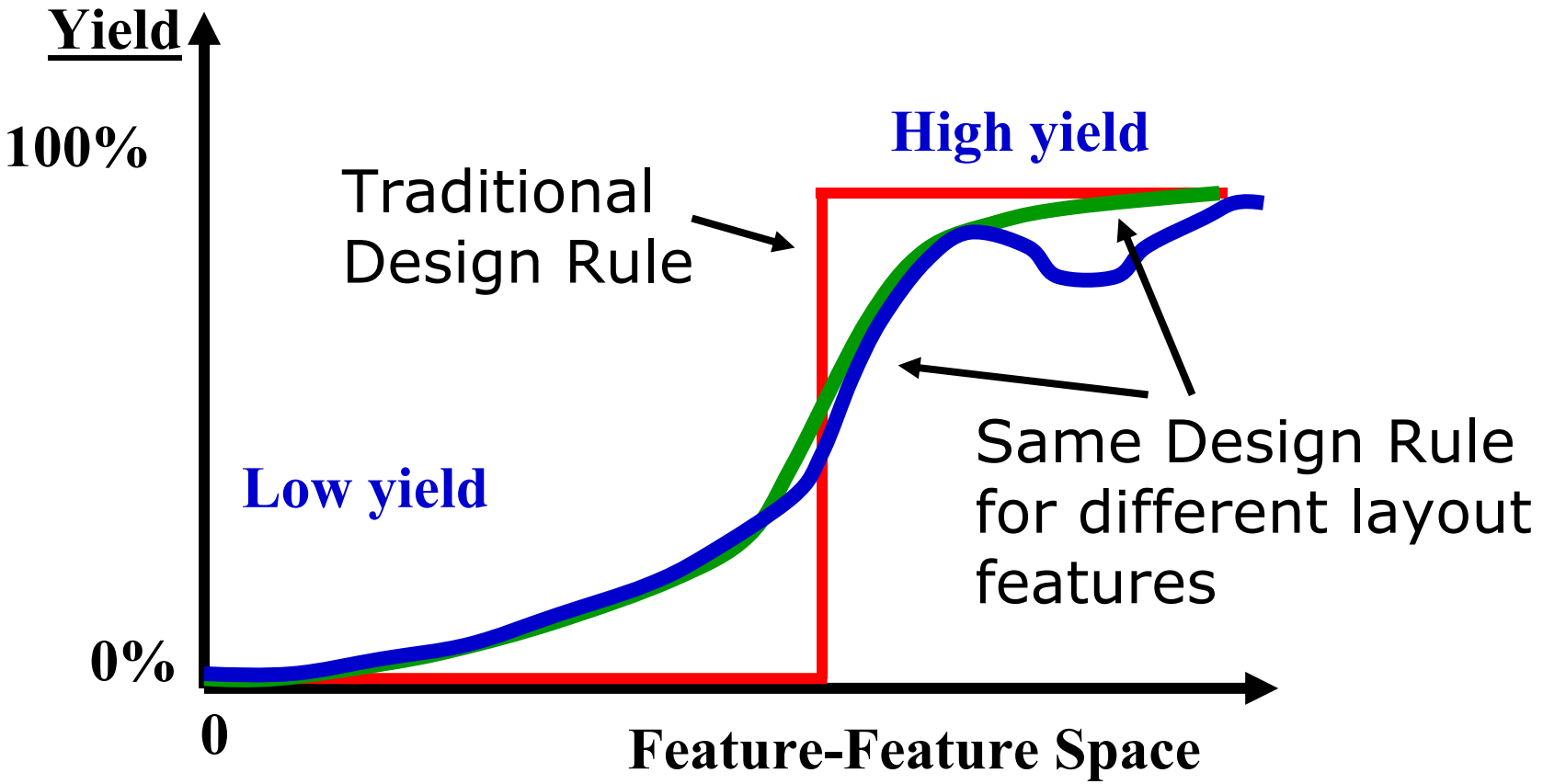
130 nm, **90 nm**, 65 nm …

ENABLER:
Layout Printability Verification

(DR) + RET + (RB-OPC) + (MB-OPC) + [?]

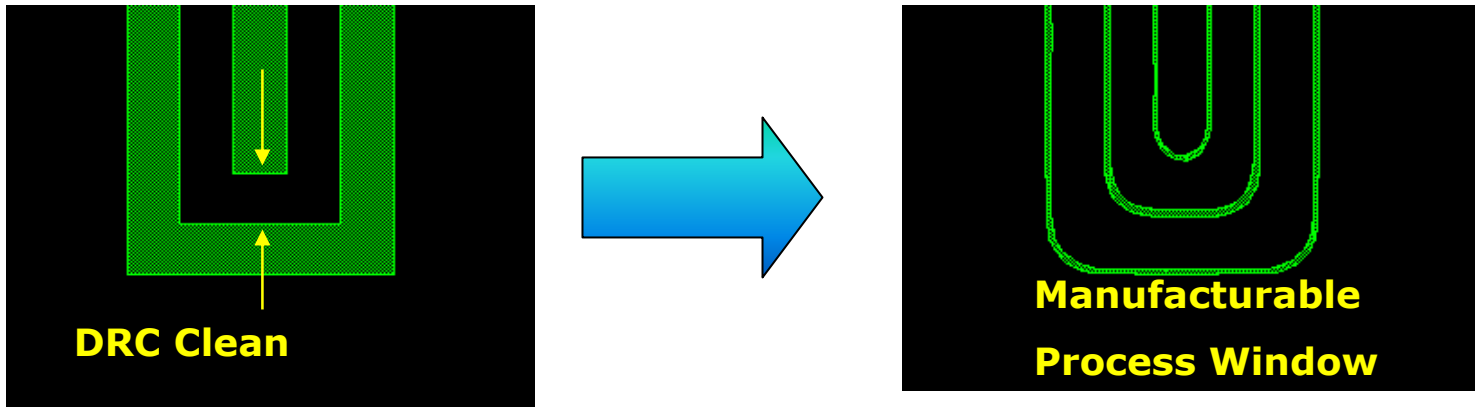


Yield vs. Design Rules at 45, 32 and 22 nm

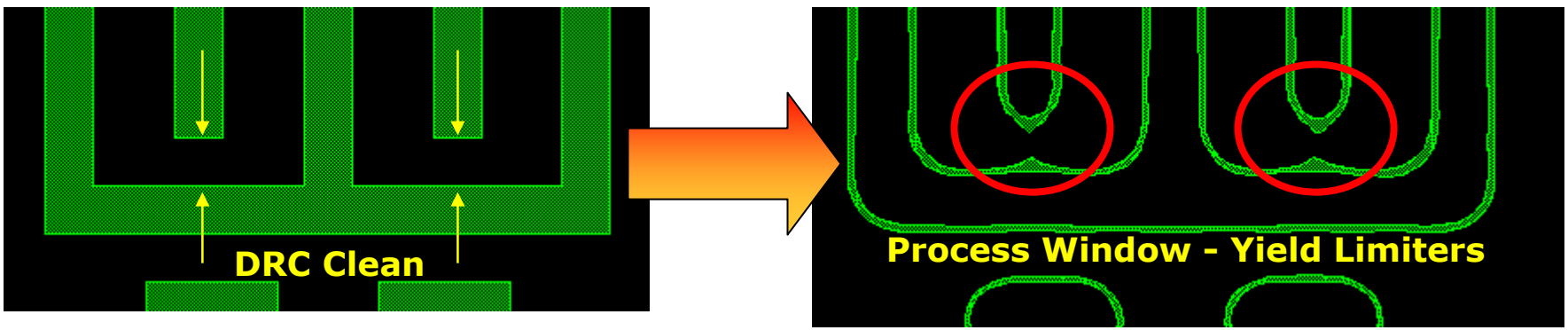


Courtesy of Kevin Lucas (Freescale)

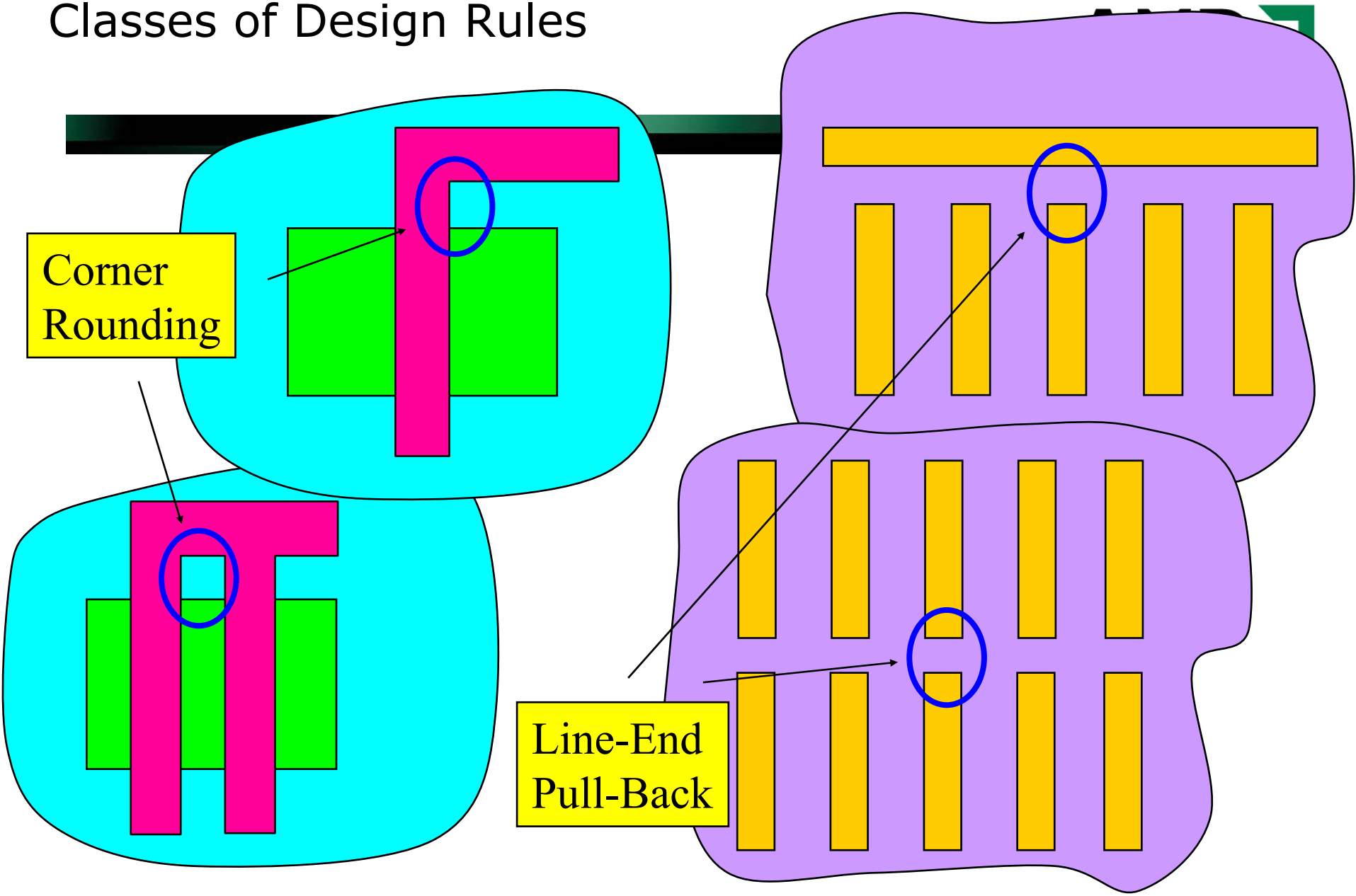
Yield vs. Design Rules at 45, 32 and 22 nm



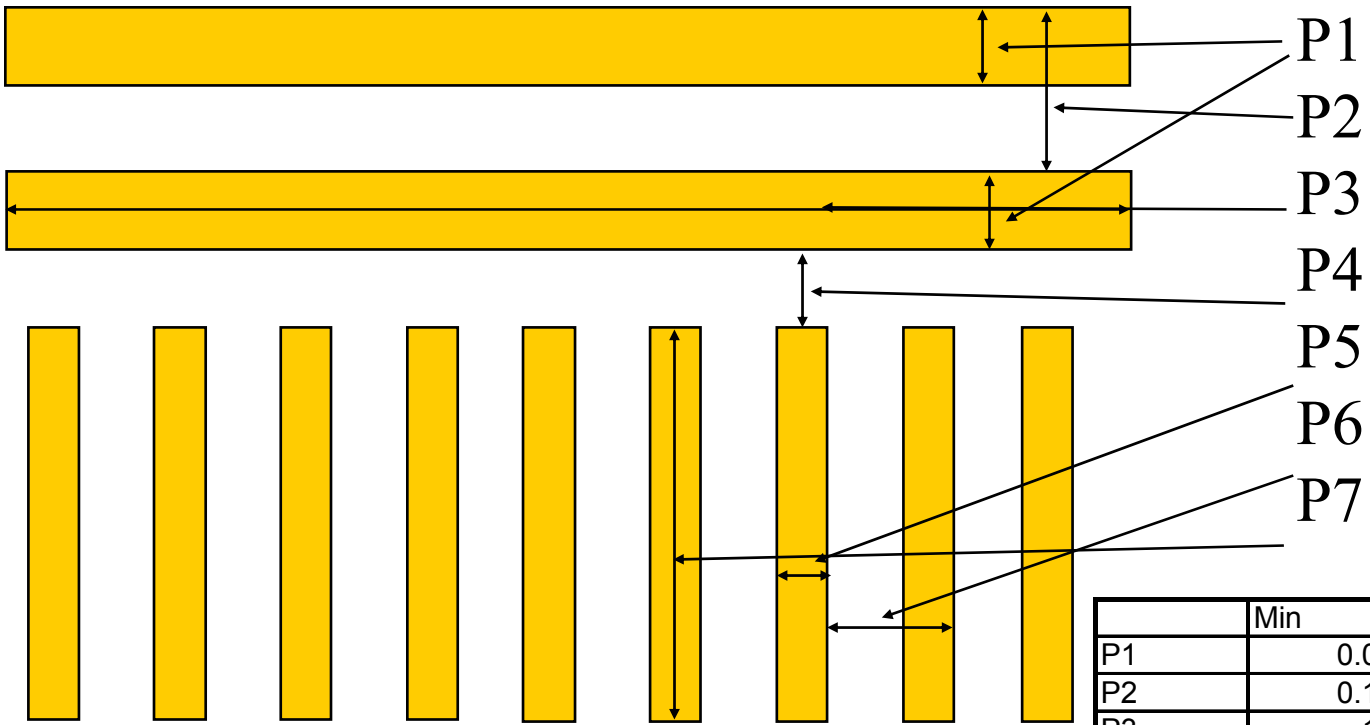
Design-Rules Compliance does NOT guarantee Yield due to: Non-Linearity Effects Induced by Sub-Wavelength Fabrication. Furthermore OPC cannot fix all Yield Limiters configurations



Classes of Design Rules



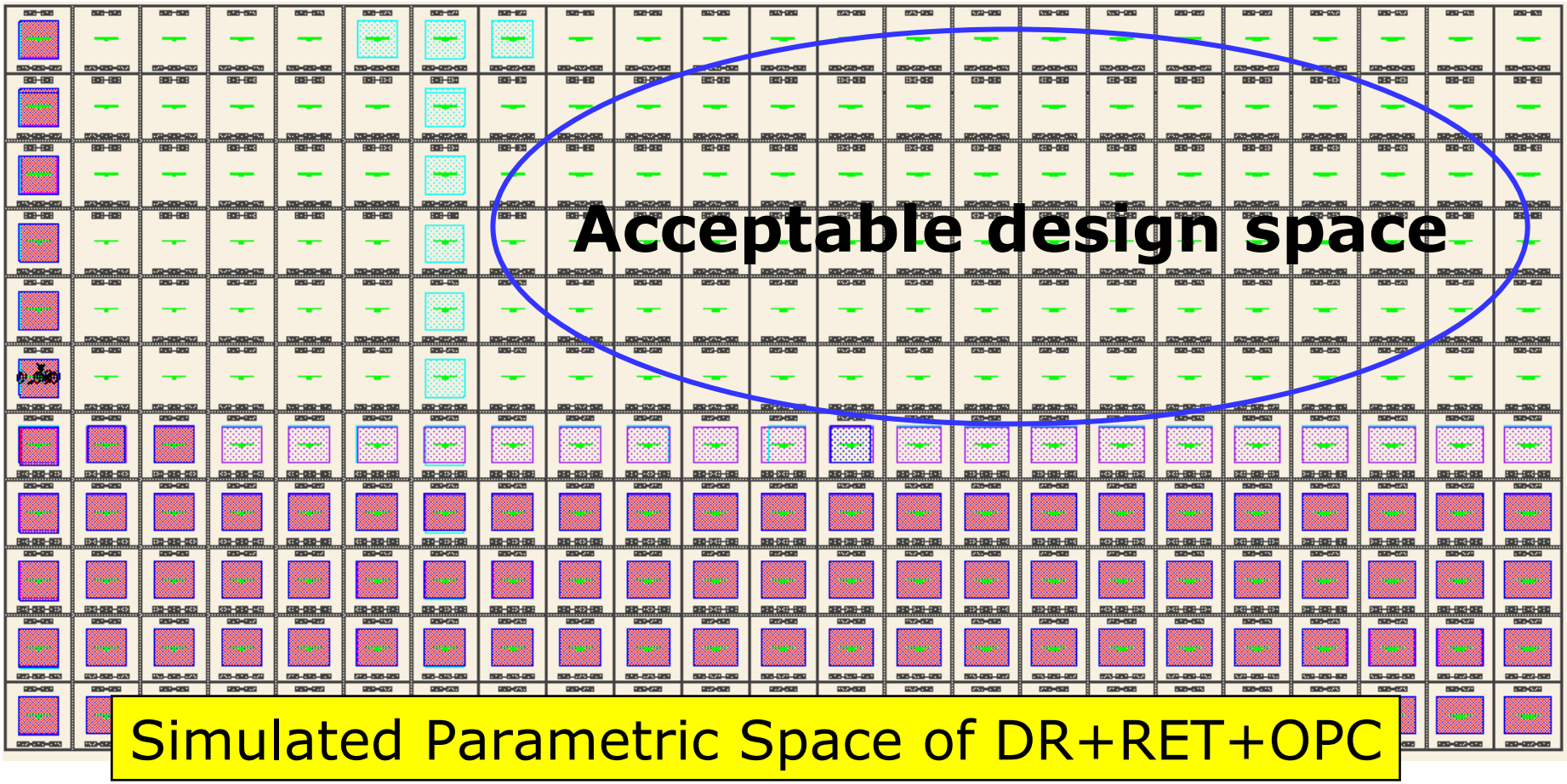
DFM Optimization of Design Rules [I]



	Min	Max	Step	n
P1	0.08	0.16	0.04	3
P2	0.18	0.45	0.09	4
P3	10	10	0.01	1
P4	0.04	0.14	0.01	11
P5	0.08	0.12	0.01	5
P6	0.16	0.6	0.02	23
P7	1	1	0.1	1
Total				15180

Definition of
Parametric Design Rule

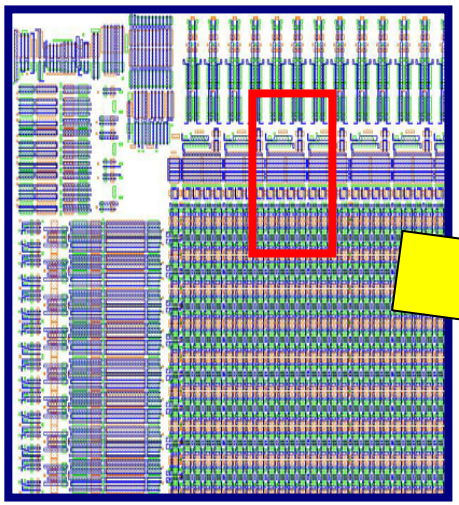
DFM Optimization of Design Rules [II]

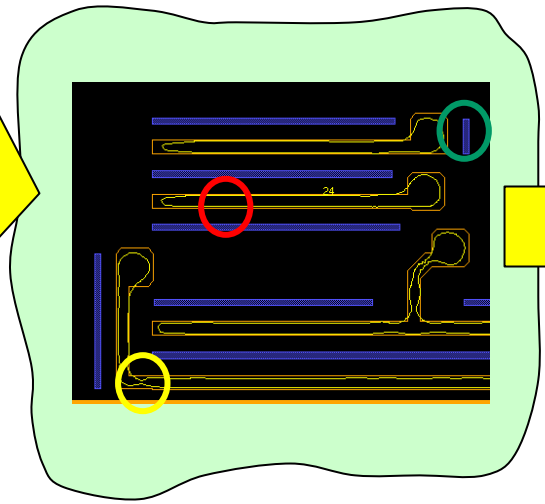


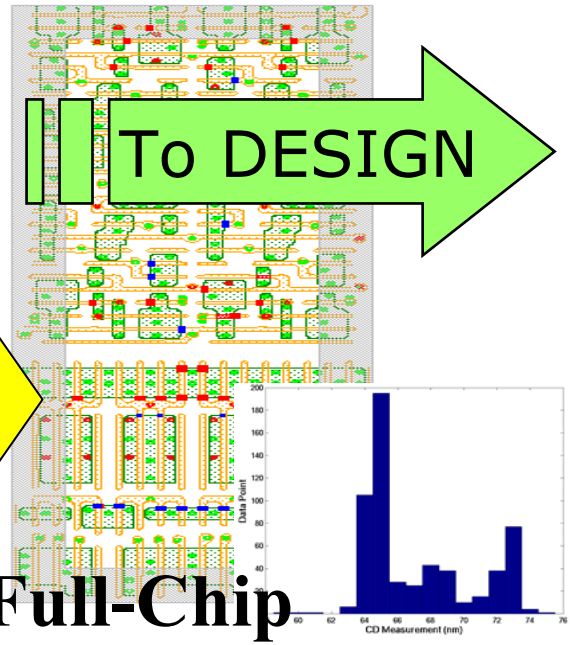
DFM Fundamental Building Block

Si-Calibrated

Process Simulator







Design Layout (GDSII/OASIS)

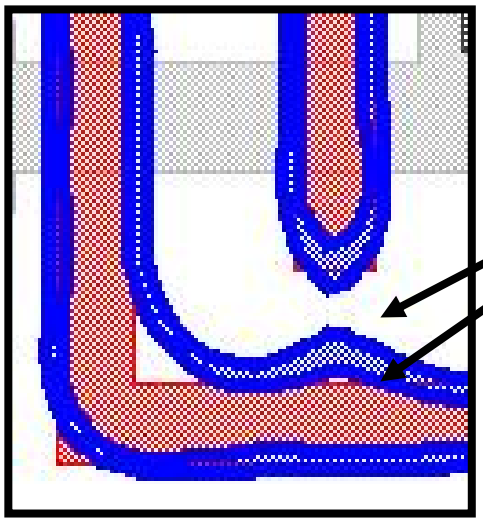
Full-Chip

- **CD Error Map**
- **Statistical Count**

Integrated into a **verification** (DRC) software environment, with a suitable programming (or scripting) language

To FAB

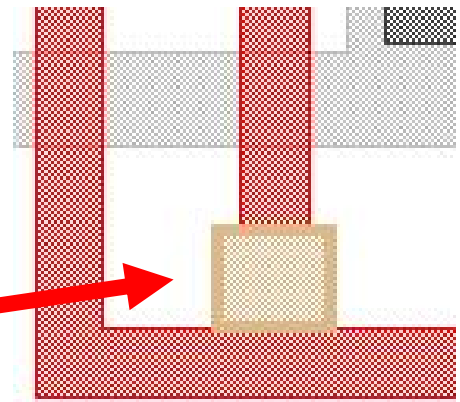
Layout Printability Verification



Process Variability Bands

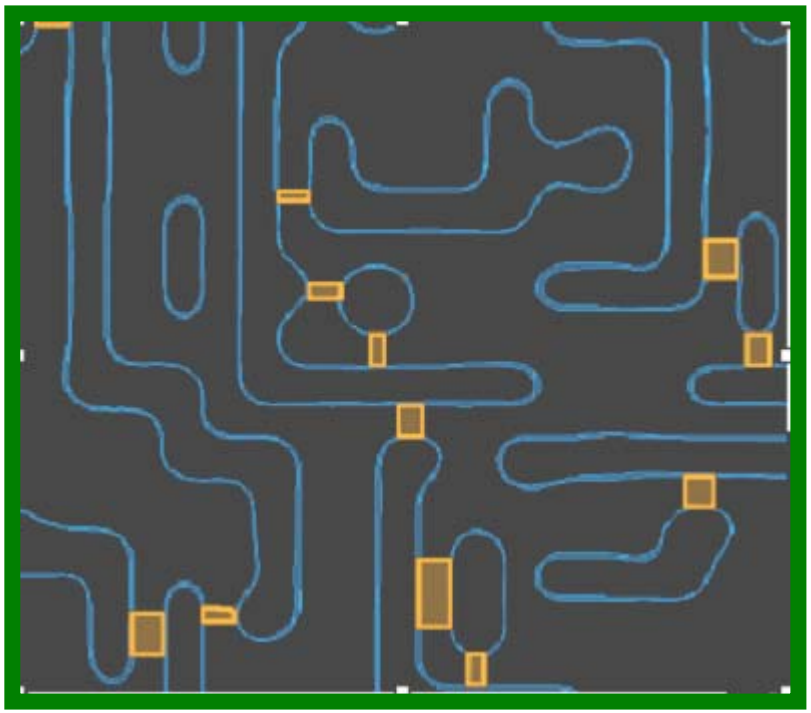
across Focus
and Exposure

Process Variability
Check/Flag

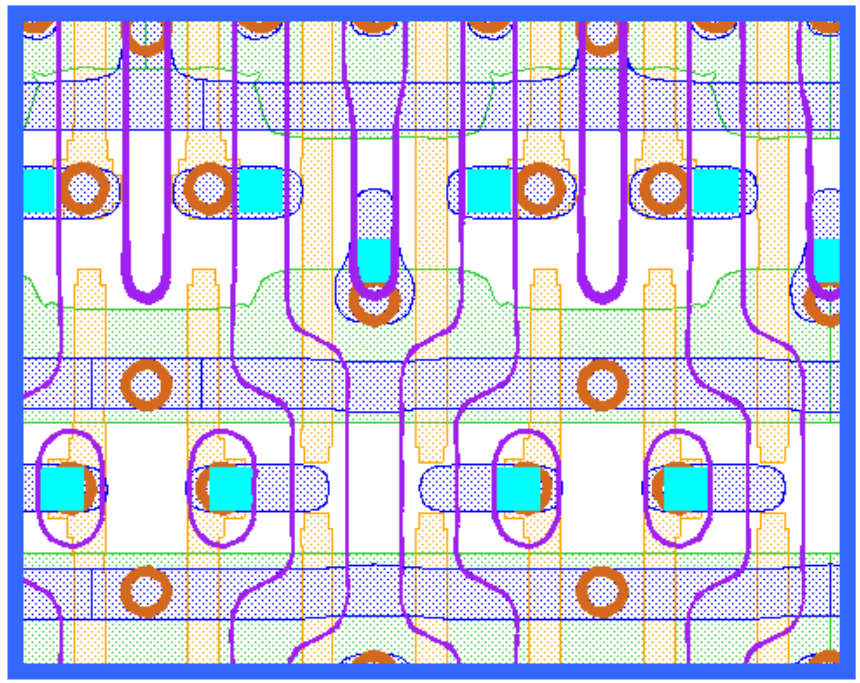


Potential
Yield Limiter

Lithography-Driven Layout Verification and Optimization



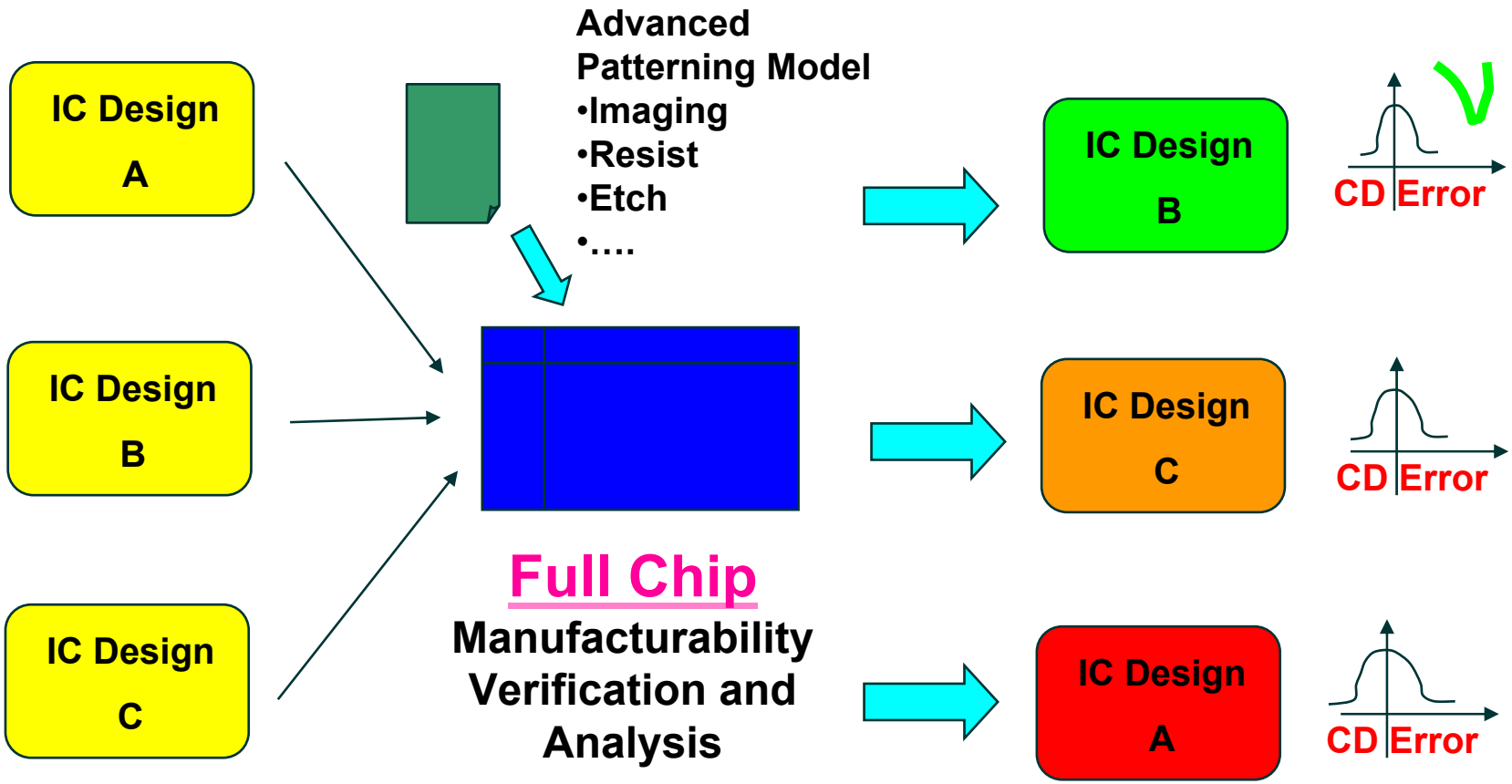
Single-Layer



Multi-Layer

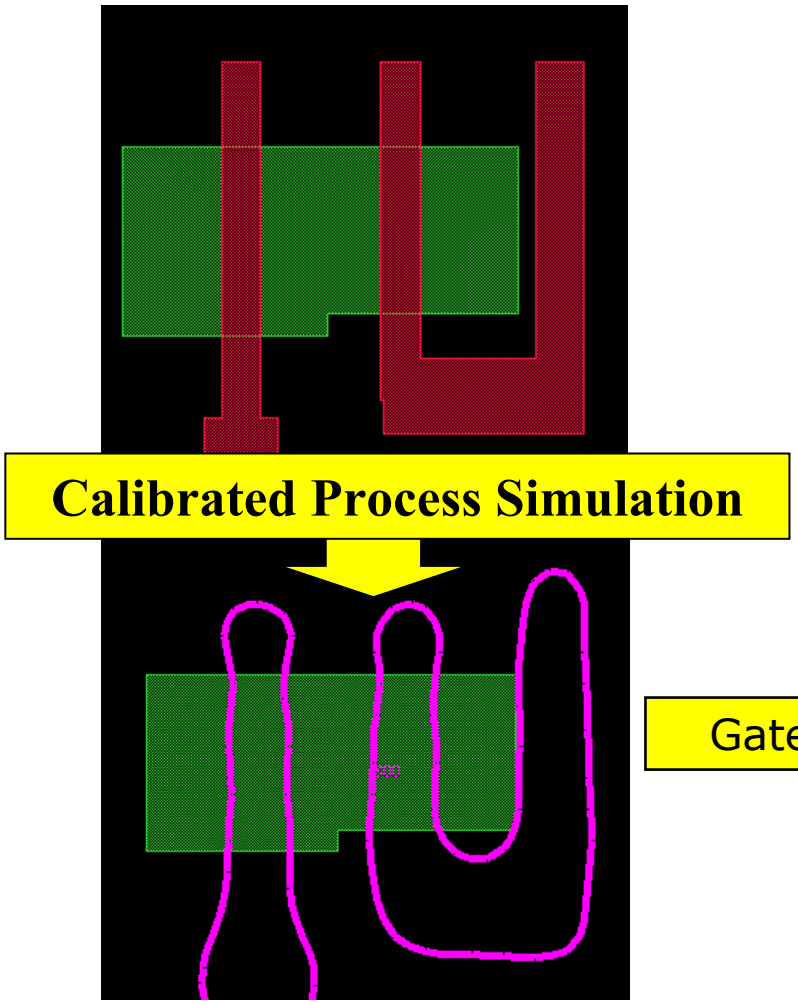
"Layout Verification and Optimization Based on Flexible Design Rules"
J. Yang, L. Capodieci [6156-09] – **Thursday at 2:10 PM**

DFM **Design Analysis** Application

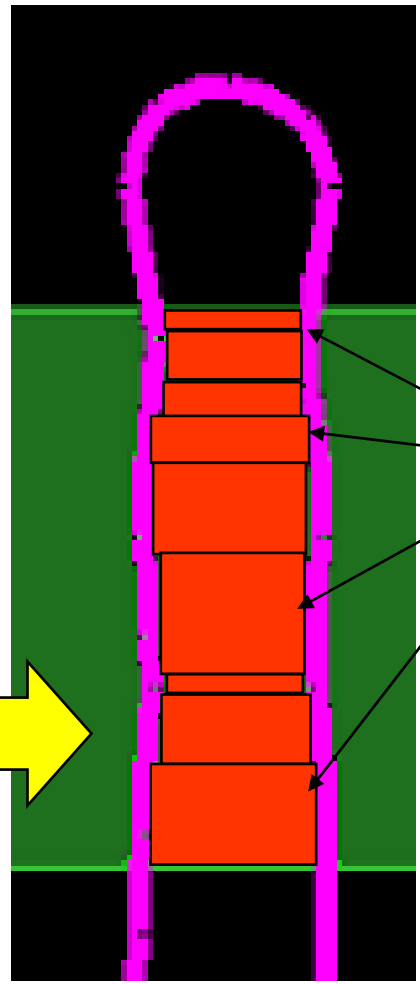


Design refers to Physical Layout and **also** Circuit

Advanced DFM Application: Modeling of **Non-Rectangular** Transistors



Gate



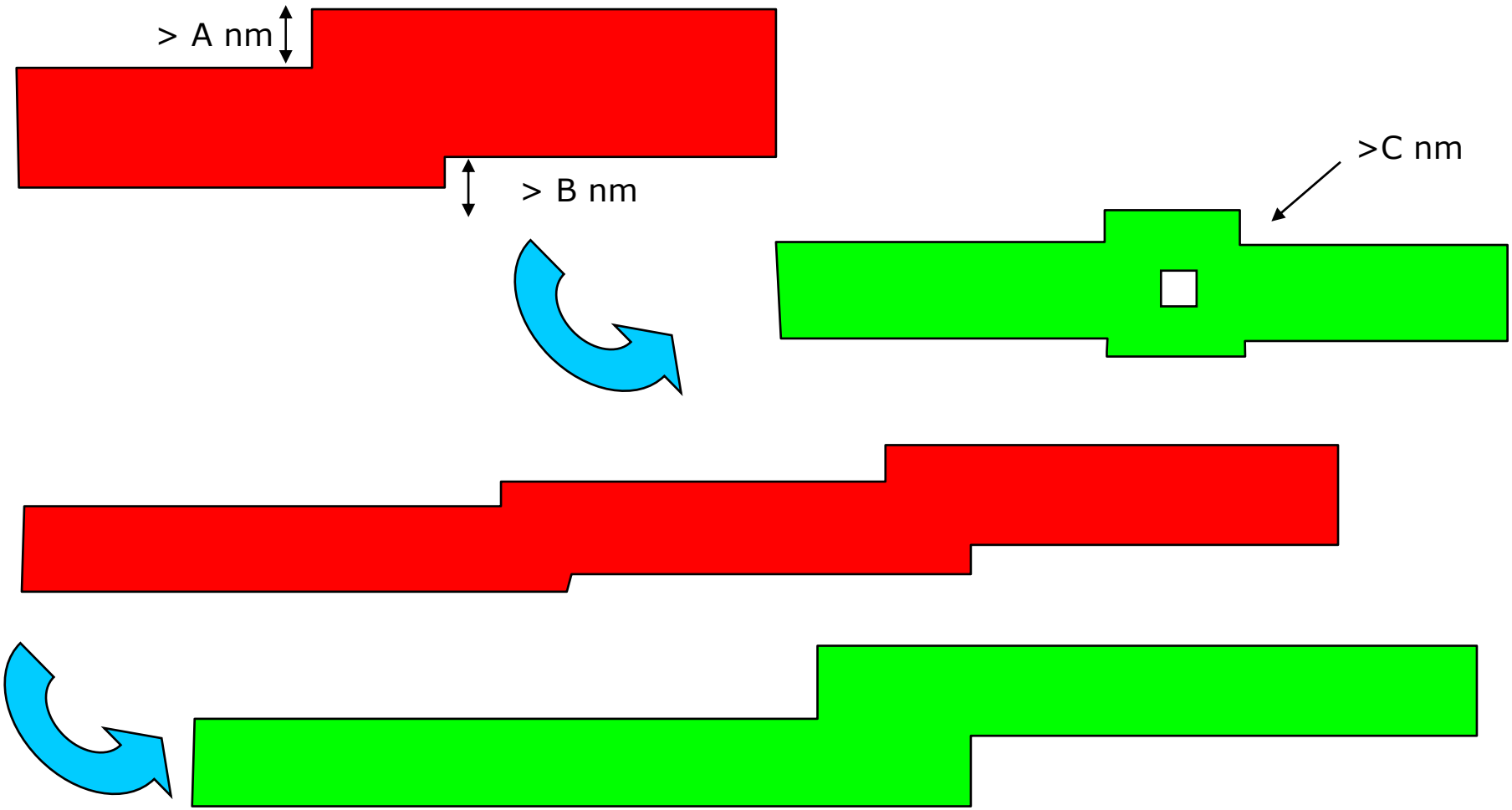
NEW DFM FLOW: Integrated Process Simulations with Transistor Models

BSIM models are generated for each rectangular slice.

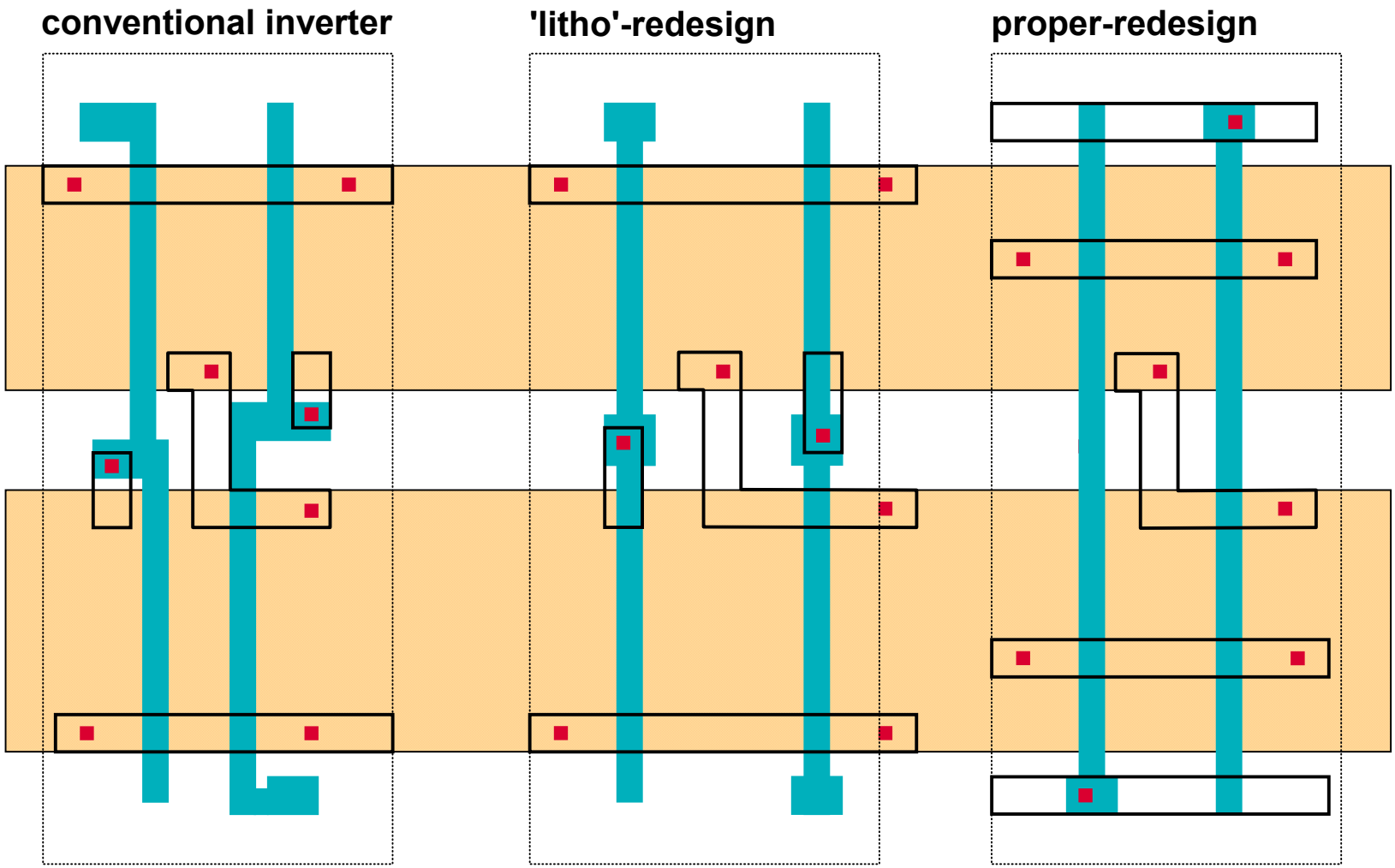
"From poly line to transistor: building BSIM models for non-rectangular transistors"

W. Poppe, L. Capodieci [6156-26] **SPIE 2006**

Design Layout Regularization (“manual”)

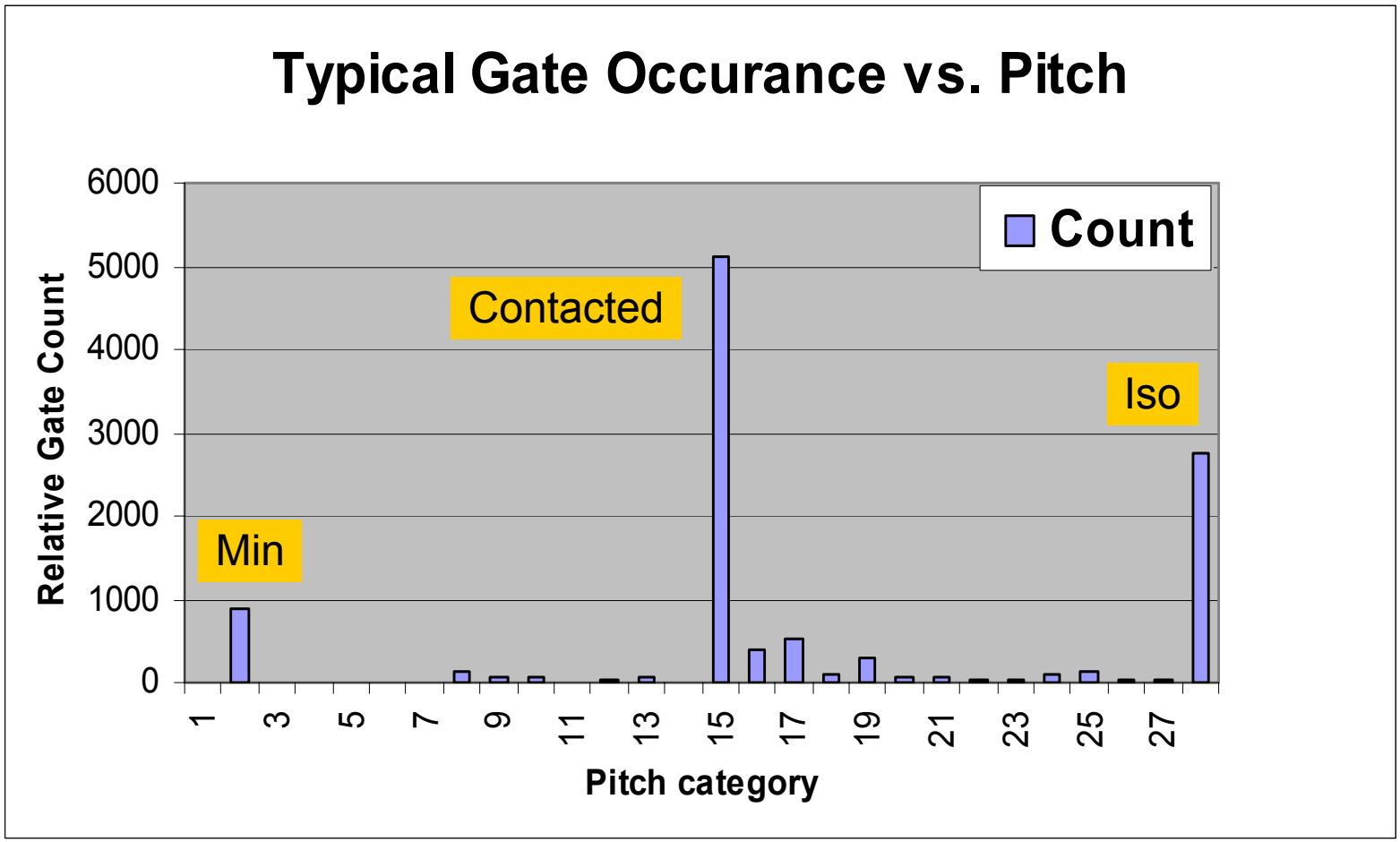


Layout Re-Design Trend (65nm to 45 nm)



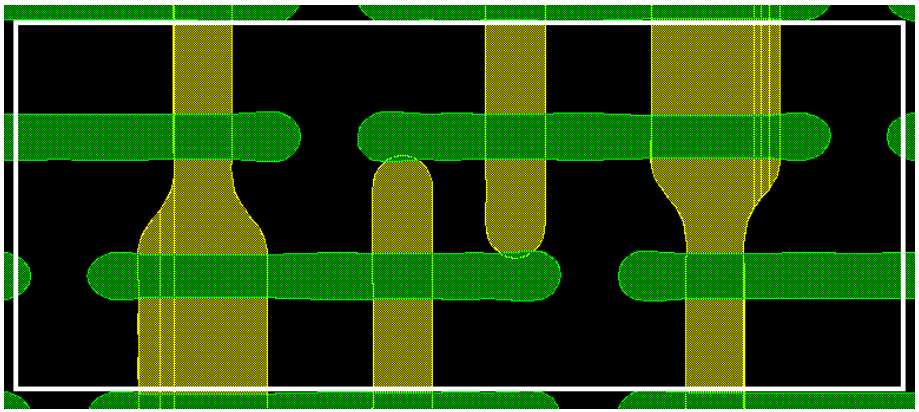
Courtesy: Lars Liebmann (IBM)

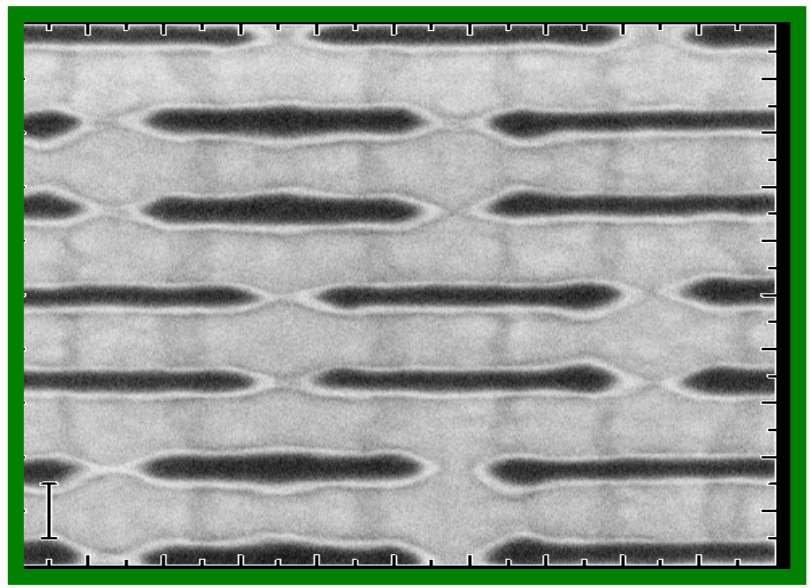
Gate Pitch Classification in Microprocessor Logic



Data Source: Kevin Lucas (Motorola/Freescale)

Regular Layouts and Piecewise Patterning

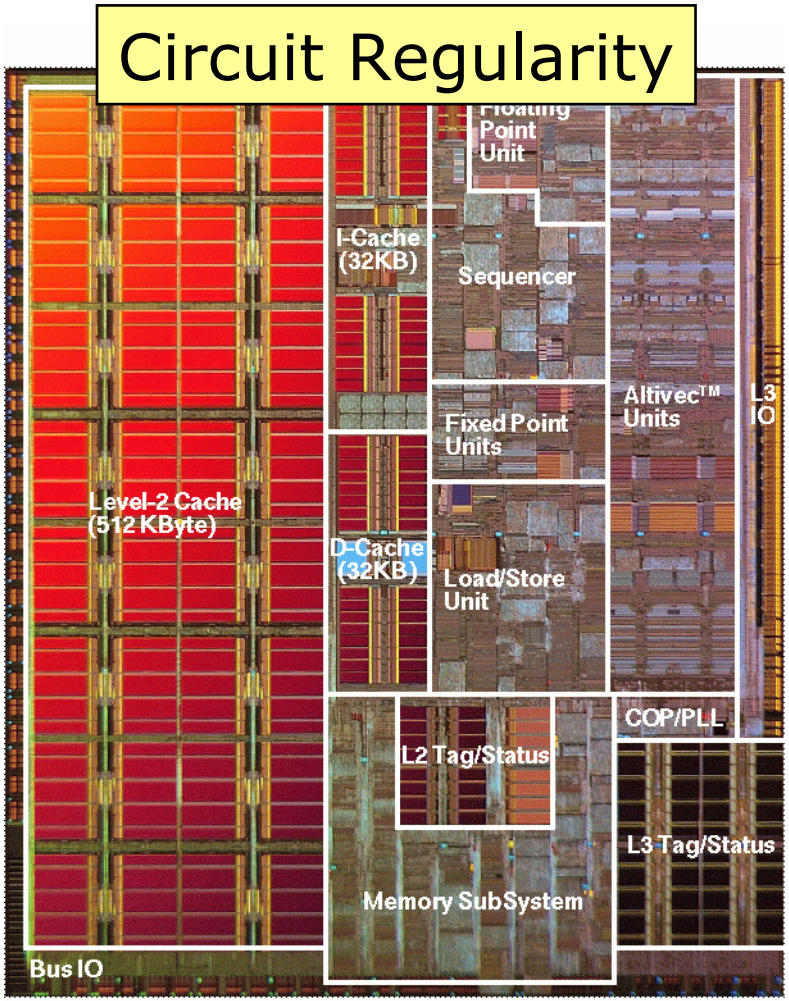


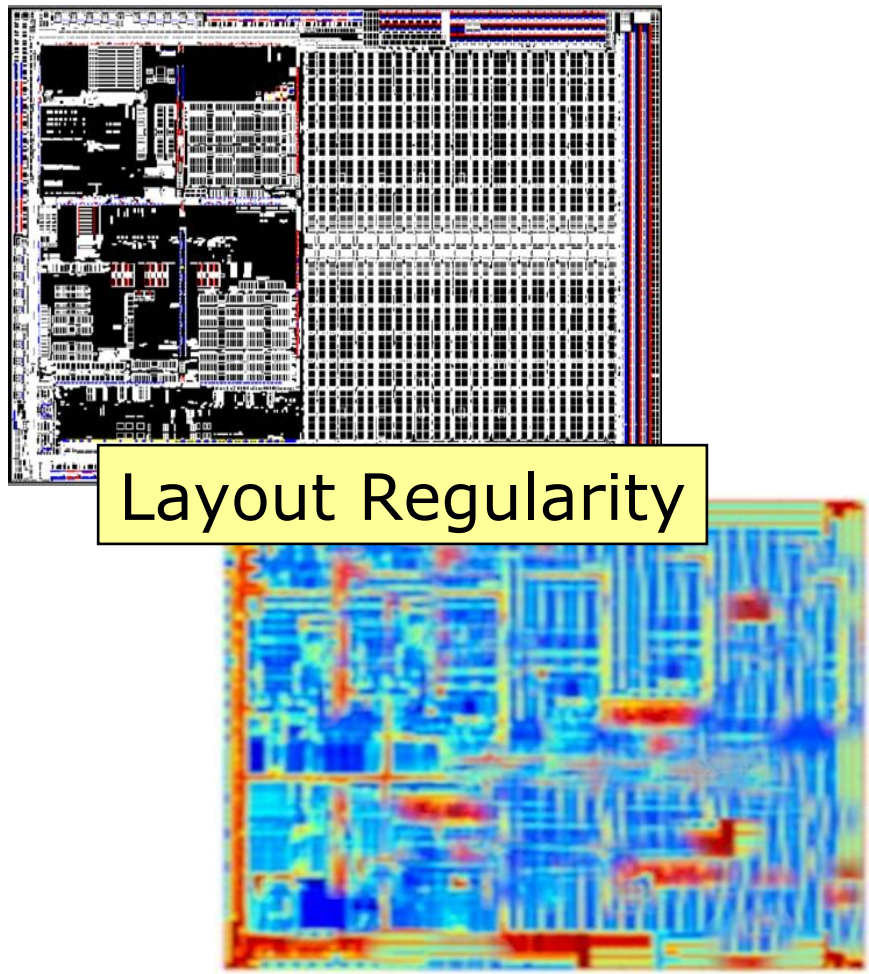


Regular Layouts are needed (enable) piecewise patterning (e.g. dual-mask)

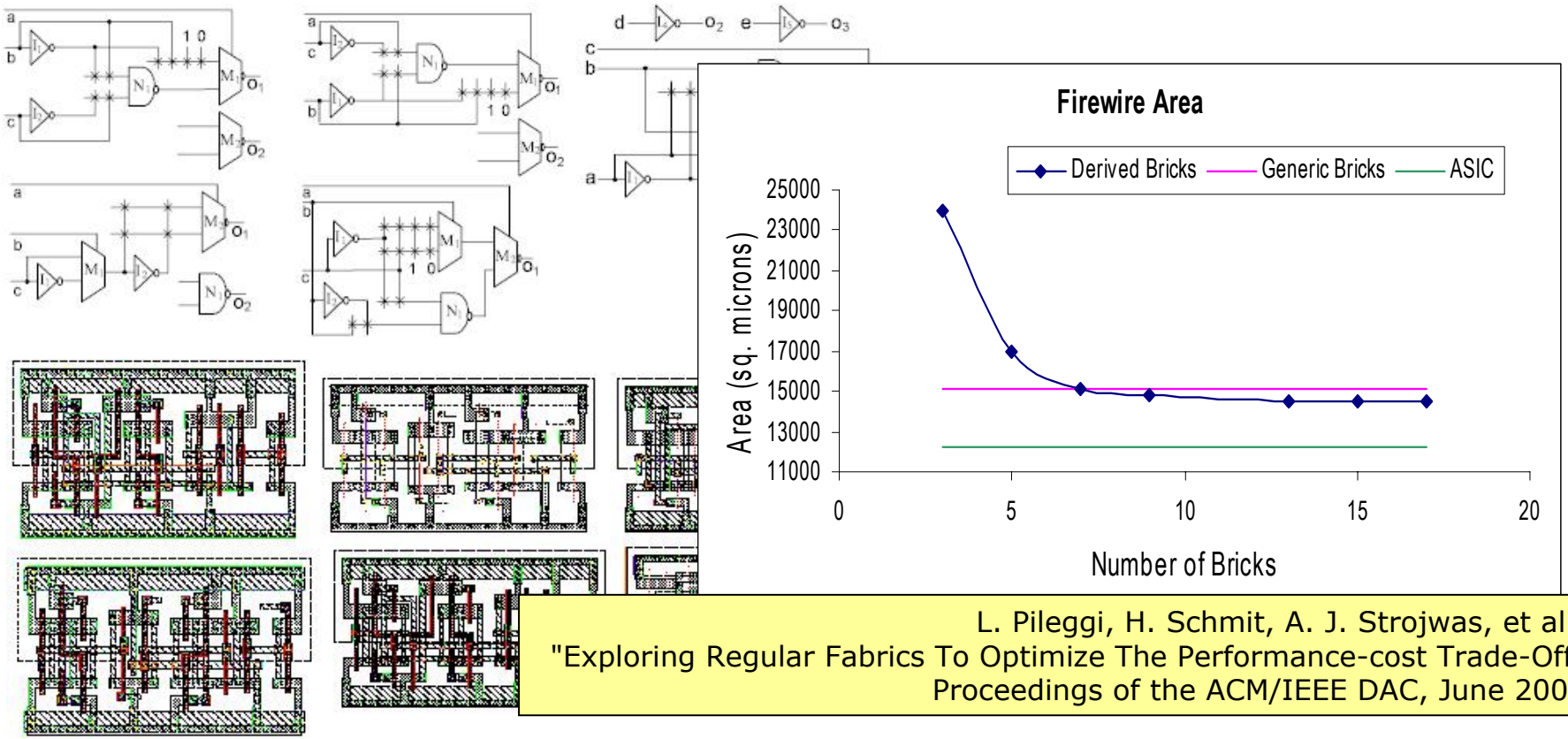
Manufacturability Constraint:
Layer to Layer Alignment

Regularity in Integrated Devices





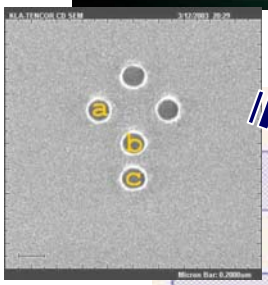
Regular Circuit Fabrics: Generic, Fixed-Size Configurable Bricks



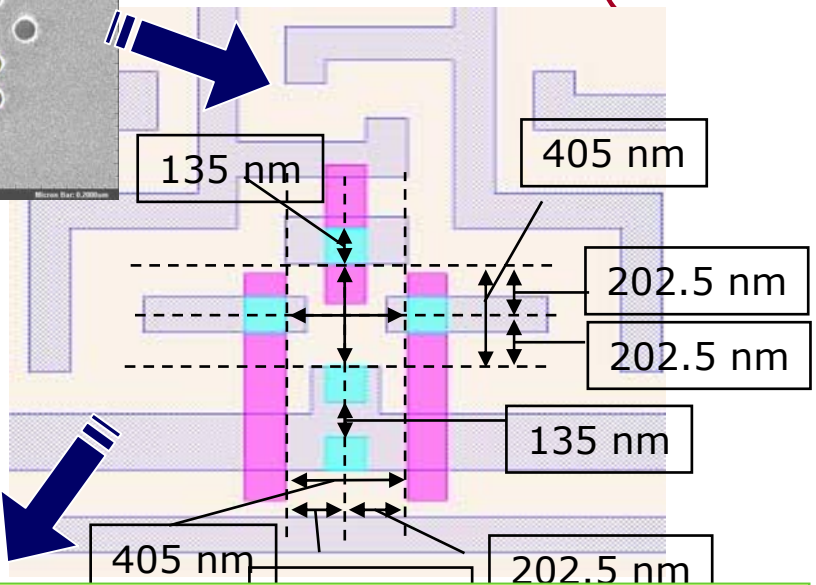
L. Pileggi, H. Schmit, A. J. Strojwas, et al.,
"Exploring Regular Fabrics To Optimize The Performance-cost Trade-Off"
Proceedings of the ACM/IEEE DAC, June 2003

V. Kheterpal, V. Rovner, T.G. Hersan, D. Motiani, Y. Takegawa, A.J. Strojwas, L. Pileggi
"Design Methodology for IC Manufacturability Based on Regular Logic-Bricks"
Proceedings of the ACM/IEEE DAC, June 2005

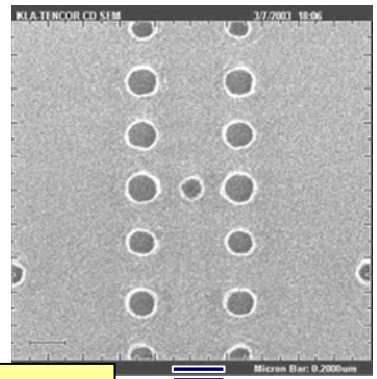
2D Image-Based Design Rule Checks



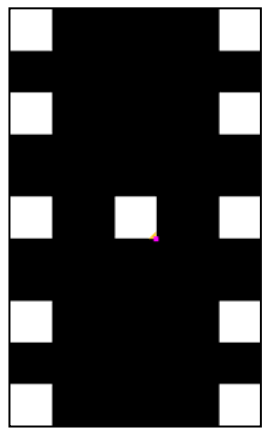
Traditional DRC (Hard-Coded)



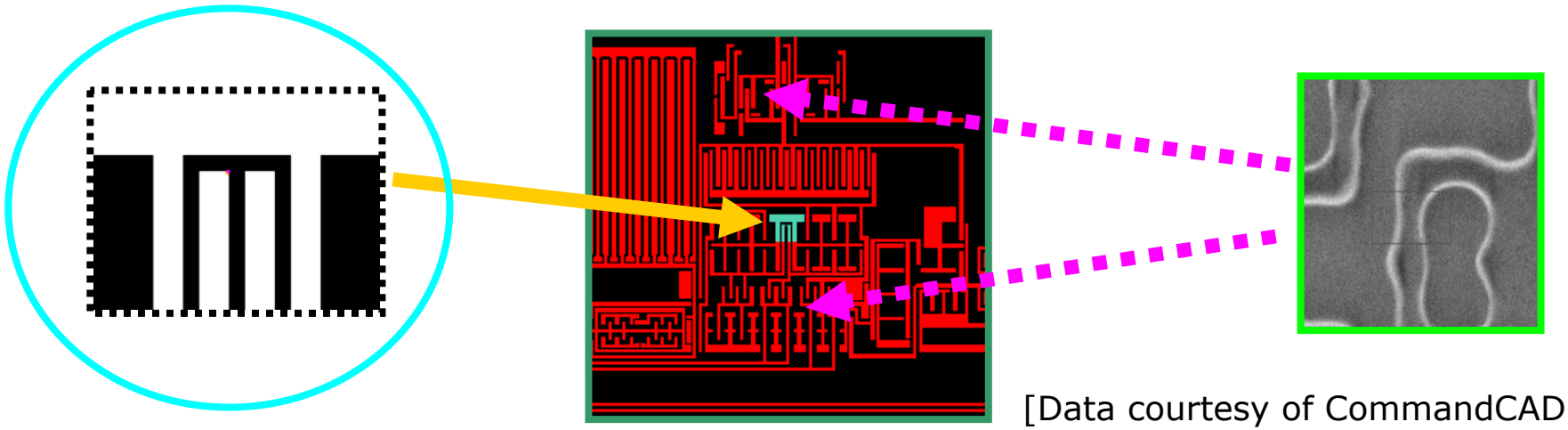

```
poss_cross_spacer  = EXT VIA1 == cross REGION OPPOSITE
//should be a "cross" shape
poss_square_spacer = EXT VIA1 == v_square REGION OPPOSITE
//135 by 135nm
//Verify the correctness of the "cross" spacer
//Width == via_size
test1 = vertex poss_cross_spacer ==12
test2 = AREA test1 == .091125
test3 = length test2 != VIA_SIZE //edges not equal via width
test4 = EXPAND EDGE test3 outside by .01
cross = test2 NOT INTERACT test4
```



2D-DRC
Image-Based



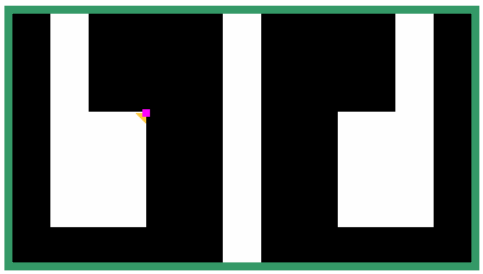
Layout Analysis by Pattern Matching

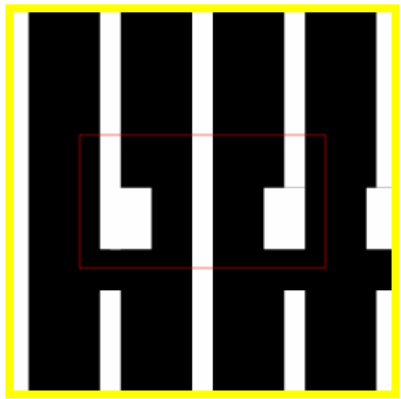


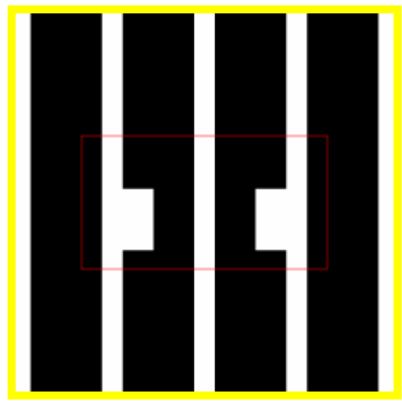
[Data courtesy of CommandCAD]

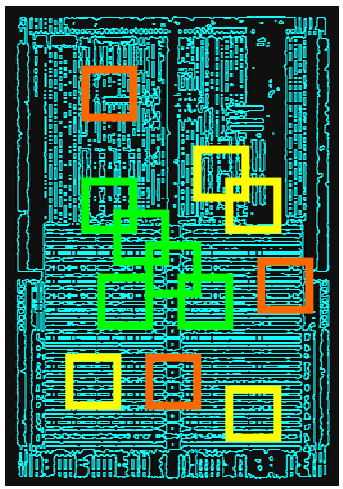
- 2D (ultra-fast) Image-Based Pattern-Matching capability has been demonstrated, for full-chip layouts
- (X,Y) Locations of Polygonal Clips (images) can be identified
- Image-based pattern-matching allows for fuzzy-matching
- Approach can be extended to SEM images

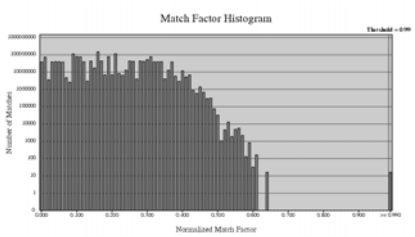
Layout Analysis by Patterns Matching [I]





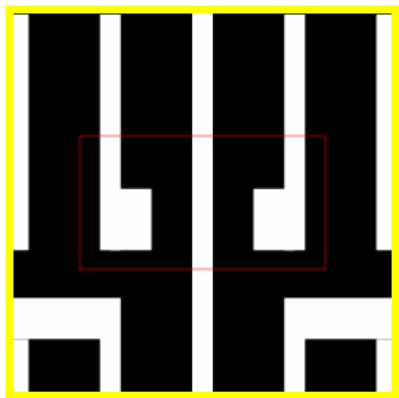




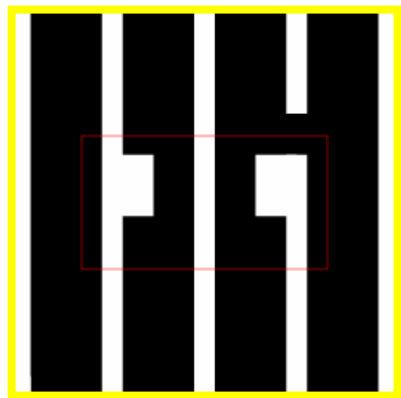


Full-Chip Pattern-Match (X,Y) Locations

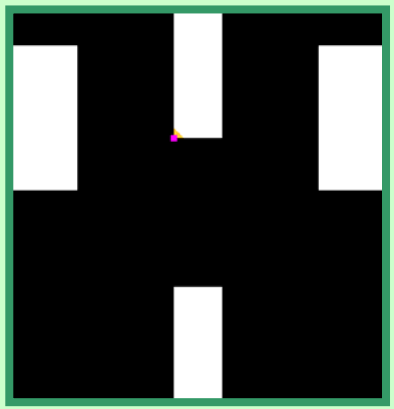
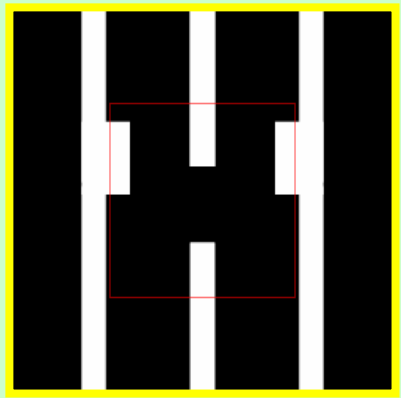
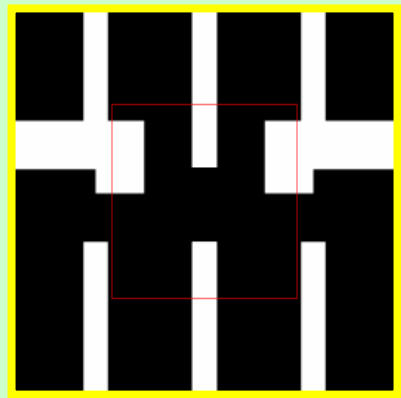
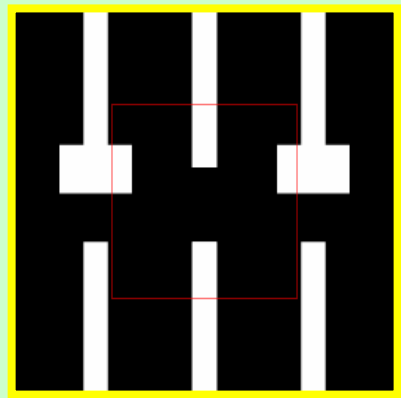
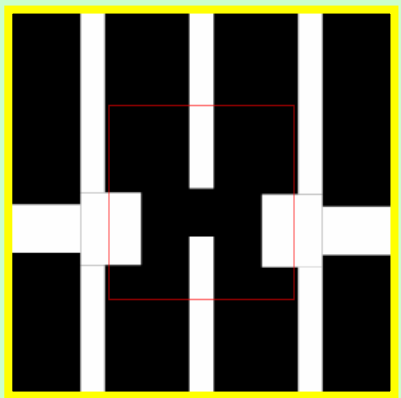
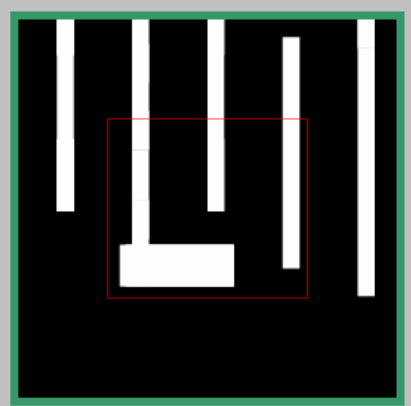
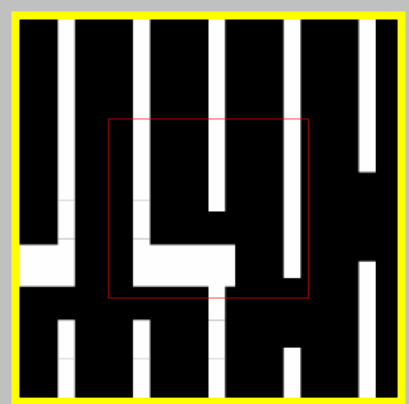
Exact Match



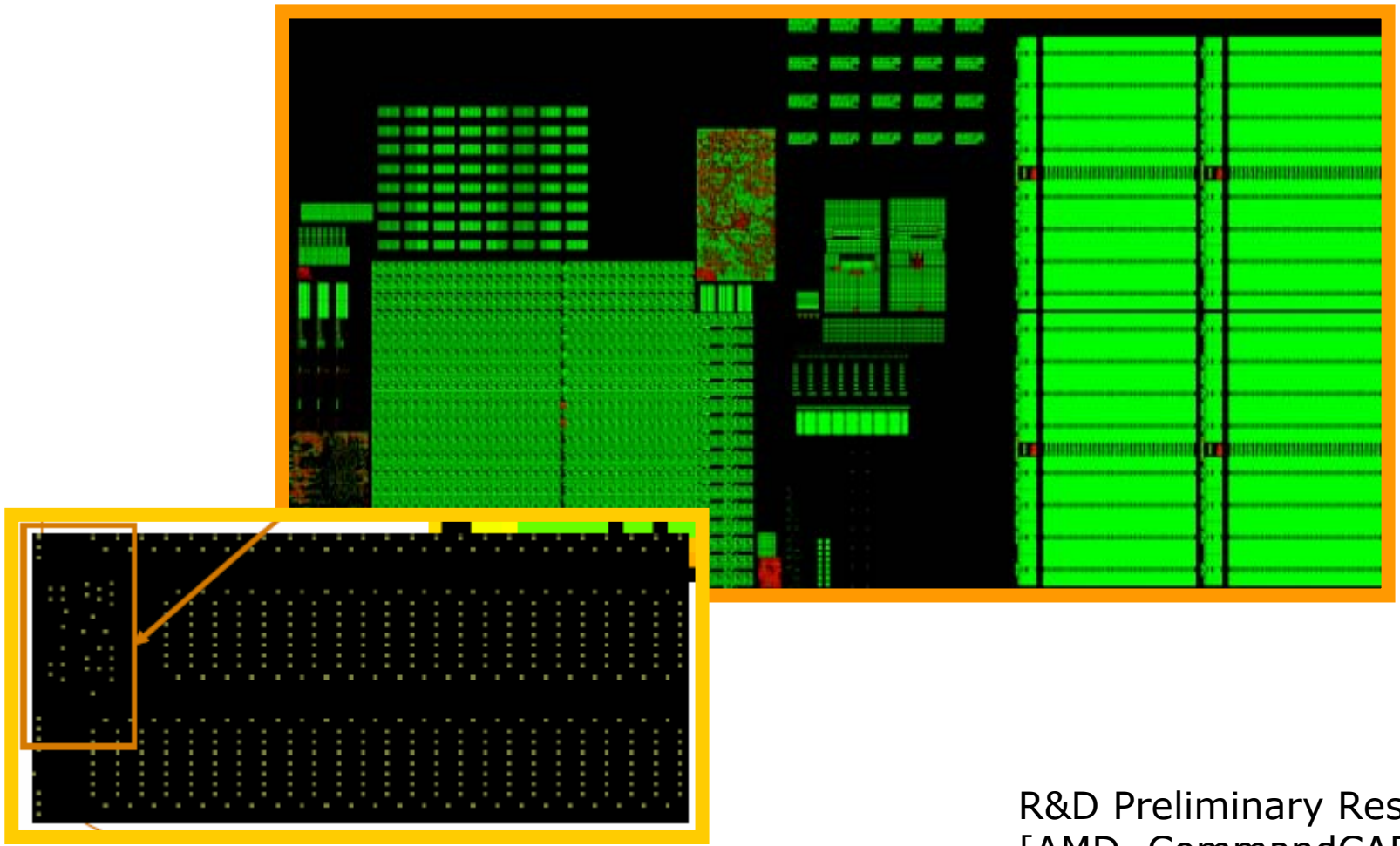
FUZZY MATCH



Layout Analysis by Patterns Matching [II]


Identifying Non-Regularities in Layouts



R&D Preliminary Results:
[AMD, CommandCAD]

Summary and Conclusions

- For the past 10 years constant "evolution" of RET and OPC has remedied lack of "intelligent (layout) designs"
- Lithography-Driven Design For Manufacturing (Layout Printability Verification) is now a well established practice at 65 nm
- Continuing DFM evolution drives towards more and more Regular Layouts (concept adopted also at Circuit Design Level)
- 2D DRC Flows have been demonstrated to identify potential Yield Detractors early in the Design-to-Fabrication Cycle
- Independently of choice of next-generation patterning solutions (lithographic and/or non-lithographic) DFM methodologies (i.e. integrated approach to patterning) will enable and support roadmap at 45, 32 and 22 nm nodes

Acknowledgements

- Yi Zou, Vito Dai, Cyrus Tabery, Huda Saeed, Kishan Shah
- Norma Rodriguez, Jie Yang, Wojtek Poppe, Ethan Cohen, Mark Craig
- Christopher Spence, Christopher Lyons, Marc Staples, Mike Exterkamp, Bhanwar Singh, Todd Lukanc, Sarah McGowan
- All APD-Lithography and SDC engineers, all FAB30 and FAB36
- … and many others. Thank you all !!!