OA Gear: OpenAccess for Academic Research

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Outline

- Academic Research
- OpenAccess
- OpenAccess Gear: Timer, Gui, Func, Aig
- IWLS 2005 Benchmarks and
  IEEE Programming Challenge at IWLS
- Future Plans
- OA Gear Team

Academic Research

- Key algorithmic inventions are coming from academic research: Logic synthesis, placement, …
- Implementation still mostly based on point-tool view:
  - Dedicated data structures and file formats representing only one or few aspects of the design (for example placement problem as boxes and connections)
  - Lack of serious “vertical” benchmarks for complete flow.
- Difficult industry adaptation:
  - Hard to evaluate true value of new algorithm
  - Most likely need to reimplement from scratch to find out whether it really works and gives good results.

OpenAccess

- OpenAccess is an open source design database for EDA
  - OA has been adopted by many companies:

    98 Si2 members, 31 OpenAccess coalition members
  - Standardization helps tool interoperability
- OpenAccess should also be beneficial for academic users
  - Ensures benchmarks, experimental results can be easily exchanged
  - Technology transfer of algorithms developed at universities into industry tools
- Si2 Nonmember Academic Program: Si2 distributes the latest OpenAccess members-only release (binaries, header files, and API reference documentation) to academic researchers (students and university faculty)

http://www.si2.org

OpenAccess Motivation

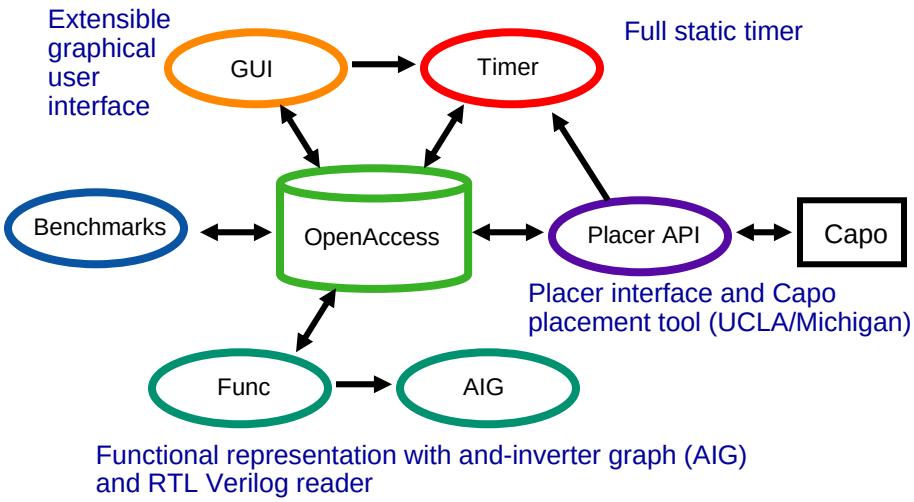
- Provide **tight integration and incremental design flows** using design tools and data from multiple sources
- Ease **integration** of internally developed tools with those from EDA suppliers
- Provide more cost effective **technology transfer** of university research into the design flow
- Simplify **technology sharing** for collaborative development between business partners for design tools and design data

from “What is OpenAccess?” ,http://www.si2.org

OA Gear

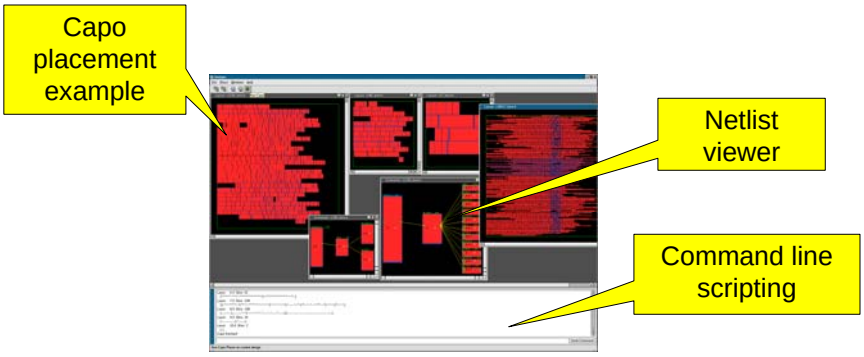
- OA Gear = a library of essential utilities / components built on top of OpenAccess
- Initially released Nov 2004, ~600 downloads so far
- Open source licensing model
  - Critical for academic use, true community development model
  - Working well: Fixes / improvements from user feedback, users have even provided complete bug patches
- Freely distributed, no cost
  - Available even on tightest budget, also free for commercial use

OA Gear



OA Gear Bazaar

- Graphical User Interface
  - Layout & netlist viewers, with a command-line scripting window
  - Extensible by OA users, developed using OpenGL & QT toolkits



OA Gear Timer

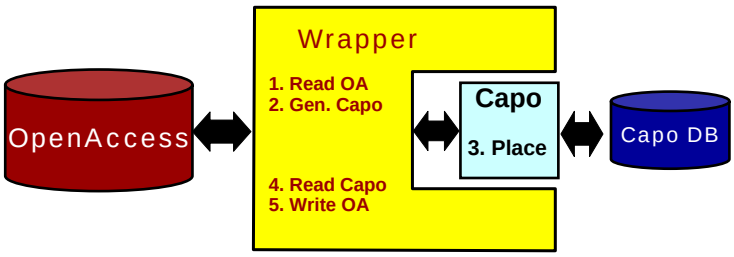
- Timing is often ignored in academic research
  - Difficult/expensive to integrate commercial timing engines
  - Significant task to write own timer
  - Significant calibration/fidelity issues
- Solution: OA Gear Timer
  - Common timing infrastructure
  - Integrated, rich feature set
  - Accurate slew propagation for rise and fall
  - Results validate to ~1% against Cadences RTL Compiler tool
- Upside
  - Helps ensure results from different researchers can be compared directly

OA Gear Timer

- Supports Synopsys Liberty (.LIB) formats
- Supports .SDC constraint subset: Clock period, external delay, multiple clocks, multi-cycle paths
- Incremental Timing Analysis
- Three wire load models (so far…)
  - **Idealized:** ignores wire loads
  - **Linear:** half-perimeter bounding box using unit C, R info from technology library
  - **Custom:** allows users to specify their own models for wiring
- Standard APIs & reporting formats
  - Worst critical path
  - Paths *–from –to –through* a node

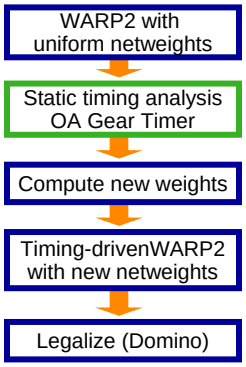
Placement: Capo Wrapper

- Motivations
  - An OA Gear placer let users work on apps requiring some real layout
  - Excellent example of how to **integrate** a large, already **mature** CAD tool
- OA Gear includes a wrapper for the open-source Capo placer
  - Tool developed at UCLA/Michigan for several years
  - Existing code base does not use OA; "wrapper" API allows Capo to use OA



CMU WARP2 Placer

- Our starting point: WARP1 [Xiu et al DAC04]
  - Wirelength-only placer with ad hoc academic db
- Our result: WARP2 [Xiu et al DAC05]
  - Timing-driven -- complete native OA integration
  - OA Gear Timer critical to flow
  - OA Gear Benchmarks, PDKs exploited heavily
- How fast: ~1 month to integrate, prototype
  - Out best guess: **3X – 4X faster** than proprietary

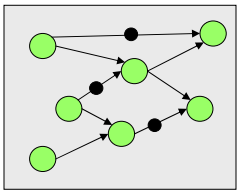


Wirelength-only WARP2 / Domino			Timing-driven WARP2 / Domino		
ΣWirelen	Worst Neg Slack	ΣCPU	ΣWirelen	Worst Neg Slack	ΣCPU
1.00	1.000	1.00	1.01	0.635	1.47

OA Gear Func

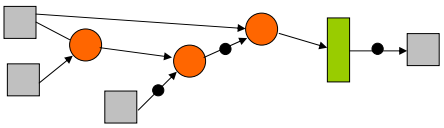
Functional representation for synthesis and verification

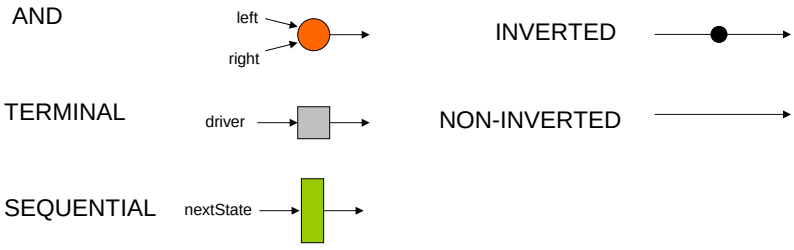
- Functional descriptions can be imported from RTL Verilog or gate level Verilog with Liberty (.lib) libraries
- **RTL Verilog:** Parser understands a synthesizable subset of the commonly used 1995 standard: structural / mapped designs, hierarchical designs, behavioral descriptions, arithmetic operations, sequential logic
- All functional information is synthesized into a common format



OA Gear Func

And-inverter graph



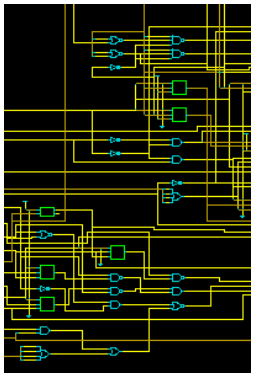


OA Gear Func

- Efficient memory management
  - Paged allocation, garbage collection, hashing by structural isomorphism
- Toolbox of useful algorithms
  - Transitive fan-in and fan-out
  - K-way cut enumeration
  - Equivalent node marking and substitution
- Directly incorporated into OpenAccess database
  - Automatically serialized and unserialized
  - No data conversion, import/export, etc.
- Tools
  - simpleMap – a simple mapper (3 different cells: AND, INV, sequential cell)
  - equivCheck – an equivalence Checker using CU BDD package.

IWLS 2005 Benchmarks

- 84 benchmarks from
  - OpenCores (26)
  - Gaisler Research (4)
  - Faraday Technology Corporation (3)
  - ITC 99 (21)
  - ISCAS 85 and 89 (30)
- All benchmarks synthesized and mapped to a 180 nm library with 38 different library cells (distributed with the library)
- In two formats: Verilog and OpenAccess



- http://iwls.org/iwls2005/benchmarks.html

IEEE Programming Challenge at IWLS

Programming Challenge at the International Workshop on Logic Synthesis (IWLS)

- Challenge: Implement one or more logic optimization algorithms on OpenAccess, use OA Gear.
- Judging criteria:
  - native OpenAccess / OA Gear implementation
  - architecture and versatility (to use in synthesis flow)
  - unit tests, regression tests, documentation, OpenAccess coding standard
- Prizes: travel grants to the IWLS workshop in Vail, CO, 7 - 9 June 2006, (airfare, full registration and lodging) and one cash prize for an outstanding contribution
- Deadline for submission: 1 May 2006
- http://www.iwls.org/challenge

OA Gear Future Plans

- Timer support for statistical timing model
- Extractor (coming soon)
- Migration to Synopsys Liberty and SDC parser
- Export OA Gear APIs to TCL with a standardized interface
- Routing-related tools: global/detailed routing, better routing estimation techniques (for placement), etc.

OA Gear Team

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David Papa	Univ. of Michigan	Bazaar, Capo Wrapper
Afshin Abdollahi	Univ. of Southern California	Timer
Aaron Hurst	Univ. of California, Berkeley	Functional Layer
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http://openedatools.si2.org/oagear/