



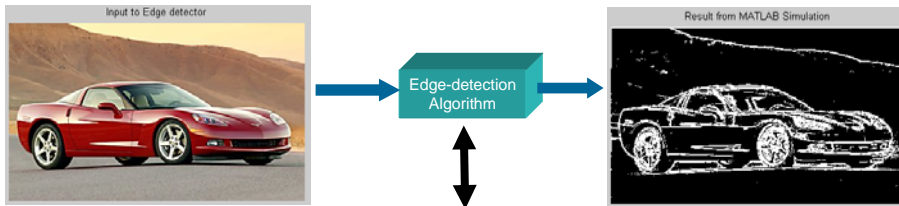
# High-Level Specification and Design of DSP Systems

April 13, 2006  
Rev 1.

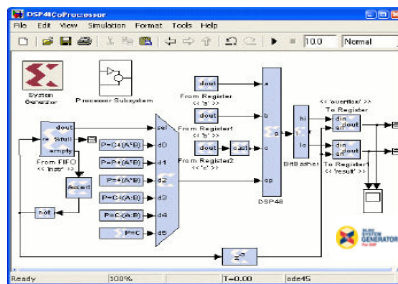
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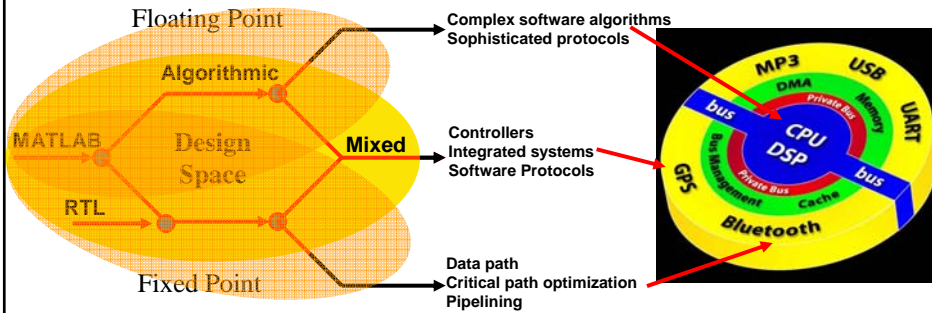
## Algorithms to Implementation “DSP : An estimate of reality”



```
function edge_pixel = edge_detection(pixels,nColumns,threshold);  
persistent Row;  
if isempty(Row) Row = zeros(1, nColumns); end;  
dY = abs(Row(nColumns) - pixels); % difference from present pixels to line above  
dX = abs(pixels - Row(1)); % difference from present pixel to adjacent pixels  
if ((dX > threshold) || (dY > threshold))  
    edge_pixel = 255;  
else  
    edge_pixel = 0;  
end  
Row = [pixels Row(1:end - 1)];
```



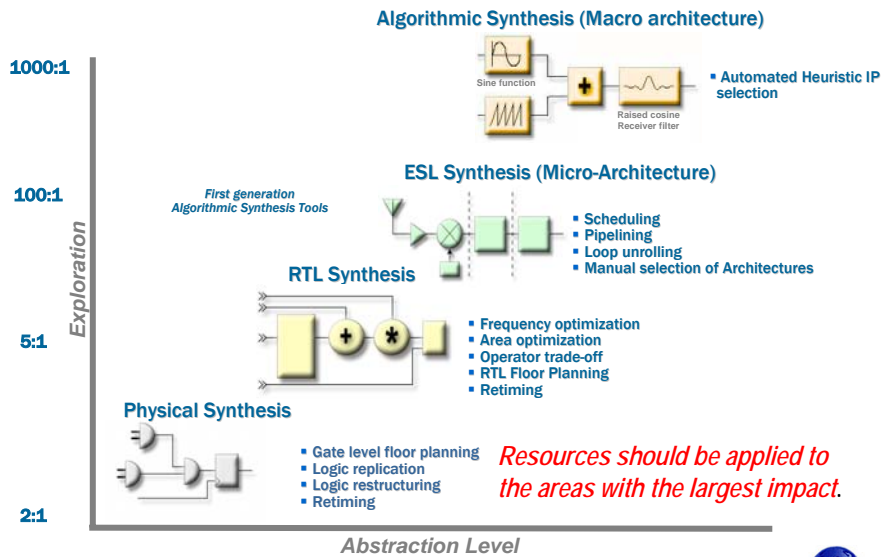
# Algorithmic System Design



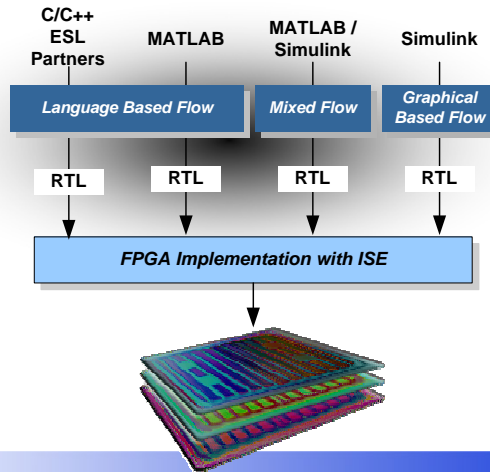
AccelChip's focus is "Designer Quality" ASIC, FPGA and Structured ASIC Implementations



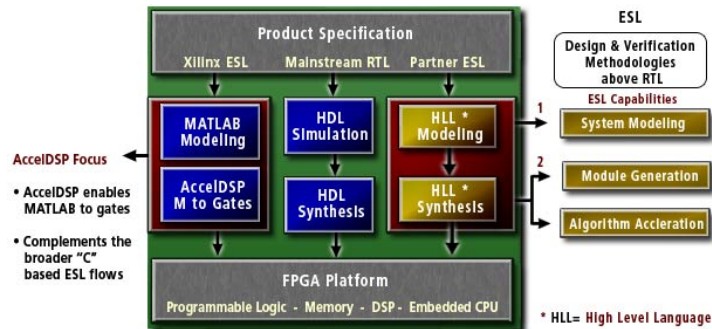
# Design Abstraction effects QofR



# Xilinx DSP Tools and Flows Accelerating DSP Design



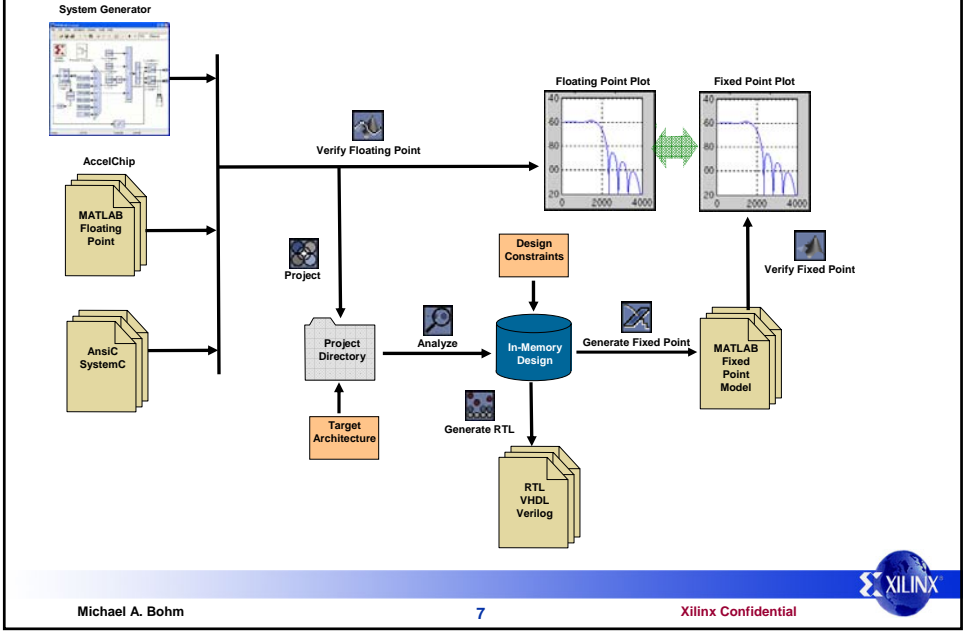
# ESL Initiative



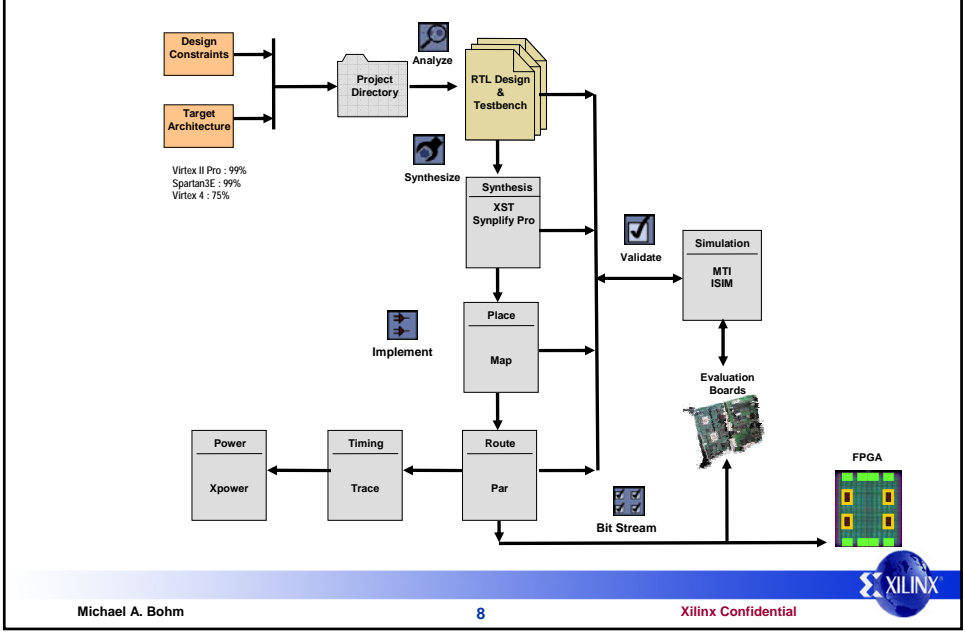
Making electronic system level (ESL) design methodologies and tools more accessible  
*Bluespec Inc., Celoxica, CriticalBlue, Impulse Accelerated Technologies, Inc., Mitronics, Inc., Nallatech, Poseidon Design Systems, Inc., SystemCrafter, Teja Technologies.*



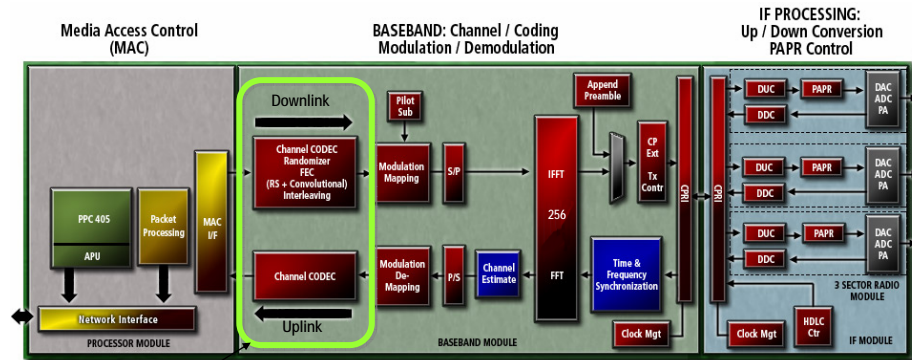
# ESL Design Flow



# RTL Design Flow



# 802.16d PHY



OFDMLibv1.0 covers the IP within this section of the 802.16d PHY



## Typical Design

### Original MATLAB

```

NFFT=32;
divOrder=2;
rand('state',0);
h_mat_fft=rand(4,32);
rTwoSide = rand(4,32);

h_f = fft(h_mat_fft);
r_f=fft(rTwoSide);

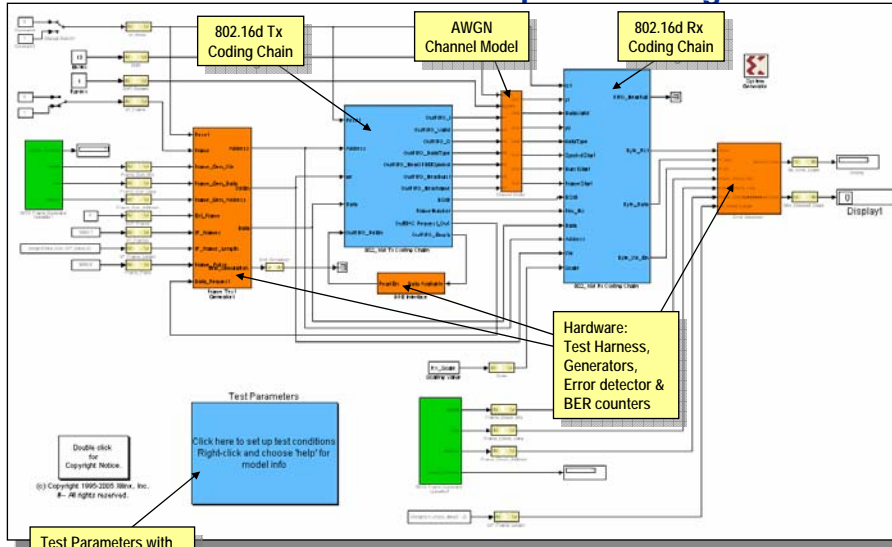
% inversion
E = r_f(1:divOrder,1:divOrder);
E = reshape(E,divOrder,divOrder);
E = transpose(E)
E = E + 0.05;
tmp_out = inv(E)* (h_f).';
w_f = tmp_out.';

% dimension-wise IFFT;
w_t = ifft(w_f);
    
```

- Equalizer for WCDMA
- Specifications
  - Tech : FPGA
  - Area : ~2-4M gates
  - Clock : 40Mhz
  - Throughput : 520
- Includes many MATLAB and toolbox functions from AccelWare toolkits
  - FFT (8) : 32 point Radix-2
  - IFFT
  - Reshape
  - Transpose
  - Inv : Invert square matrix
  - Abs : Absolute value
- Verified hardware: 6 days



## System Generator Model Based Design Model 1: 802.16d Loop Back Design



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Test Parameters with detailed description of circuit operation.

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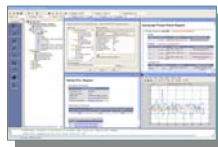
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## Xilinx DSP Solutions

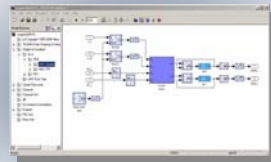
AccelDSP



Coregen DSP IP Cores



System Generator



Hardware Platforms



DSP Reference Designs

RACH  
Seacher  
TCC (3GPP2, 3GPP)  
HSDPA (Symbol & Chip)  
Digital Pre-Distortion  
CFR  
DUC/DDC (3GPP2, 3GPP)  
OBSAI  
CPRI

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