Physical Synthesis Challenges for FPGAs

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Field programmable gate arrays (FPGAs) are an increasingly popular medium for implementing digital circuits. FPGA implementations usually enjoy reduced development and verification times, and avoid the large costs involved in chip fabrication. This initial cost advantage over ASICs makes FPGAs an ideal medium for low-cost, small to medium volume productions. Modern FPGAs are large complex devices which allow for the realization of entire systems on a single chip. For example, Altera's Stratix II device (EP2S180) [1] contains 180K logic elements, 9MB of onboard memory, 96 DSP blocks, and support for 48 clocks. Achieving timing closure on such FPGAs is no longer an easy task, and a physical synthesis step is often needed in the CAD flow help close timing. In a traditional FPGA CAD flow, the synthesis step optimizes area and timing without any knowledge of the where the logic will be placed or how the connections will be routed, and yet it is the routing that dominates overall circuit delay. The physical synthesis solution is to apply logic restructuring techniques to improve the critical path at a point in the CAD flow where the impact of routing is better understood. A number of different physical synthesis flows can be considered. A *multipass* approach chooses to feed placement and routing information back into the synthesis step so that a new circuit which takes routing into account can be generated. Another approach, referred to as *early physical synthesis*, uses predictive techniques to estimate the effect that placement and routing will have on the circuit, and the results of these predictions are used to guide restructuring operations. In the third approach, referred to as *late physical synthesis*, restructuring operations take place after placement or routing have completed, and any resulting changes are integrated into the existing placement or routing using incremental techniques.

The introductory part of the talk describes some common restructuring techniques that are used during physical synthesis. These techniques include logic replication, combinational resynthesis, and register retiming. Next, the talk describes several challenges that need to be overcome in creating an industrial strength physical synthesis tool for FPGAs. These challenges include:

- Handling a wide variety of timing constraints during restructuring operations.
- Practical realization of compute intensive algorithms such as retiming.
- Functional correctness of restructuring operations that modify asynchronous paths.
- Legality constraints imposed by the FPGA architecture on the restructuring operations.
- Cost of integrating changes made by a late physical synthesis flow into an existing placement.
- Timing predictability for the purposes of an early physical synthesis flow.

Some potential solutions to these challenges are described using Altera's QuartusII software as an example [2, 3]. The talk ends with some some concluding remarks and directions for future work.

References

[1] Altera Inc. *Altera Product Catalog*. v2.0, December 2005.

[2] Altera Inc. *Quartus II Development Software Handbook*. v5.1, October 2005.

[3] D. P. Singh, V. Manohararajah, and S. D. Brown. Two-Stage Physical Synthesis for FPGAs. In *Proceedeings of the IEEE Custom Integrated Circuits Conference*, San Jose, California, USA, September 2005, pp. 171–178.