Towards Manufacturability Closure: Process Variations and Layout Design

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ABSTRACT
This work is based on a recently proposed manufacturability framework. To demonstrate the effectiveness of such framework, a layout optimization was performed using the information provided by manufacturability indices. The indices are based on process and failure characterization derived from a process variability description. The optimal layout configuration is analyzed via pattern-transfer and signal delay variations across multiple manufacturing conditions. These results suggest that existing process information can effectively be used to improve the manufacturability of IC designs.

Keywords: Microlithography, litho-friendly, RET-compliant, timing analysis, process models, low k1, subwavelength, DFM framework.

1. INTRODUCTION
Traditionally, IC designers have relied on a hand-off approach in which geometric and connectivity design rules determine the manufacturability of a particular product. The necessity of capturing processing effects in geometric rules was in part based on the lack of adequate models (accurate and fast). However, there are a number of effects that range from optical to chemical, to electrical, which can only partially be addressed by the existing geometry-centric design rules as proven by many studies that consistently demonstrate how random yield-loss mechanisms have been surpassed by systematic yield-loss contributions [1]. It is until recently that advances in process modeling [2] have demonstrated the feasibility of compact process models to predict manufacturing behavior at conditions other than nominal. Although there is no shortage of ideas about the objective of DFM [3]- [7], the industry lacks a wide consensus on the meaning of manufacturability. Instead of trying to define manufacturability this work focuses on the pattern robustness of the design. While process window metrics (e.g. depth of focus, exposure latitude) are easily extracted for simple 1D features they are not well suited to describe 2D or arbitrary topology arrangements [8], in addition they are mostly lithography centric and cannot be immediately used to explore other manufacturing process effects like etch or CMP. The framework this work is based on [9] uses the concept of process variability bands (pv-Bands) (Figure 1) which integrates three major requirements of an ideal DFM system: Parallel evolution to manufacturing process, process effect independence and locality.

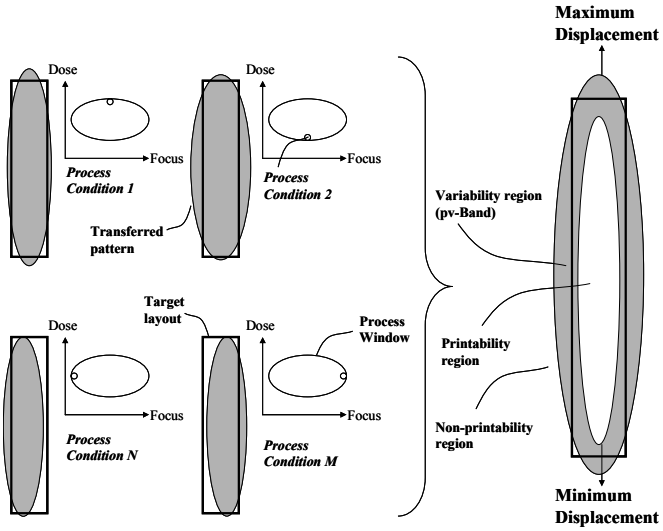


Figure 1. Process variability bands (pv-Bands). Example using two process variability effects: Energy dose and defocus.

By using the pv-Band as the DFM object it is possible to derive a sought-after scalar quantitative definition for pattern manufacturability, thus providing the foundation for manufacturability optimization. PV-bands are closed loop objects associated to each layout element, thereby meeting the locality requirement. Each band is defined by the sensitivity of the design to a particular processing effect providing process independence. Since the variability is defined by the existing process margins imposed by the process control, it immediately responds to the process evolution.

As the process matures, the process margins narrow, thus reducing the observed variability. While it is important that the pv-Bands improve as the process matures, they also provide a consistent way to design layouts less sensitive to existing process variations. This can be achieved by direct application of the framework and it is the subject of this study. We have used a generic implementation of the framework and executed a 130nm design optimization and evaluated its manufacturability for a direct shrink to a 90nm process. The optimal cell is analyzed by pattern robustness, manufacturability indices and delay process windows criteria. A complete IC-DFM framework should incorporate logical (design), electrical (materials) and pattern (process) related aspects to manufacturability. This work concentrates only on the pattern aspect but provides a forward

look on how all three aspects to manufacturability are indeed complementary.

2. MANUFACTURING CHECKS

Generic process models were calibrated for a 90nm process. The process characterization included the addition of the respective resolution enhancement technique (RET) in order to avoid false variability detection, especially important at 90nm.

The manufacturing checks are targeted for single layer interactions and focus only on pinch and bridge detection. Using the syntax defined by the applied framework [9] these faults can be written as:

$$pinch_{Violation} = OR\begin{pmatrix} AND(pvBand(layer)), \\ I2I(pvBand(layer)) \le pinch_{\min} \end{pmatrix} \quad (1)$$

$$bridge_{Violation} = OR\begin{pmatrix} AND(pvBand(layer)), \\ E2E(pvBand(layer)) \le bridge_{\min} \end{pmatrix} \quad (2)$$

Where,
$pinch_{min}$ = 45nm, $bridge_{min}$ = 45nm.
I2I is a pv-Band operator that measures the distance between internal pv-Band edges and *E2E* is a pv-Band operator that measures the distance between external pv-Band edges. The process manufacturability index (PMI) and the design manufacturability indicex (DMI) can now be defined as follows:

$$PMI = \sum_{layer} \frac{AREA(pvBand(layer))}{AREA(layer)} \quad (3)$$

Where, layer is: polysilicon, n and p implantation, nwell, diffusion, contact, metal 1 and thin oxide.

$$DMI = \sum \frac{AREA(DesignRule\ Violations)}{AREA(SupportLay\ er)} \quad (4)$$

Where,

DesignRuleViolations is a layer that contains the failure regions defined by equations 1 and 2 and *SupportLayer* is the layer subjected to analysis.

SupportLayer could be made to better capture the failure region in question, for example to define line-end enclosure errors a support layer would consist only of the areas that define the line-ends. In this study only pinch and bridge failure mechanisms were assumed. However, more complicated design rules can be incorporated by the correct combination of layers and operators. A complete description of all the available operators can be found in the formal description of the framework [9]

3. TEST CELL

The schematic and layout understudy are shown in Figure 2.

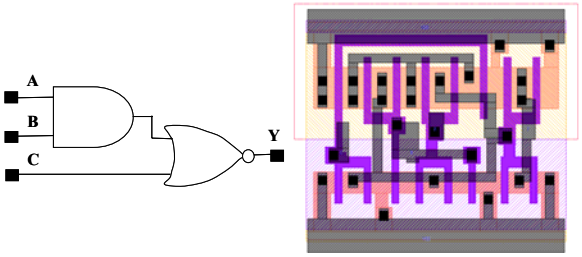


Figure 2. Schematic and intial physical implementation**.**

This DRC clean cell was initially obtained by an automated compaction tool. The subsequent operations maintained the DRC clean condition while seeking a different –more manufacturable- topology. The modifications were subject to traditional multi-layer constraints (e.g. poly landing pads are aligned with contact and metal layers). The complete truth table was tested for static functionality. The dynamic functionality was defined by 13 events which correspond to the number of times the output signal (Y) changes during the truth table test. The manufacturing process used to simulate the 130nm cells is a 90nm capable process. This is done for two reasons. First, it tests the sensitivity of the design optimization method since a 90nm process should have no problems in manufacturing 130nm designs rules. The second reason is the lack of complete SPICE models. Because of their tabular nature, by using a 90nm process models there is access to smaller feature sizes relative to the 130nm nominal features.

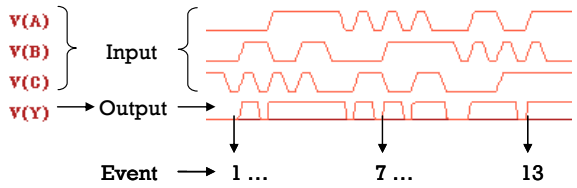


Figure 3. Event definition. Thirteen events were sampled for every litho-process condition.

4. DESIGN OPTIMIZATION

After a series of iterations the most manufacturable equivalent cell is depicted in Figure 4.

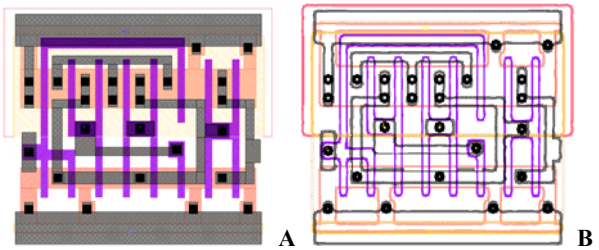
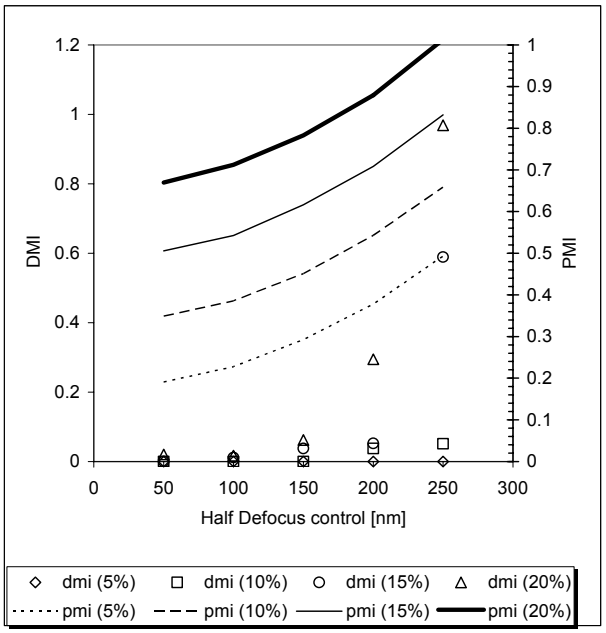


Figure 4. Optimal 130nm physical implementation of the test cell (**A**), and respective pv-Bands for all layers (**B**).

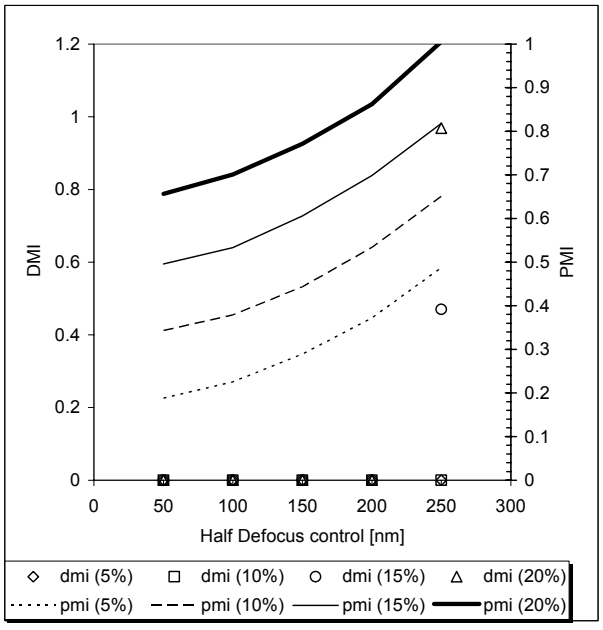
Notice how the cell implementations (Figure 2 Vs Figure 4) differ in topological aspects, in which the optimized cell takes a more manufacturable grid-like aspect. The area of the original and the optimized cells is the same, and both operate as designed at nominal conditions. However a more strict comparison involves the cell characterization at other processing conditions.

The DMI and the PMI were calculated at +/-5,10,15 and 20% dose control and +/- 50, 100, 150, 200 and 250nm defocus control. Because of the definition of DMI and PMI a smaller value is desirable, indicating that the pattern-transfer variability is small with respect to the area of relevance. This effectively converts the layout optimization problem to a cost function minimization problem, opening the possibility for automatic

corrections. An automatic correction method seems within reach by combining existing compaction methods with the directionality provided by the pv-Bands. For this work however, the correction method was performed manually using a layout editor and a pv-Band calculator environment.



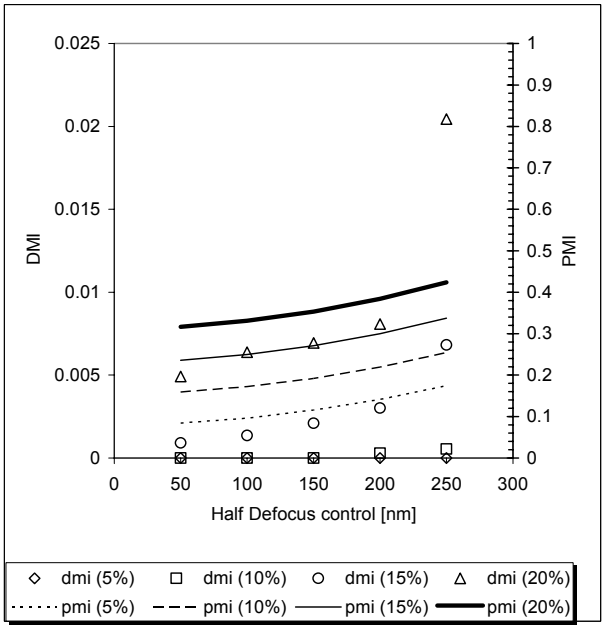
A



B

Figure 5. Manufacturability indices for contacts (130nm technology). **A**: Original cell. **B**: Optimized cell.

Figure 5A shows how contacts drastically fail (isolated contacts do not open and dense contacts merge) at the larger defocus conditions (+/-200 and +/-250nm) and more extreme dose margins (+/- 15 and +/-20%), but it also shows how there are a few errors at even tighter process control. In contrast, Figure 5B shows large failures at the largest process margins, but high process insensitivity at any other process condition. One of the main problems with making a layer insensitive is that by improving the manufacturability of one layer it can adversely affect another.



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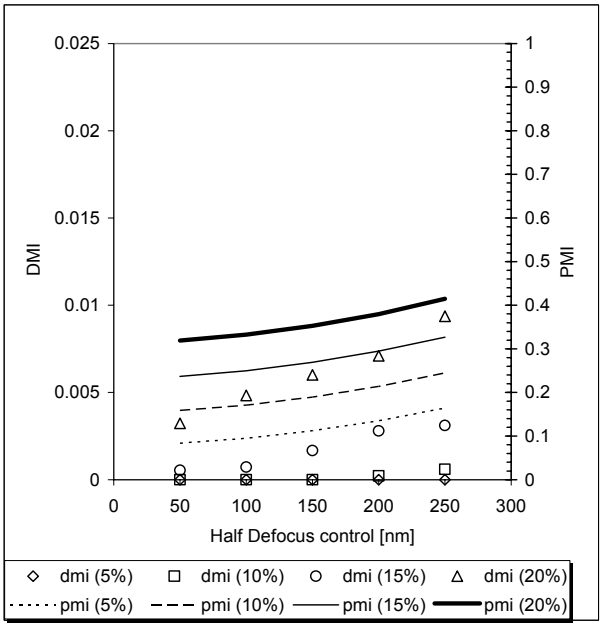
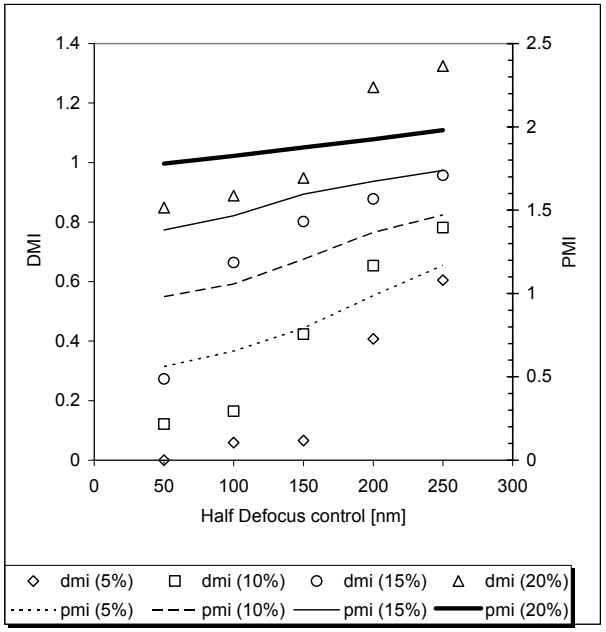


B

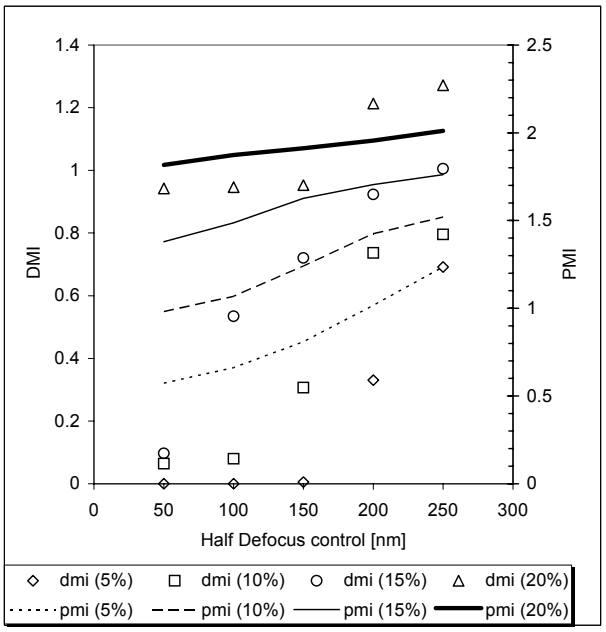
Figure 6. Manufacturability for polysilicon (130nm technology). **A**: Original cell. **B**: Optimized cell.

To assess this concern Figure 6 shows the results for the poly-silicon layer and how improvements can also be made to such layer -although much less dramatic, notice the different DMI scale-. N and P implant, oxide and diffusion layers remained constant; therefore, there is no difference between the PMI and DMI. Such layers were not optimized because they did not exhibit any failure points within the process margins of interest,

and they did not have to be modified to accommodate any changes imposed to the poly, contact and metal1 levels. Figure 7 shows the original and the optimized 130nm cell with a direct shrink to 90nm. While at 130nm the contacts started to fail only at the largest process margins, at 90nm the sensitivity to process variations is much more evident. The previously calculated optimal contact layer –now shrunk by a factor of 70%- is only slightly better than the original counterpart also shrunk by the same rate.



A



B

Figure 7. Manufacturability indices for contacts (90nm technology). **A:** Original cell. **B**: Optimized cell.

This data highlights a non-desirable side effect of DFM in which optimal topologies can be tied to a particular process in such a way that it can be difficult to generate a solution that returns maximum manufacturability for a group of available processes. In principle this limitation can be addressed by considering the bounds of multiple processes instead of one. This of course adds to the computational requirements but it is in principle feasible. The downside is that the solution can be sub-optimal for every considered process compared to a solution targeted for a specific process. This is when the availability of a manufacturability index helps guiding the design tradeoffs, by quantitative measuring how much more manufacturable a design would be between a series of available processes

5. PATTERN ROBUSTNESS

Pattern robustness is typically assessed by focus-exposure data in which a given feature is been sampled. Figure 8 shows feature changes, that affect gate length, for the original (**org**), and the optimized (**opt**) cell. Under the worst process margins (+/- 250nm defocus and +/- 20% dose change) the total CD range for the original cell is about 63nm while for the optimized cell is 53nm. This is how typically lithographers report feature behavior with process variations. The problem with this type of analysis is that not all features behave in the same manner. While there are regions that can be made more robust, others regions are very sensitive to process variations. How much these feature variations affect the electrical behavior of the cells has been a popular topic of investigation [10]-[11] and it will be addressed in the following section.

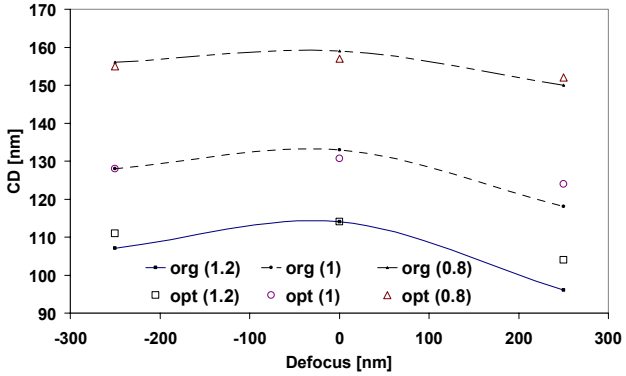


Figure 8. Focus-exposure "Bossung" graph.

6. ELECTRICAL BEHAVIOR

The simulations for each process condition used existing parasitic and SPICE models. In order to simulate timing, the 130nm cells were modeled using an existing 90nm process. This way, the SPICE model tables were able to interpolate the smaller geometries from the process-induced topological changes.

Traditionally manufacturing facilities provide five types of SPICE models: TT (nominal), FF, FS, SF and SS -referring to the fast (F) and slow (S) conditions for the n and p transistors-. By the nature of their calibration, SPICE models incorporate all processing effects including lithography from a statistical analysis of the process corners. This convolution of effects complicates the analysis of individual contributors. However, by explicitly calculating one manufacturing effect across all

available electrical models it is possible to determine the raw sensitivity of the design to such manufacturing effect. For simplicity this analysis assumes that all layers are built perfectly as drawn, and only the poly-silicon layer has been replaced by a real silicon image.

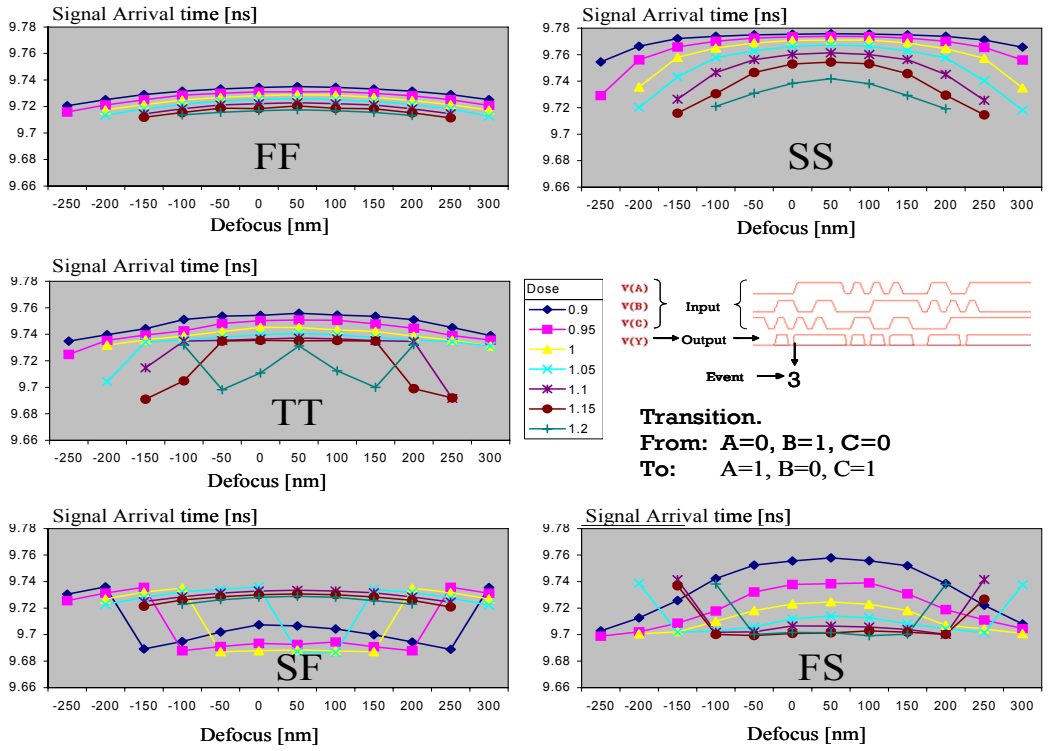


Figure 9. Original Cell Timing: Signal arrival times for event 3. Using FF,SS,TT,SF and FS SPICE models.

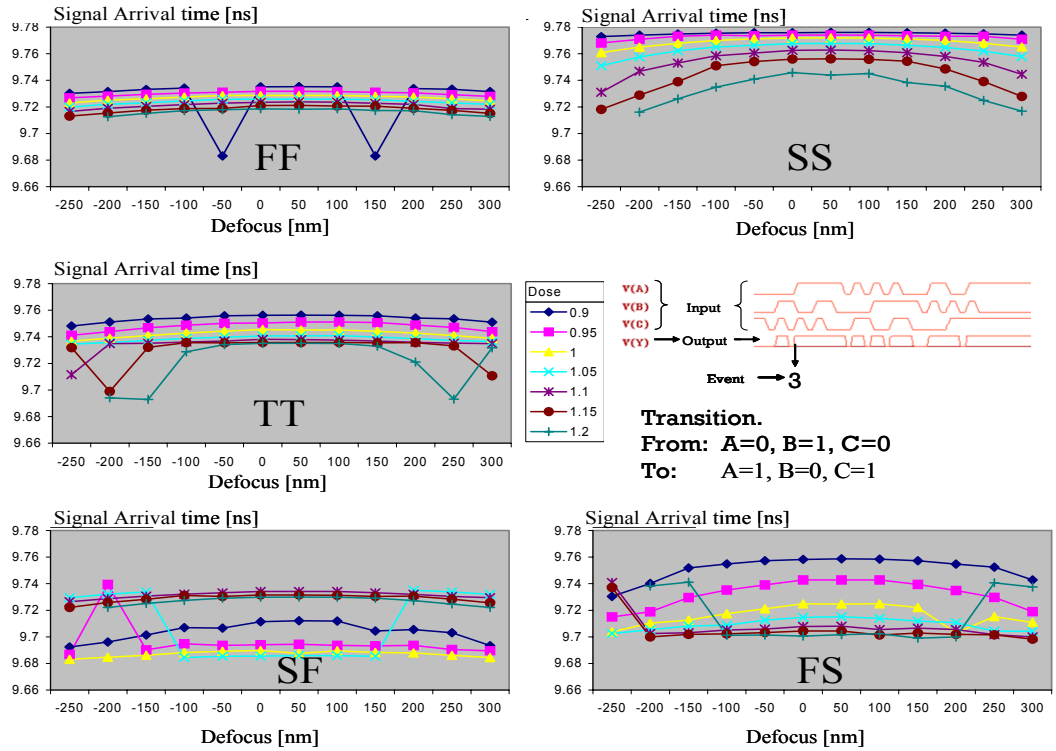


Figure 10. Optimized Cell Timing: Signal arrival times for event 3. Using FF,SS,TT,SF and FS SPICE models

This is a conservative approximation of the impact that lithography has on the electrical performance of devices. The simulations are done using all five available SPICE models in order to assess the relative contribution of lithography on the complete processing behavior. While the timing margins established by the non-nominal models (FF, SS, SF and FS) are able to enclose the poly-silicon process variations at nominal conditions (TT). It is clear that the process induced pattern variations are a large contributor to the total design margin. Figure 9 (original cell) and Figure 10 (optimal cell) show how the optimal cell remains to function at an even a wider set of process conditions. When the cell stops to operate the data series are truncated thus indicating that a fatal failure has occurred. In addition Figure 11 shows event 3 under a variety of process conditions and RET treatments. Since the RET was considered during the cell optimization, it is no surprise that the optimal cell shows the smallest delay sensitivity at most of the tested process conditions. The same analysis was done to the original cell with and without RET. The very different behavior between the three cases suggest that in order to correctly predict the electrical behavior of a layout it may be required to incorporate RET and process information during the electrical simulations, specially when trying to determine the margins of operation.

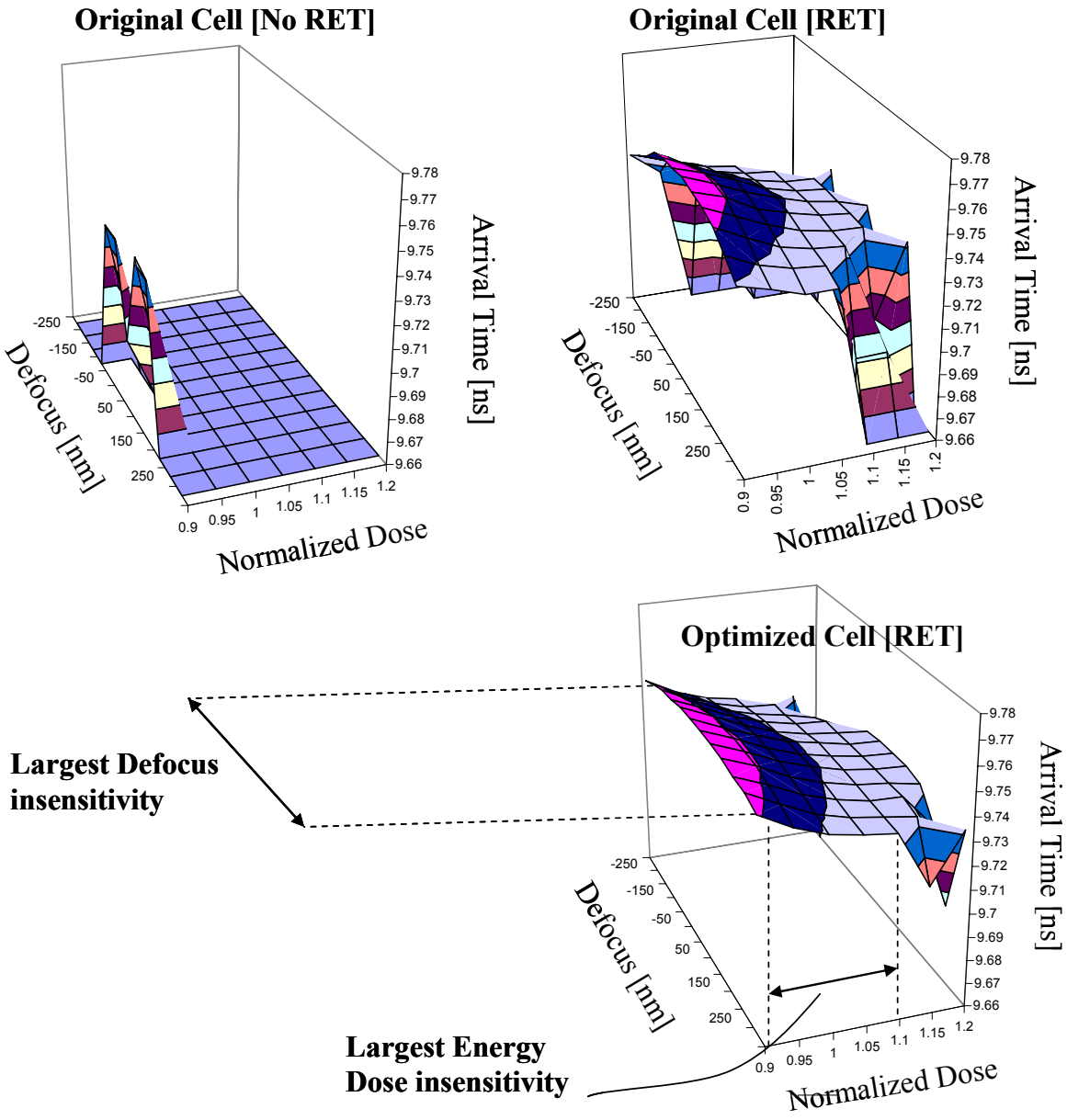


Figure 11. Pattern robustness translates in more consistent timing. (Nominal SPICE model shown).

7. CONCLUSIONS AND FUTURE WORK.

There is a clear improvement of the manufacturability of a layout at the pattern robustness level when the corrections are driven by manufacturability indices. These preliminary findings show that improved pattern manufacturability is consistent with better electrical performance across a variety of process variations, indicating the validity of this method.

One of the initial limitations of this optimization method is the availability of compact models for every processing step. Additionally, dense calculation of the process window to create the pv-Bands is unrealistic. Future studies will concentrate in the acceleration of the calculations at multiple process conditions. Due to the relative nature of the pv-Bands the process corner approach may provide a short-cut for reducing the computational requirements of the pv-Band calculations providing a clearer path for the extension of this methodology.

In the future it might be possible to enhance SPICE models by incorporating real pattern transfer information, and use redundant structures designed to be as process insensitive as possible. Since IC-DFM requires a vast cross-functional effort between process, materials and manufacturing teams, this work verifies the usefulness of a pattern-transfer metric that provides a quantitative description of the interplay between design and pattern transfer processes. The definition of a standard metric that evaluates pattern-transfer robustness enables the consistent exploration of other manufacturability components and the subsequent quantitative comparison between different proposals for IC-DFM systems and methodologies.

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