On Transparency in Design for Manufacturing

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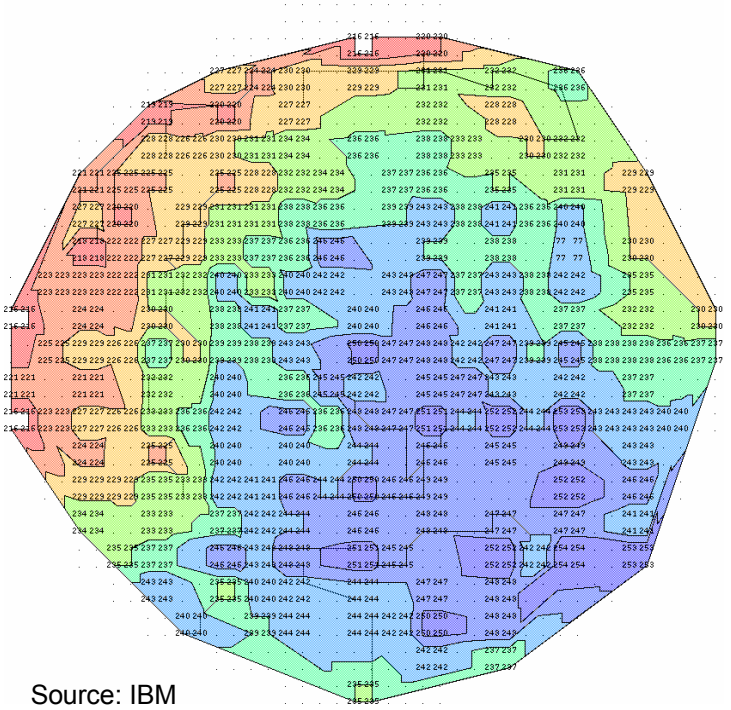
The “DFM Problem”

- There is no “DFM Problem”…
- … But users have many specific problems
  - TAT cost
  - Manufacturing NRE cost
  - Parametric yield
  - Leakage and leakage variability
  - Model-to-hardware correlation

Problem: Coping With Variability

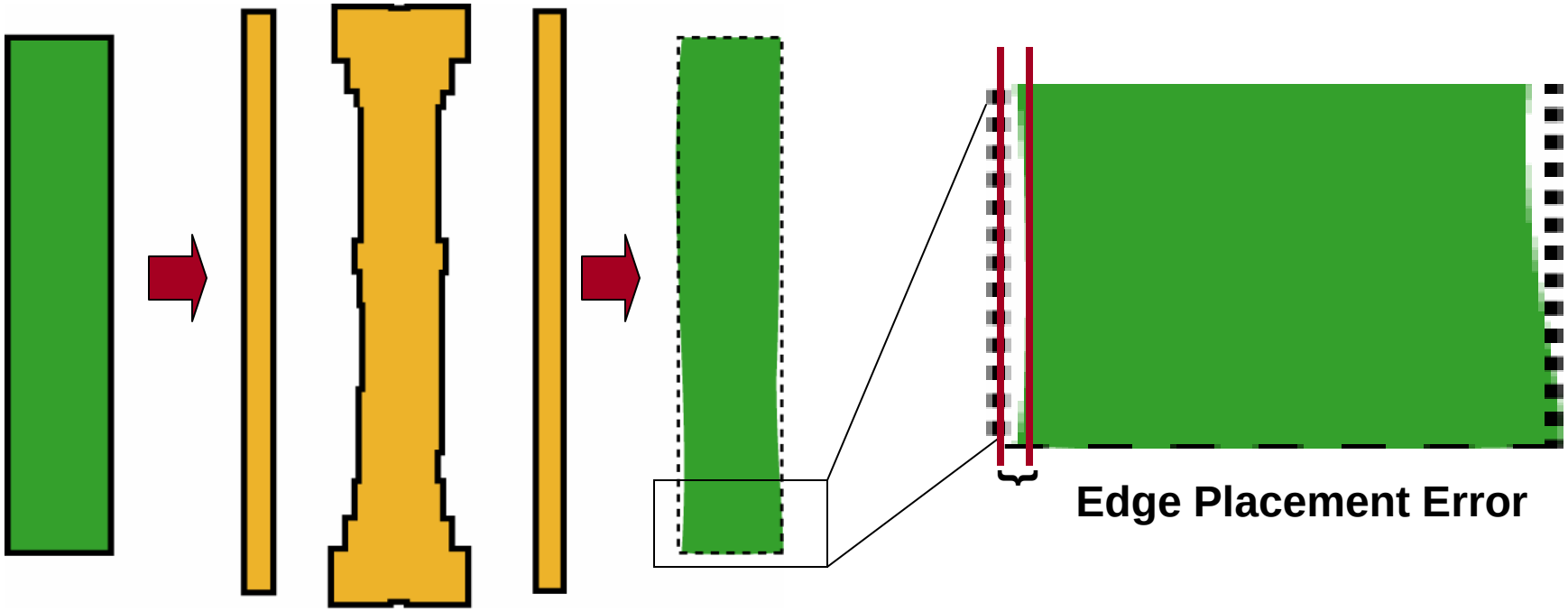
- **Sources of line width variation**
  - OPC error
  - Topography variation
  - Mask variation
  - Focus
  - Etch
  - Etc.



Source: IBM

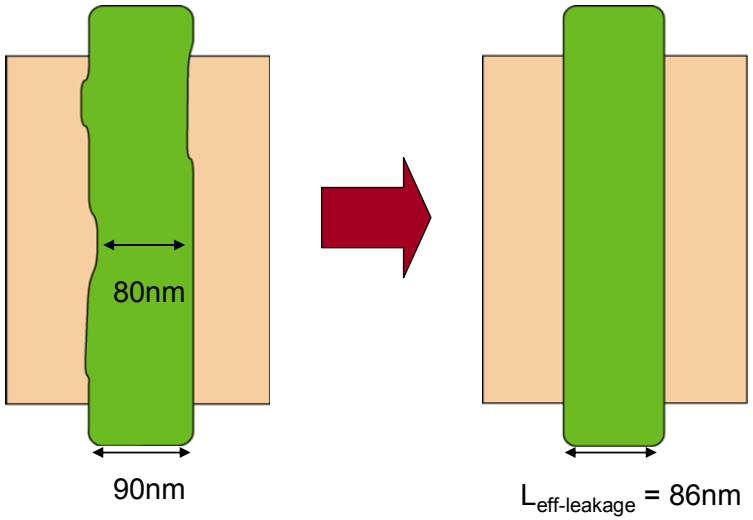
Going forward, this will get worse

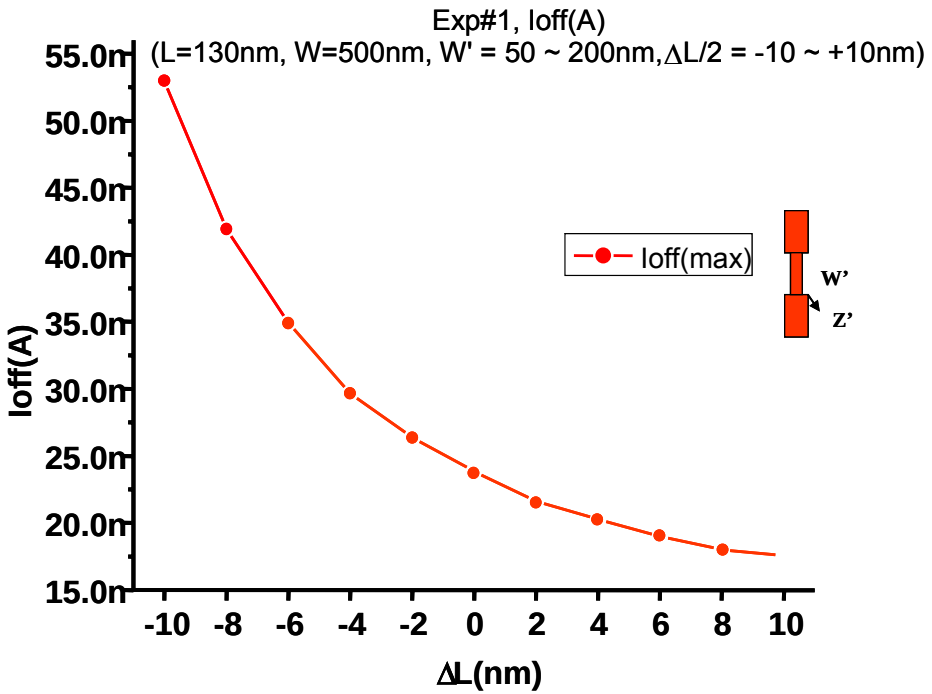
Problem: Residual CD Error After OPC



- **Sub wavelength features are not printed perfectly even with the use of OPC**
- **The residual CD error after OPC is called Edge Placement Error (EPE)**
- **EPE is an important component of line width variation**

Problem: Lgate and Leakage Variability





- Small variations in gate length have a big impact on leakage power

What Would DFM Success Look Like?

✗ Larger guard bands?

✗ Statistical timing analysis?

✗ Better equipment?

✗ … (+ many other failures of imagination)

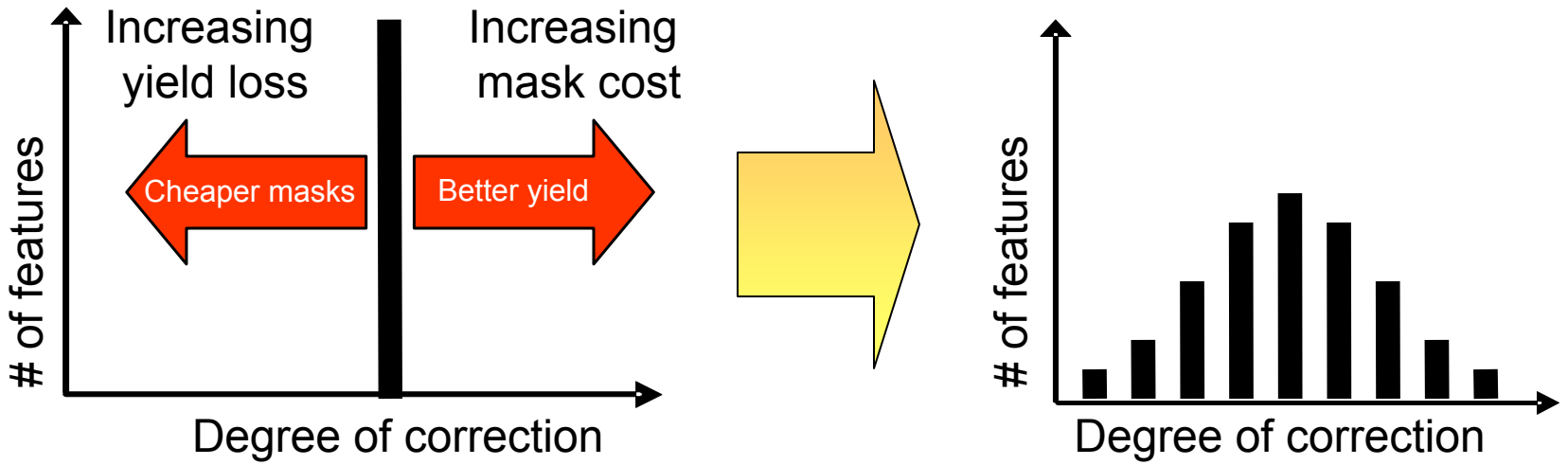
✓ Linking IC Design and Manufacturing

[Observation: Today's link = GDS, .lib, BSIM4]

Linking IC Design and Manufacturing

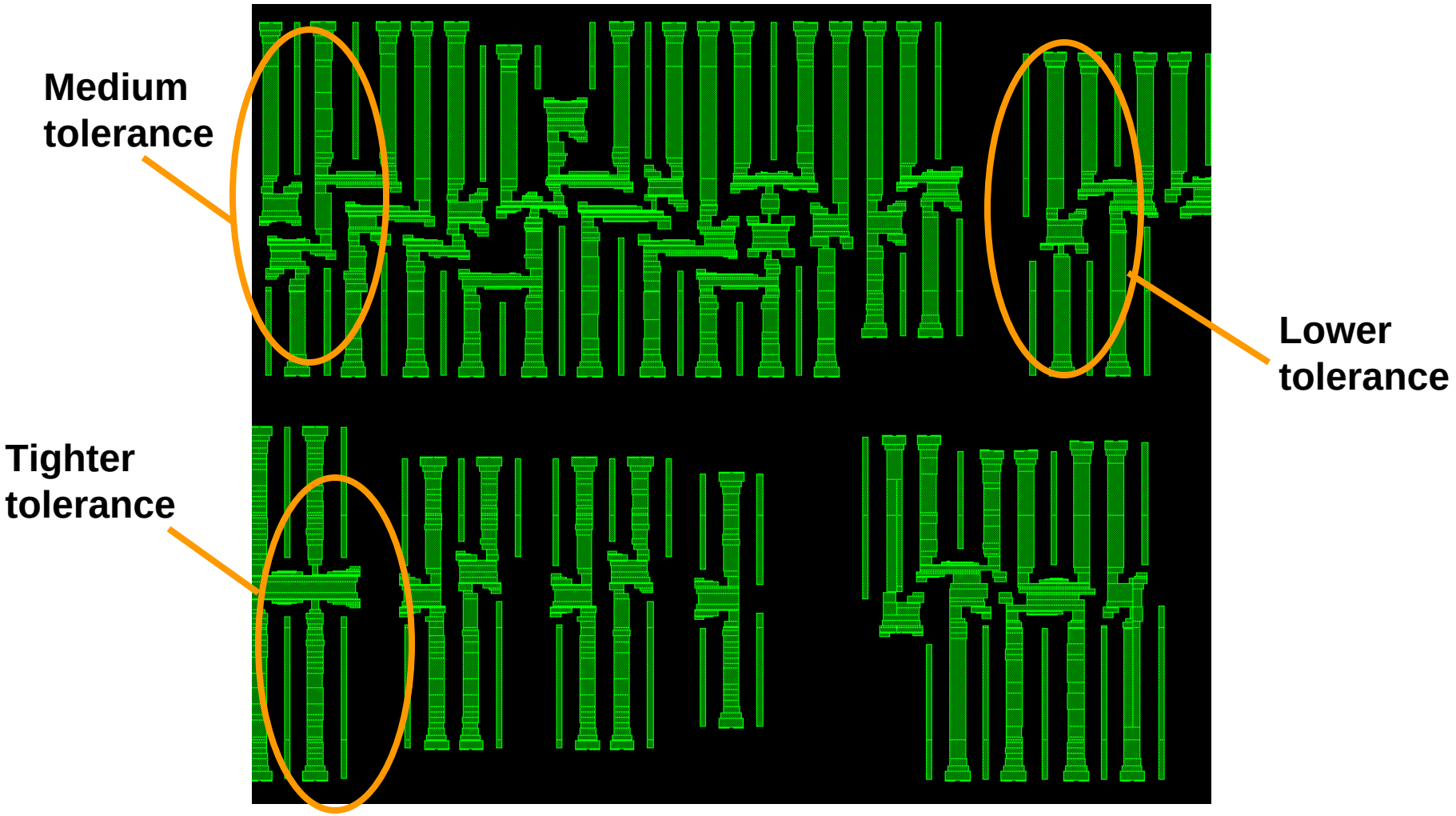
- **Drive design requirements into manufacturing**
- **Bring manufacturing awareness into design**
- **Do this as transparently as possible**

Example: Design Intent Can Drive OPC



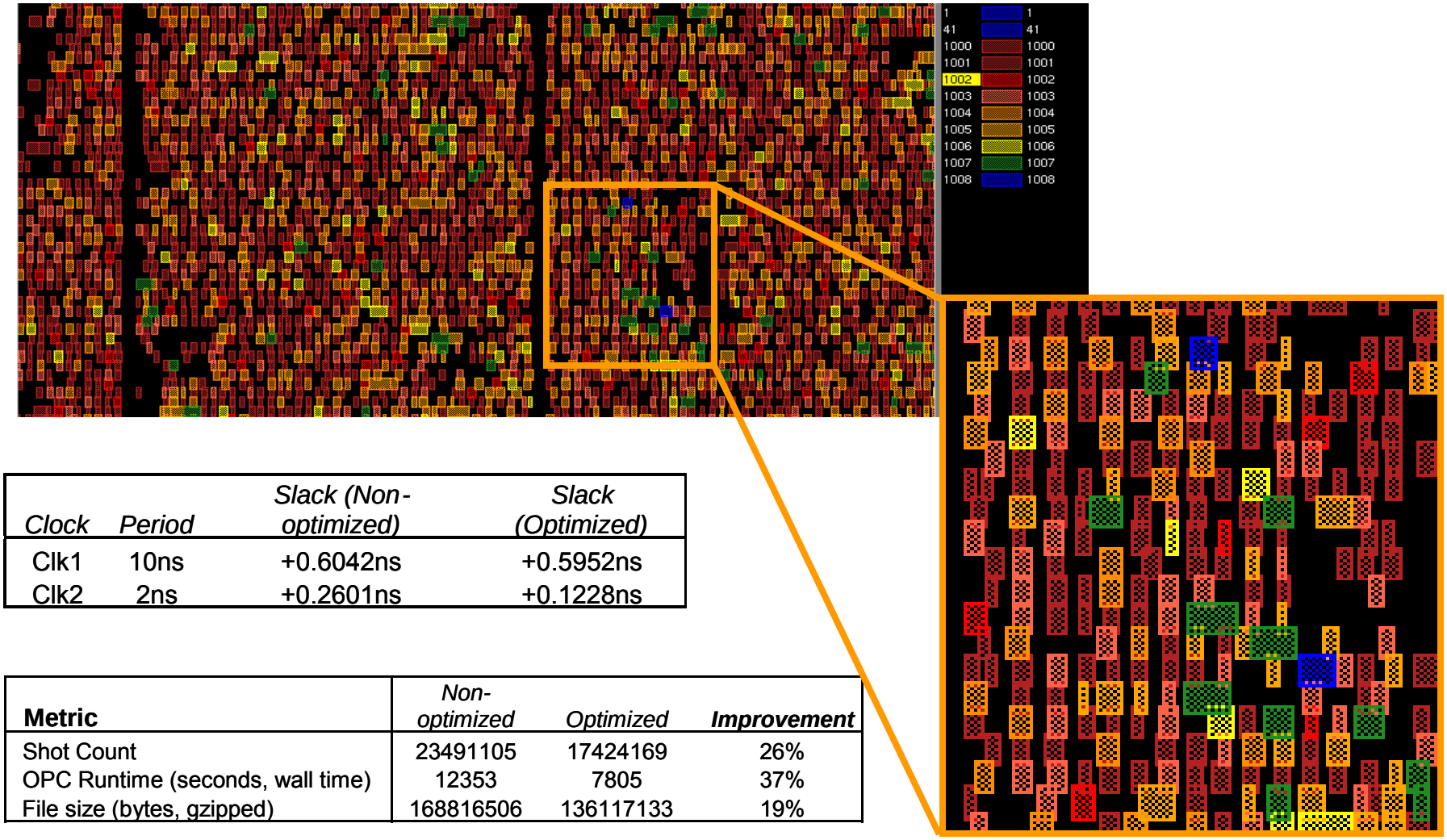
- Customized correction target per figure
- Automatically computed based on timing and yield analysis
- Superior solution for both yield and cost

Mask Complexity Optimization



Feature-specific OPC targets can reduce OPC run-time, mask complexity and mask cost

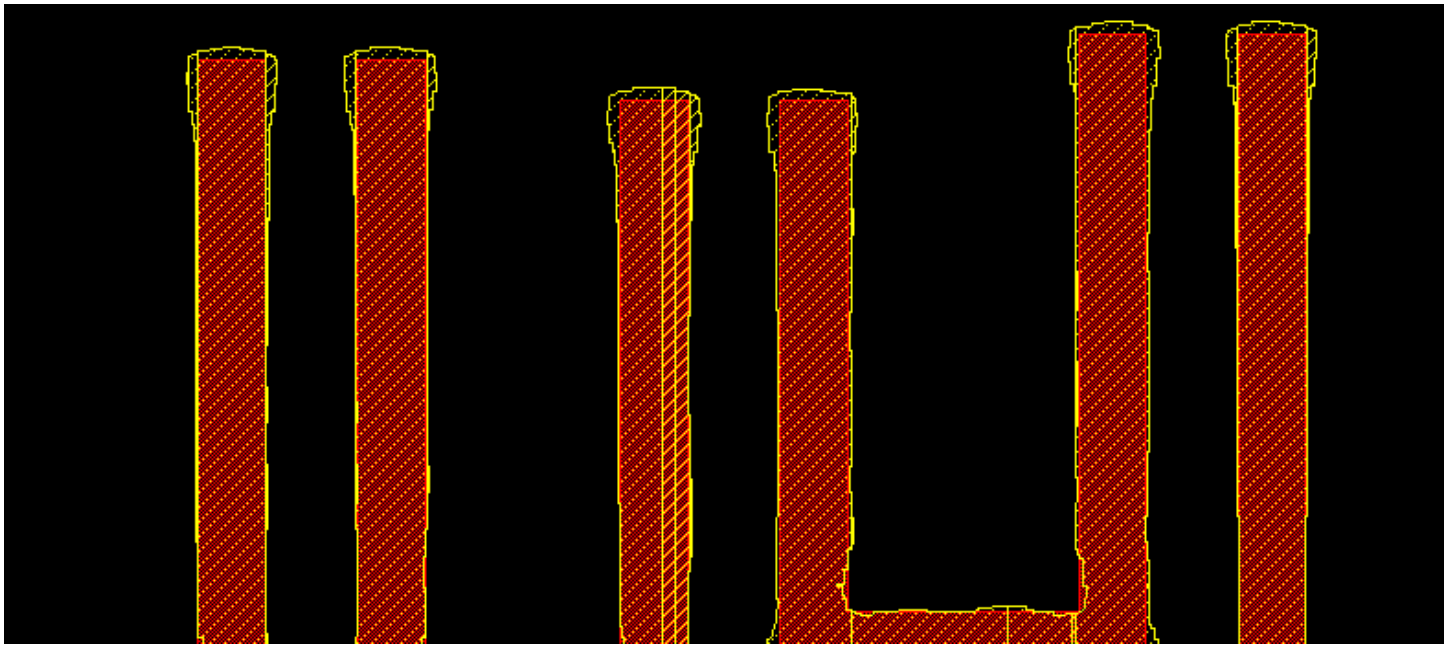
Transparency: Annotated GDSII



Clock	*Period*	*Slack (Non-optimized)*	*Slack (Optimized)*
Clk1	10ns	+0.6042ns	+0.5952ns
Clk2	2ns	+0.2601ns	+0.1228ns

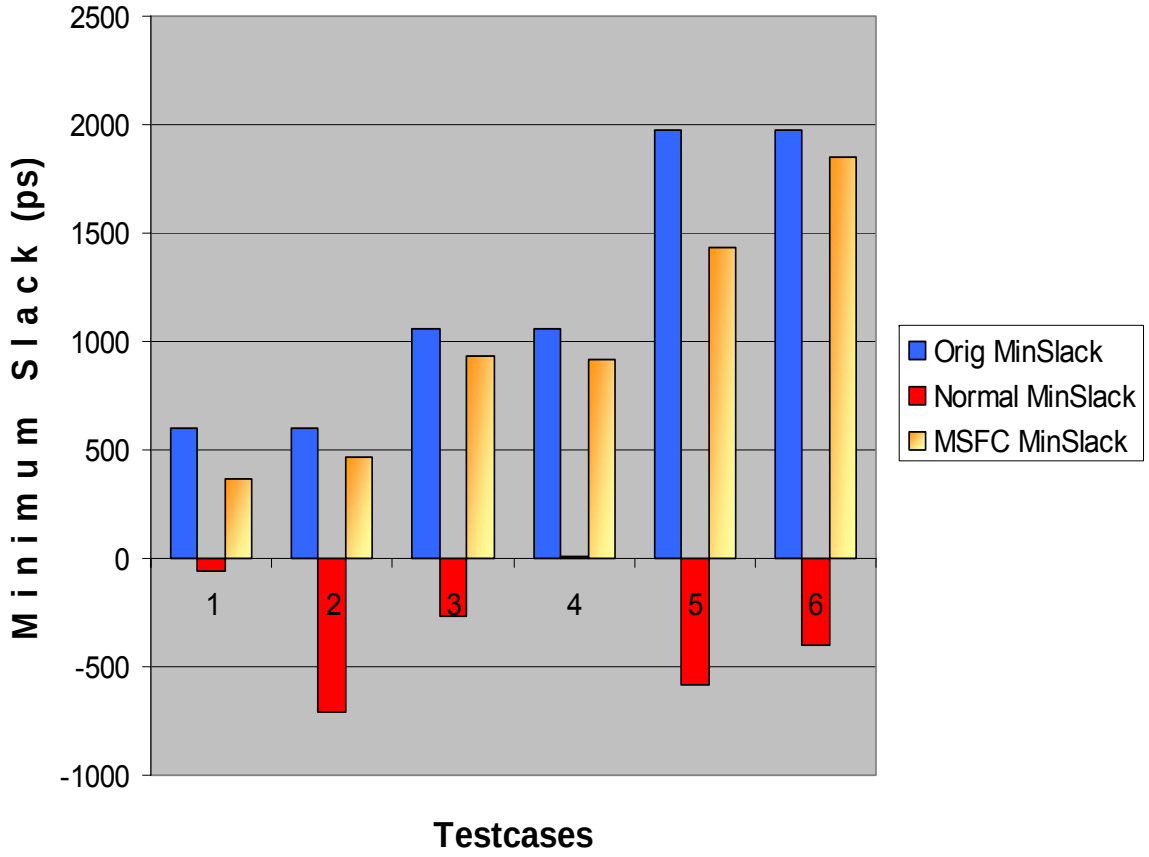
Metric	*Non-optimized*	*Optimized*	***Improvement***
Shot Count	23491105	17424169	26%
OPC Runtime (seconds, wall time)	12353	7805	37%
File size (bytes, gzipped)	168816506	136117133	19%

Example: Litho Simulation Informs Design Closure



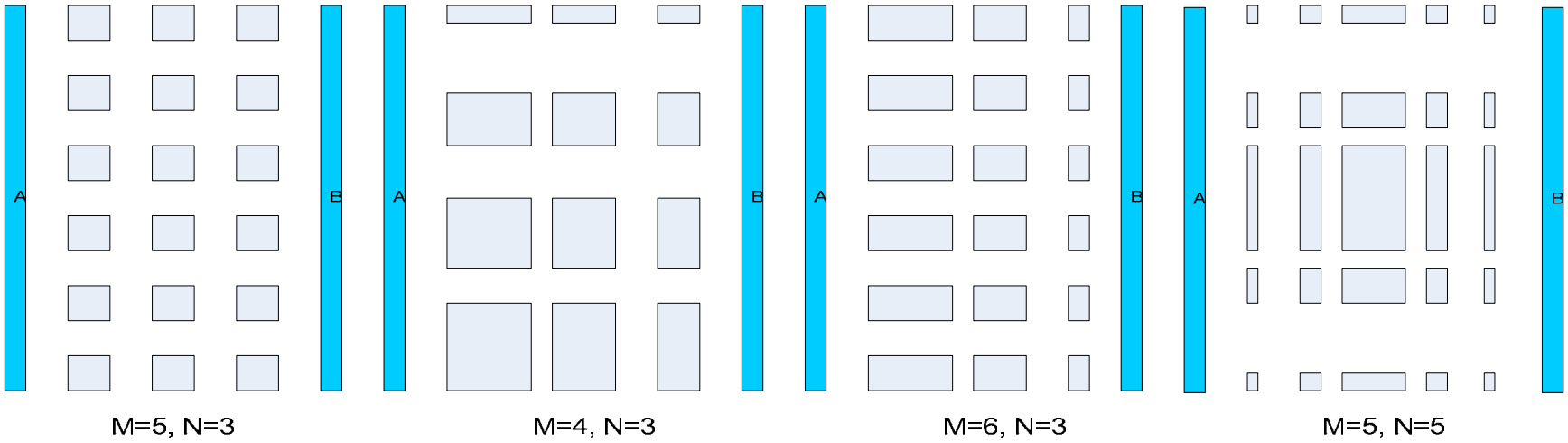
- Manufactured shapes (yellow outline) can deviate from drawn shapes (red) in a meaningful way
- Post-lithography performance analysis brings simulated post-manufacturing shapes into a signoff flow
- Transparency: GDSII, BSIM4, SPEF, .lib, …

Example: Closing the Topography Loop



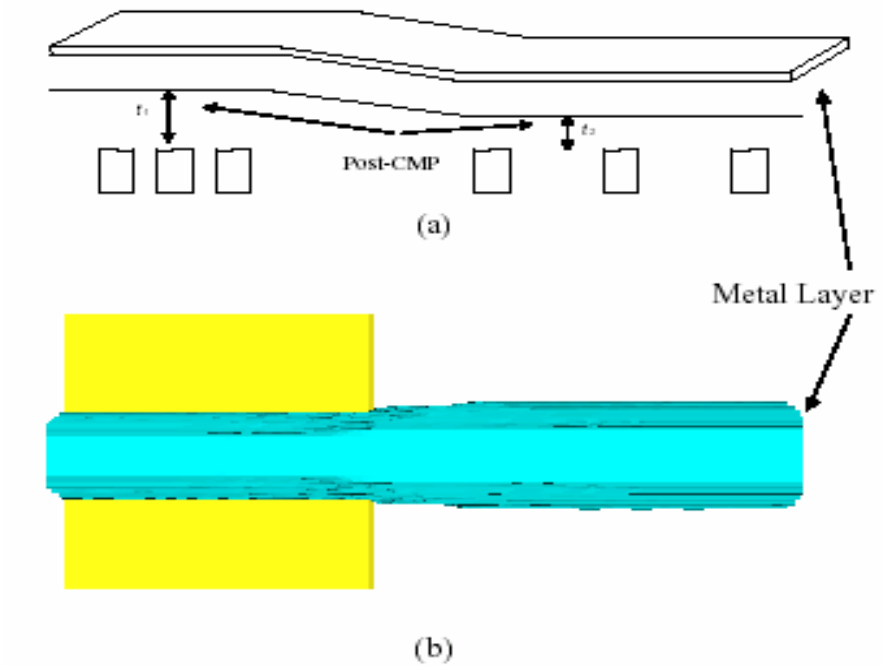
- Performance-driven fill synthesis
- Driven by CMP simulation and timing / SI closure
- Co-optimize fill pattern, interconnect design

Example: Impact of Fill Pattern Choice



How much can the fill pattern affect total capacitance and coupling capacitance? [VMIC-2004, SPIE-2005]

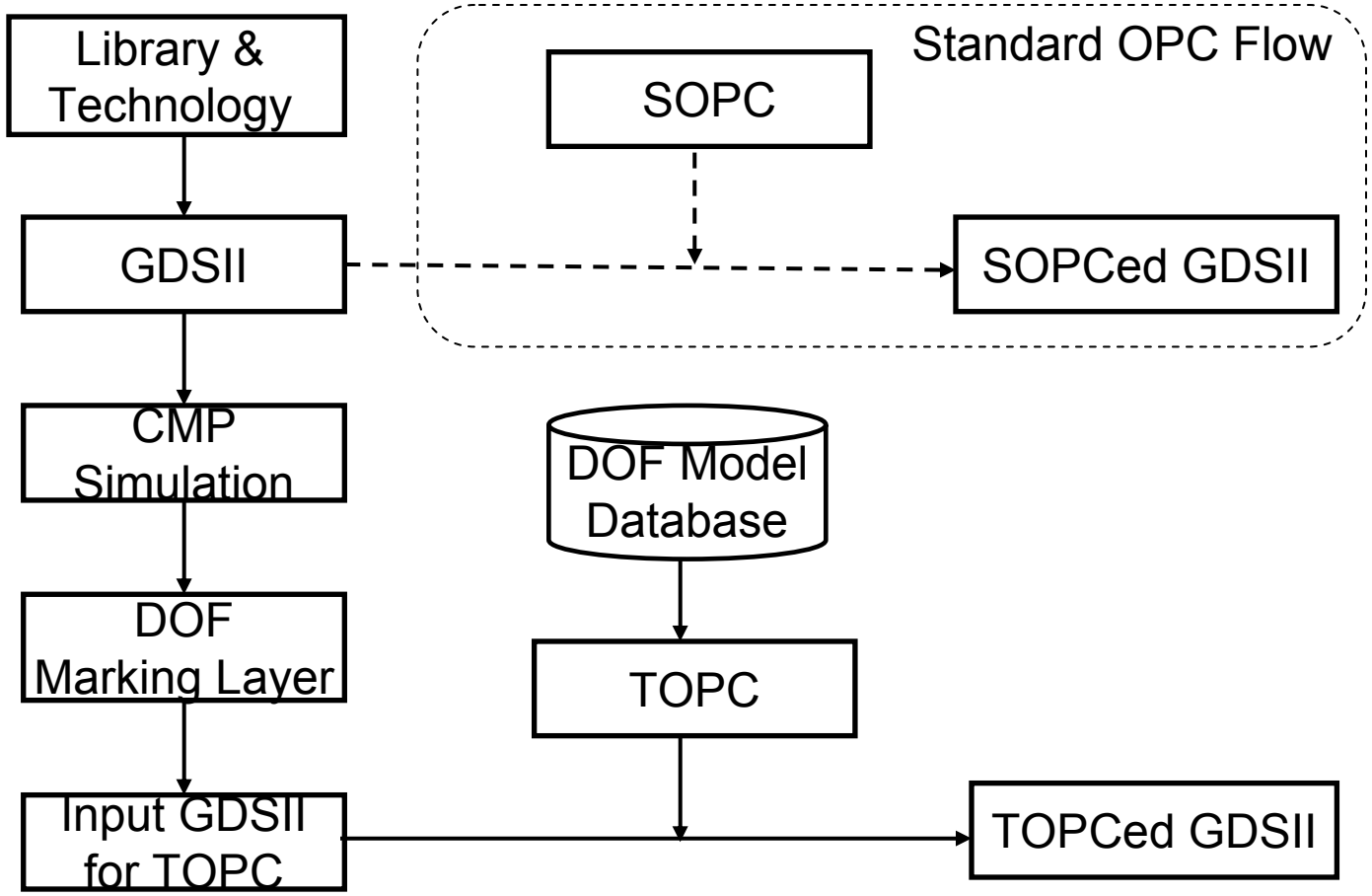
Problem: CD Variation Due To Topography



- Side view showing thickness variation over regions with dense and sparse layout.
- Top view showing CD variation when a line is patterned over a region with uneven wafer topography, i.e., under conditions of varying defocus.

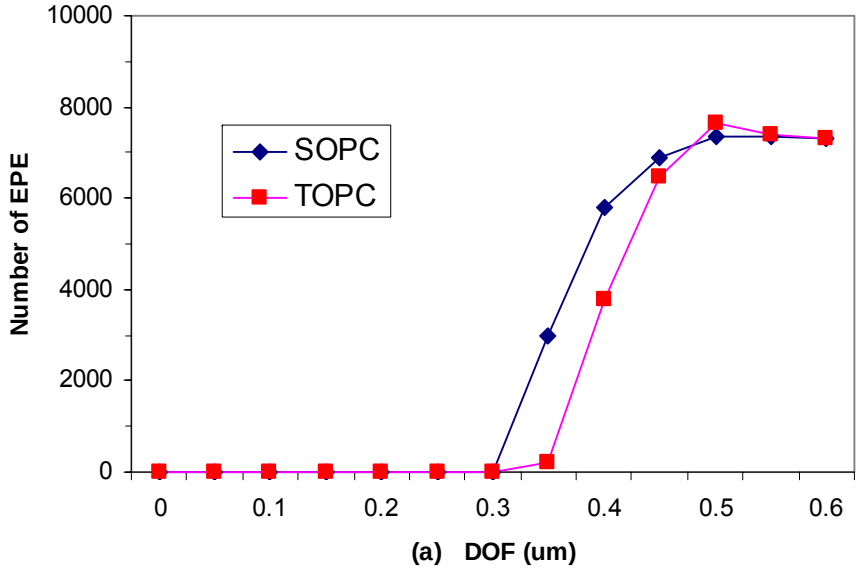
Need OPC that is aware of post-CMP topography variation

Topography-Aware OPC Flow

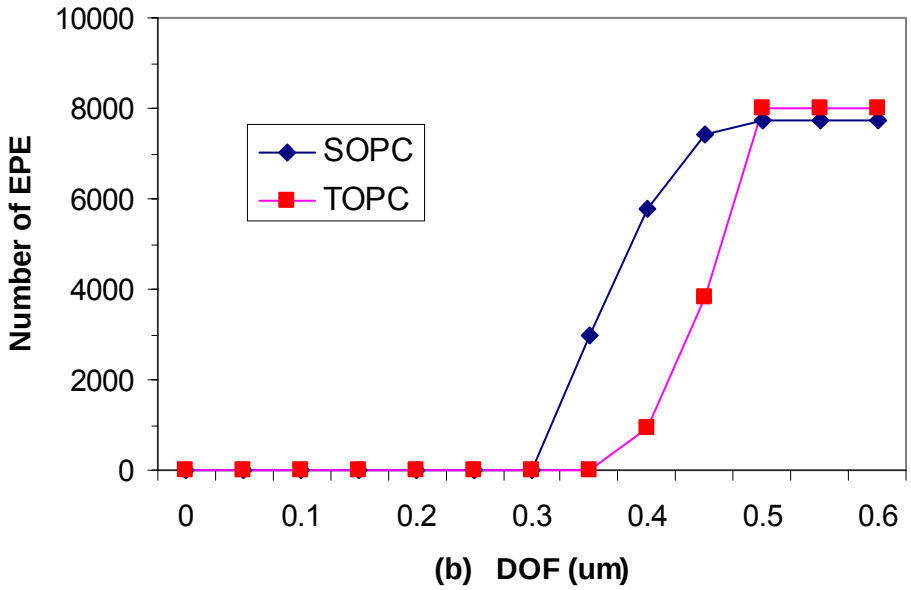


- Map of thickness variation from CMP simulation is converted to defocus marking layers and fed as GDSII for TOPC [PMJ-2005]

Impact



CASE I : 53% improvement

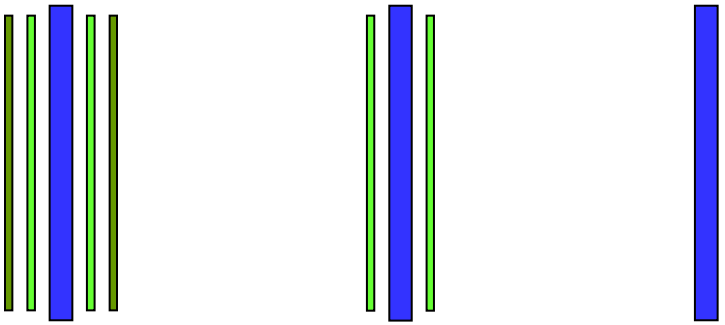


CASE II : 90% improvement

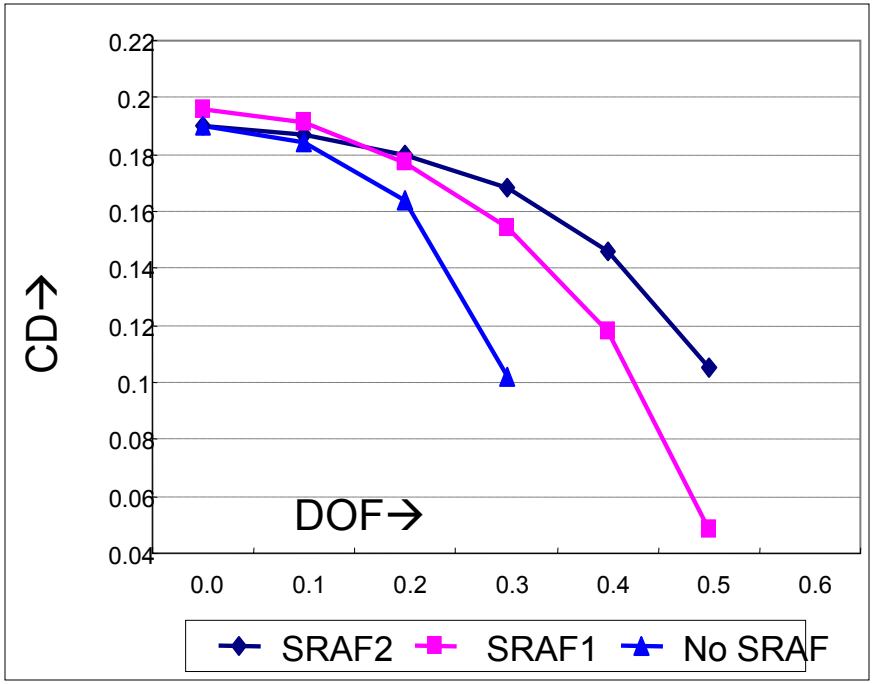
- Up to 90% reduction in edge placement errors
- Improvement in process window comes at cost of some data volume and OPC runtime increase

Example: Placement for Depth of Focus

SB = Scattering Bar ≡ SRAF



2 SB **1 SB** **W/O SB**

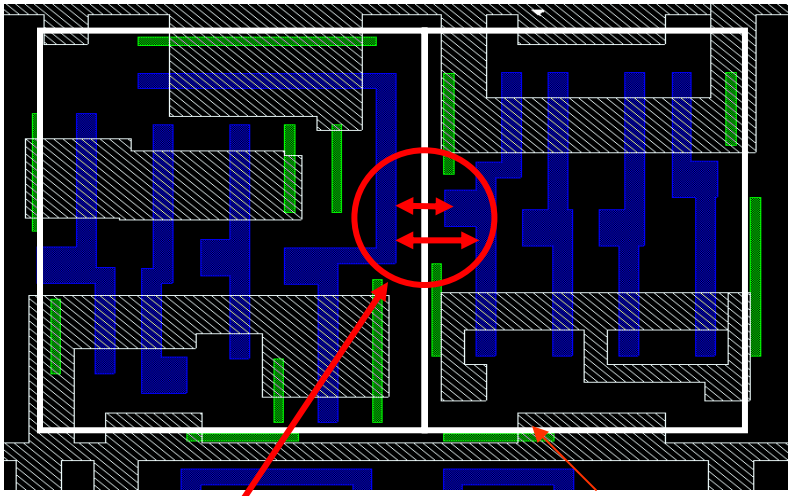


Thanks: Chul-Hong Park, UCSD

Problem: Layout Composability

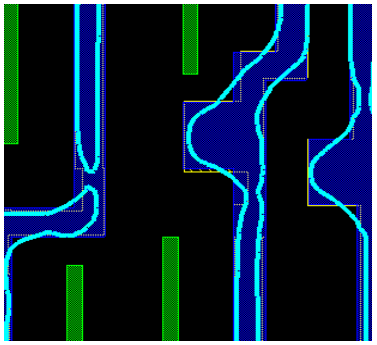
- Feature spacings are restricted to a small set
- Two components needed:
  - Assist-correct library layouts → Inter-device spacing within standard cells → Intelligent library design
  - Assist-correct placement → space between cells needs to be adjusted → Intelligent whitespace management

Detailed Placement Makes Mistakes

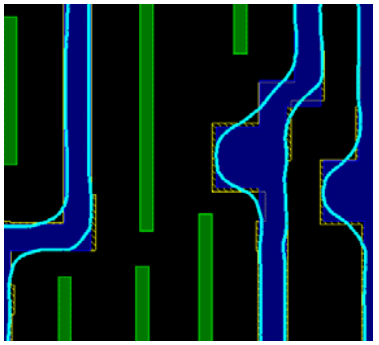


Forbidden pitch

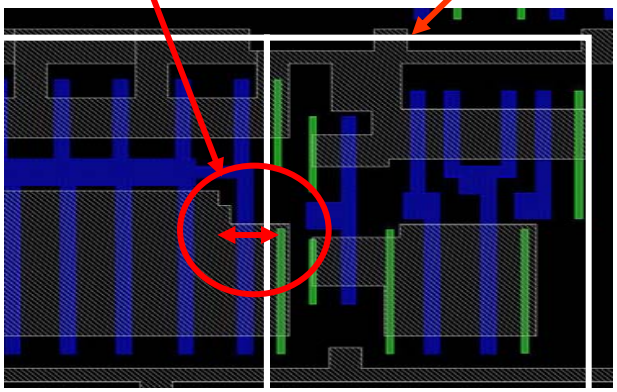
Cell boundary

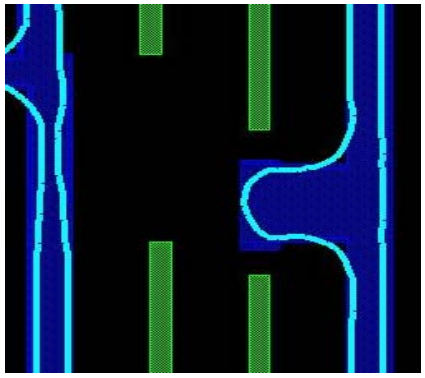


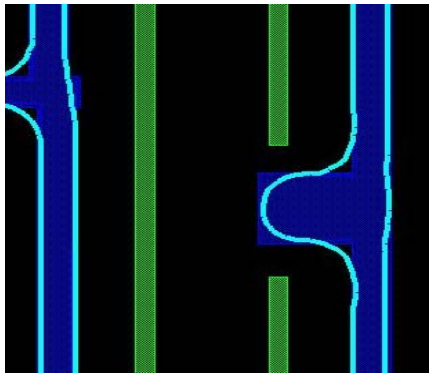
Before AFCorr



After AFCorr

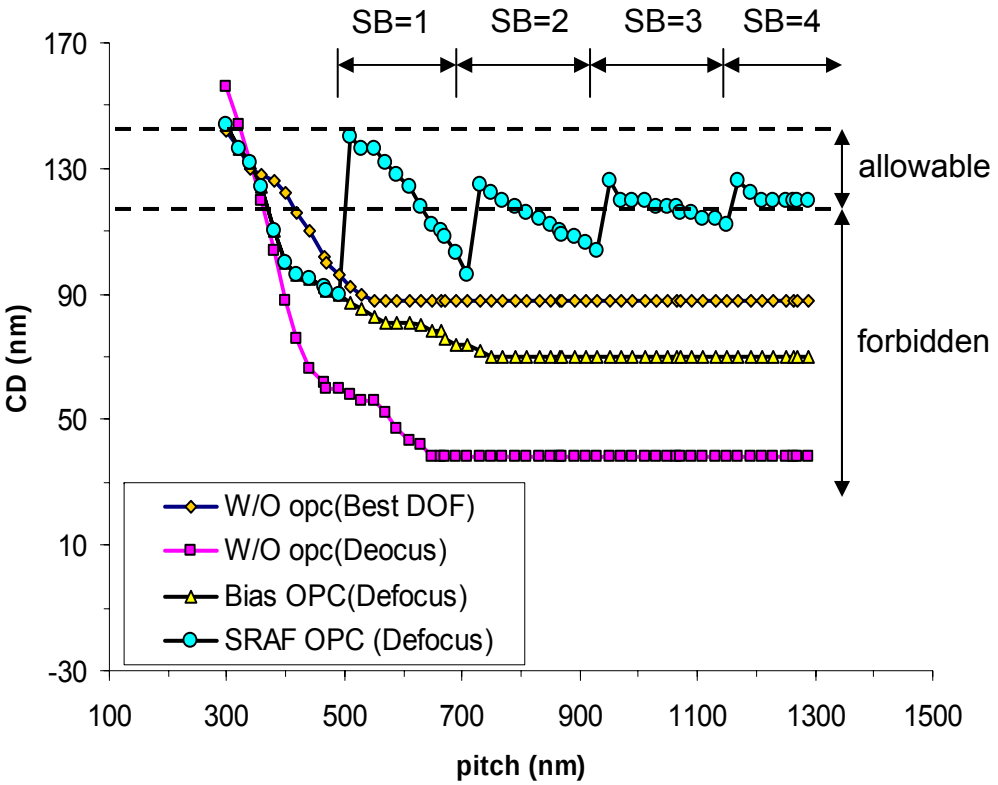






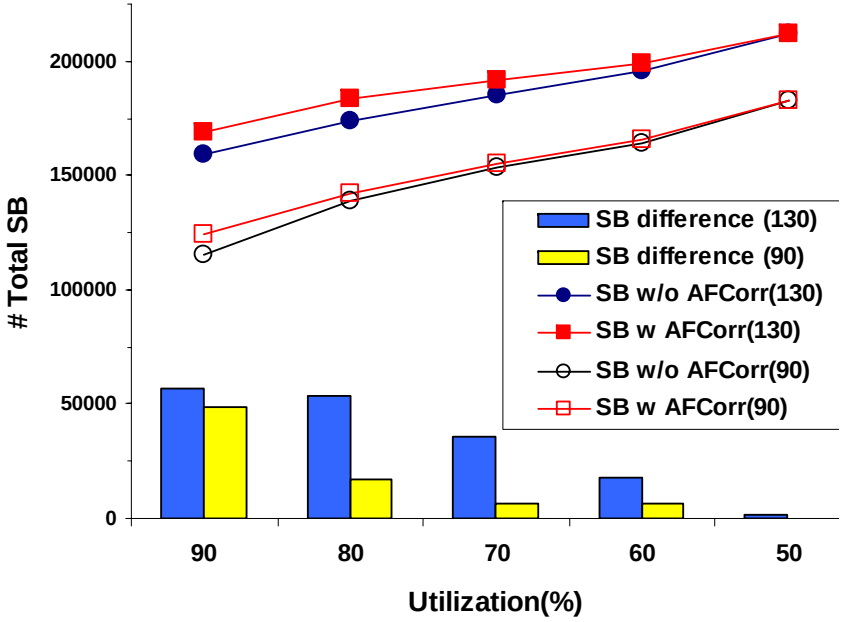
Forbidden Pitch Rules

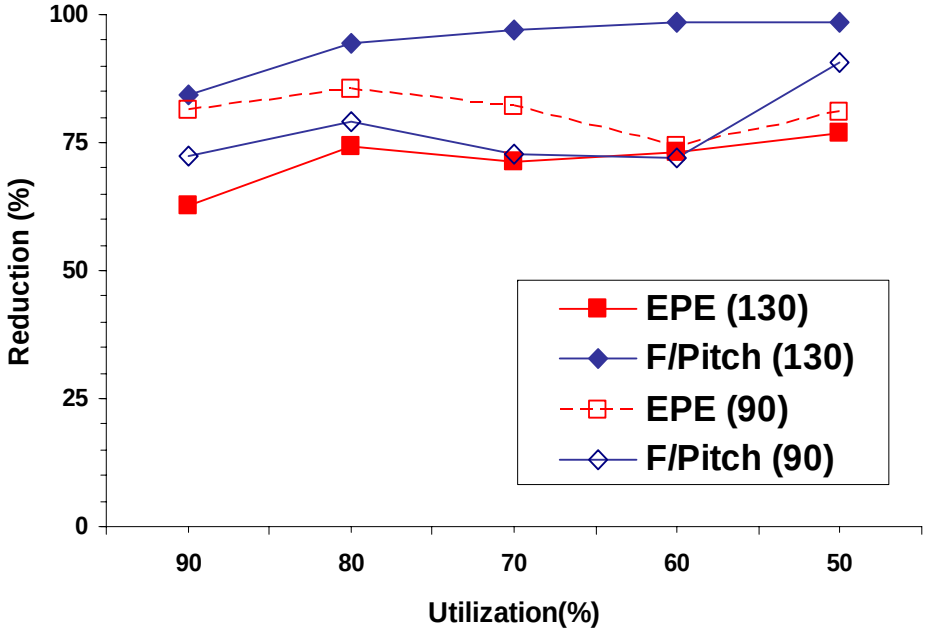
	Pitch (X:um)
#SRAF = 0	0<=X<0.51
#SRAF = 1	0.51<=X<0.73
#SRAF = 2	0.73<=X<0.95
#SRAF = 3	0.95<=X<1.17
#SRAF = 4	1.17<=X



	Forbidden pitches
Bias OPC	[0.37, ∞]
SRAF OPC	[0.37, 0.509], [0.635, 0.729],[0.82, 0.949],[1.09, 1.16]

Assist-Feature-Correct (AFCORR) Placement



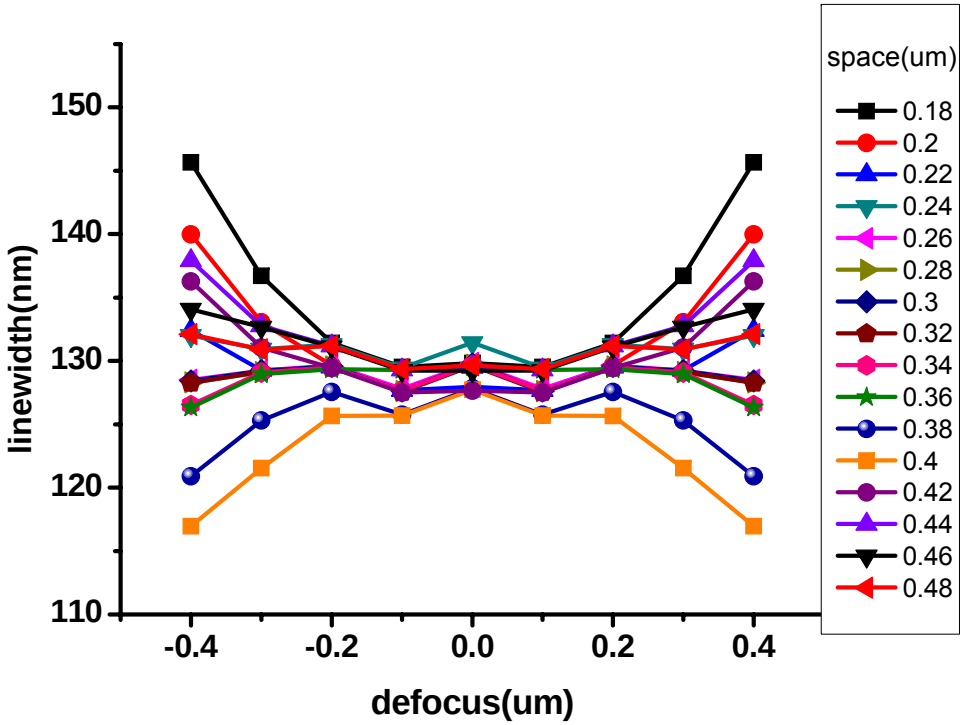


- #SRAFs increases due to AFCorr
  - Obviously, less so with low utilizations
- #high EPE and forbidden pitch instances decreases
  - For both 130nm and 90nm designs
  - Latest data: nearly 100% reductions

Example: Systematic vs. Random Variation

- Today, systematic variation is lumped in with "random"
  - → "uncontrollable variability"
  - → "need for probabilistic and statistical design"
- Say this 5 times, slowly:
  - If it is **systematic**, it can be **modeled**
  - If it can be **modeled**, it can be **predicted**
  - If it can be **predicted**, it can be **compensated**

Problem: Linewidth Variation With Defocus

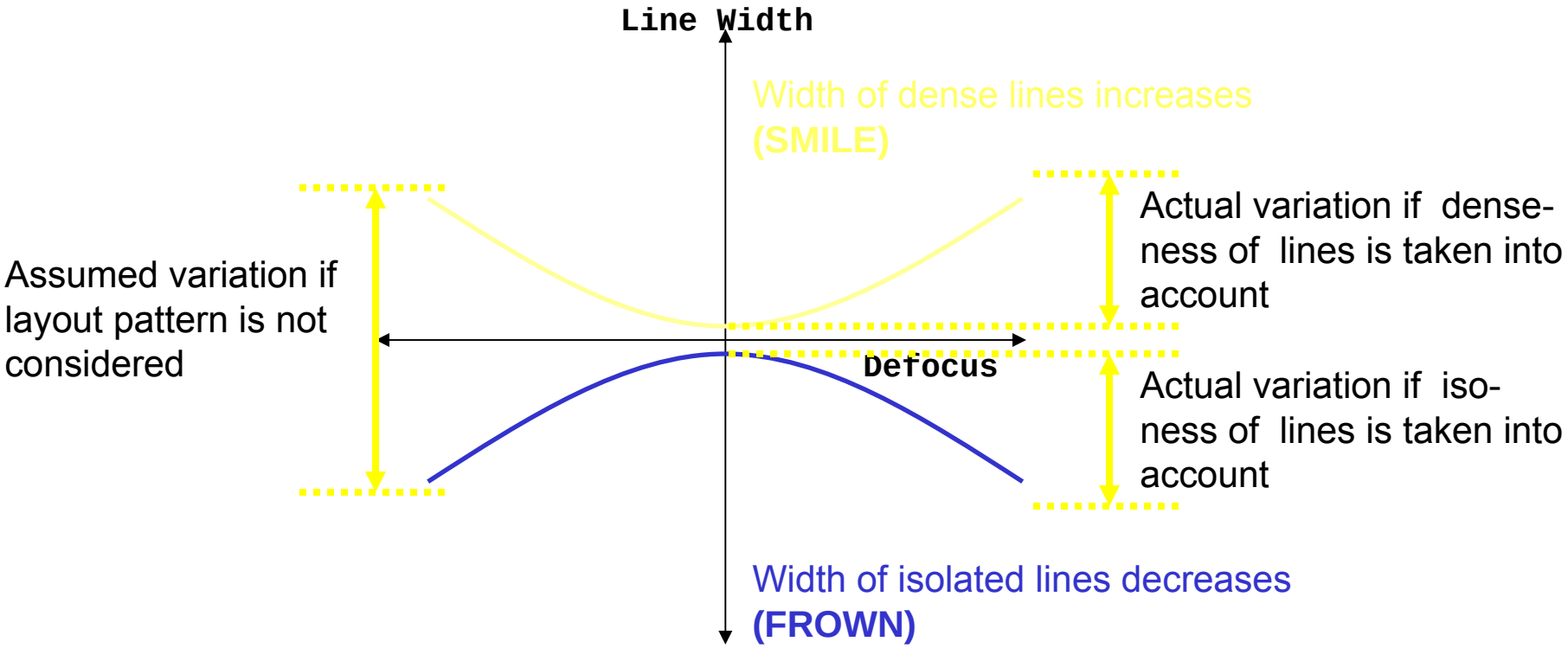


Parameters

λ(wavelength)	248nm
NA	0.7
Illumination type	Annular
SB placement	180nm
SB width	60nm
Nominal CD	130nm

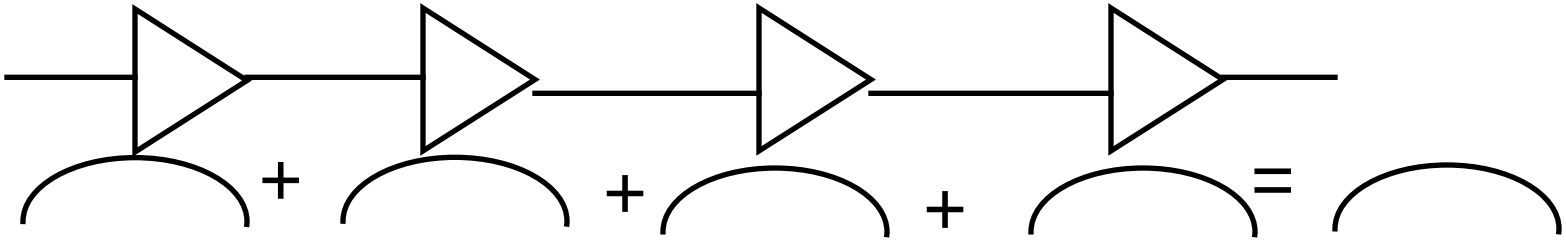
- 3 different ranges of spacings
  - **Dense** : 180nm ~ 260nm
  - **Self-compensated** : 280nm ~ 360nm (within +/- 4nm CD band)
  - **Iso** : 360nm ~ 400nm
- "Most-iso" linewidth 11% under nominal at 0.4um defocus
- "Most-dense" linewidth 13% above nominal

Today: Variability Pessimism



- Extract and exploit systematic variation
  - → Less worst-casing and over-design
  - → Valuable in design for leakage

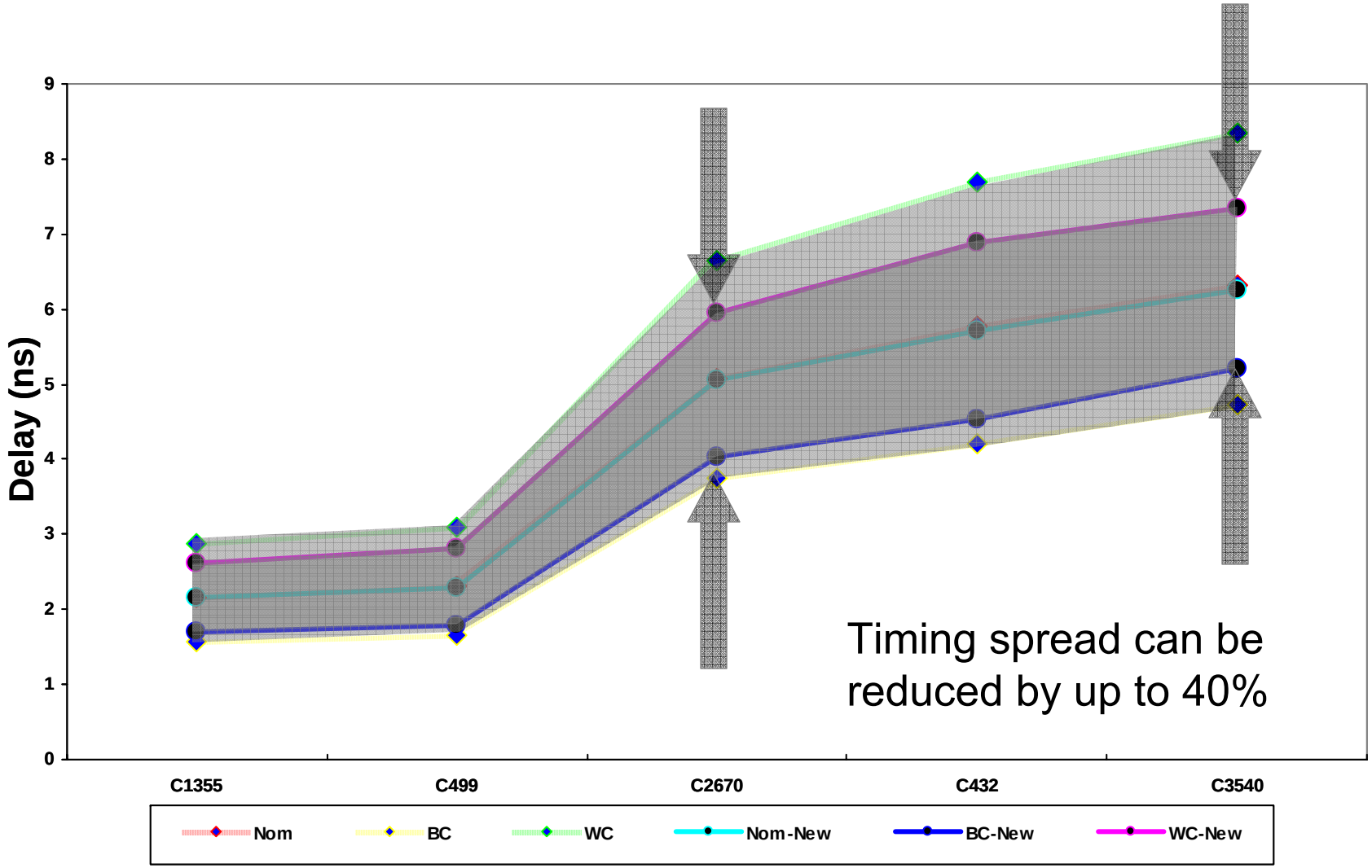
Defocus-Aware STA



- If all timing arcs frown, then the path delay will always decrease through focus → one corner is trimmed off !
- If slopes of smile/frown curves are known → circuit sensitivity to focus variation can be computed

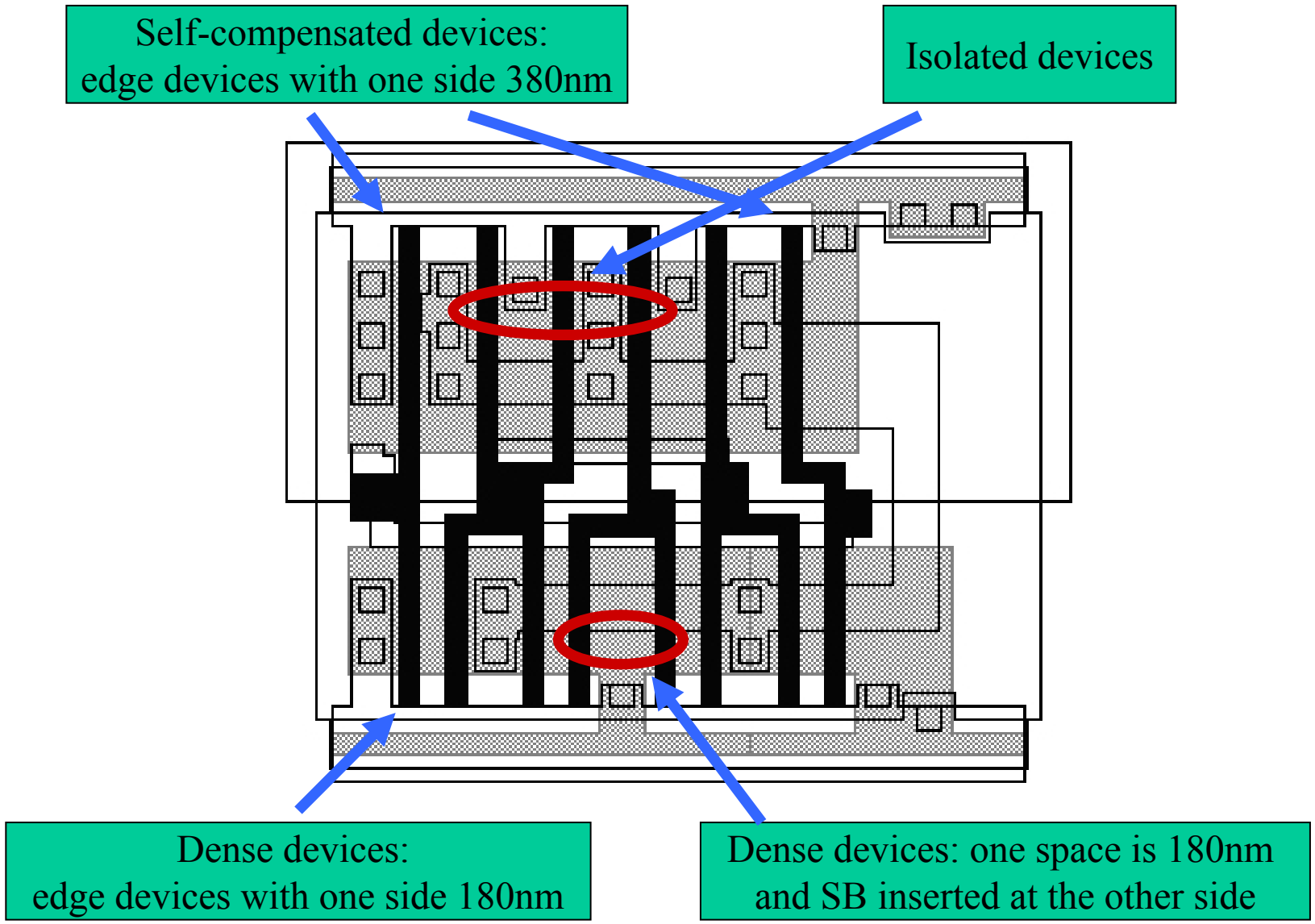
Heng/Gupta, DAC-2004

Impact of Systematic Variation Compensation

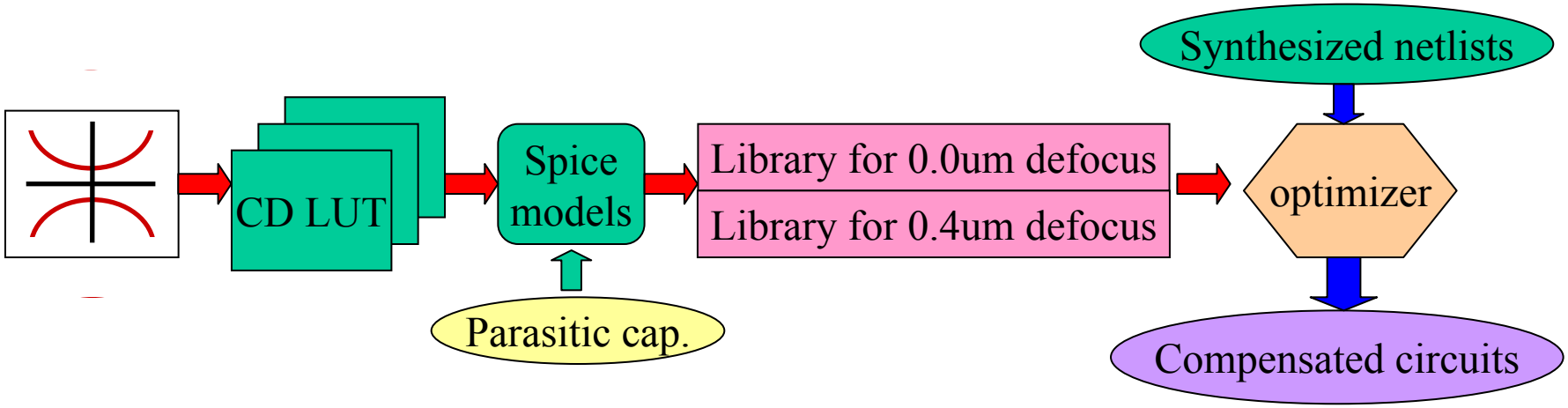


Heng/Gupta, DAC-2004

Sample Cell Layout (NAND2x6)

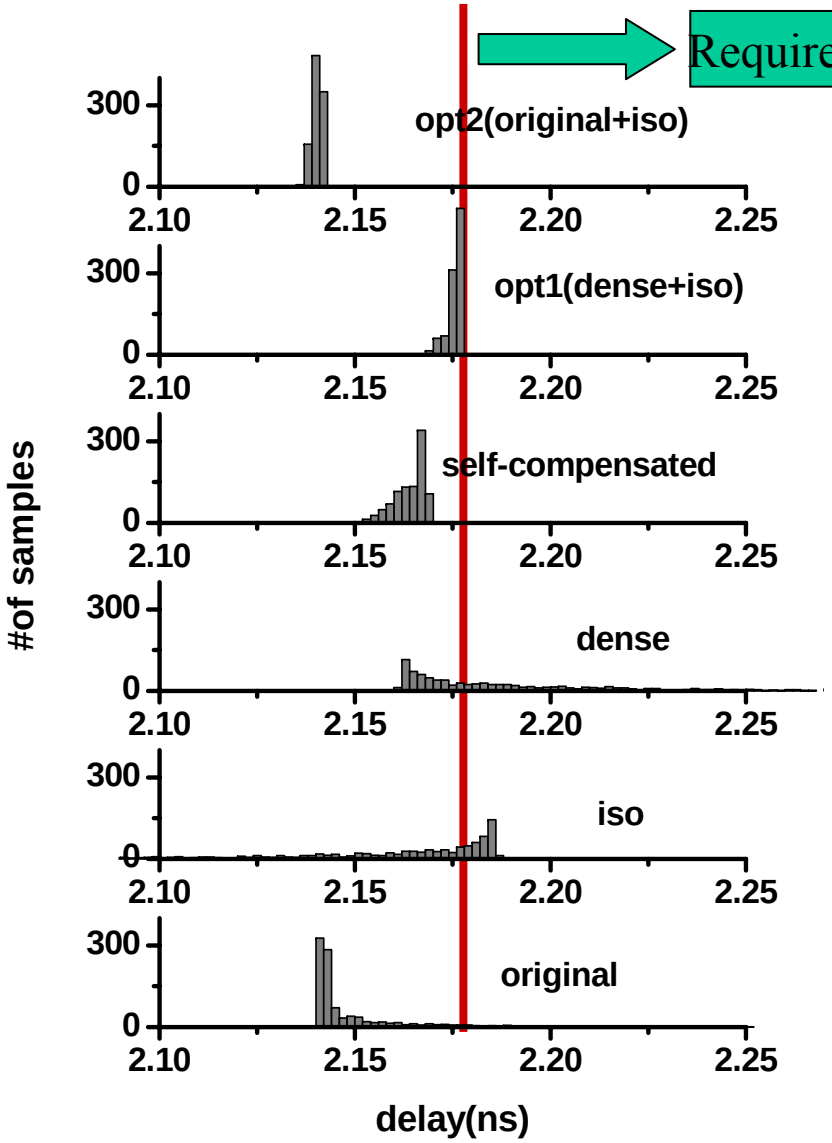


Self-Compensating Design Flow



- CD look-up table (LUT) gives *Leff* at different spacing (S) and focus (F)
  - *CD ~ f(Left Space, Right Space, Focus)*
- Library: 4 variants of each cell (original, iso, dense, self-compensated)
- Self-compensating design
  - (1) Self-compensated cells
  - (2) Optimization (self-compensated physical design)
    - Dense + iso design
    - Original + iso design
- Sensitivity-based approach: minimize area penalty while instantiating *"iso"* versions of *"dense"* cells to meet timing

Distribution of Delay Under Defocus



- Monte-Carlo simulation with 1000 trials
- Normal distribution of focus with mean=0.0um and 3σ=0.4um
- C3540 benchmark circuit with required time 2.177ns
- 2 optimization strategies give tighter distribution than self-compensated cells option
- Some tail over required time in Original library case not seen in the plot

Summary

- "DFM" success depends on real, transparent links between IC design and manufacturing
  - Today: many failures of imagination
  - Transparent solutions are possible
- Concrete examples
  - Design intent-driven OPC
  - Post-litho simulation performance closure
  - Topography-aware (everything)
  - Detailed placement for depth of focus
  - Systematic variation: model, predict, compensate
    - Example: variational timing analysis and self-compensating design for through-focus CD variation