Closing the Gap between Manufacturing and Design

Wolfgang Fichtner, Dipu Pramanik and Lars Bomholt
Synopsys Inc, Mt View, CA

Over the past decade, the EDA industry has evolved from offering selections of a few point tools to providing completely integrated software platforms that provide solutions from RTL to silicon.

For the 90nm node and beyond, issues with manufacturability and yield force the EDA industry and manufacturing to move closer together. In particular, process and device information that affect functionality and yield need to be incorporated into the design flow, addressing more comprehensively issues of Design for Manufacturability (DFM) and Yield (DFY).

At present, DFM focuses mostly on resolution enhancement techniques such as OPC, completely neglecting other factors like process and device variability. In yield terms, this implies that the current focus only covers parts of the parametric yield issues.

For true DFM and DFY, it is necessary to look beyond printability issues and include process variability in the design process. Manufacturability issues also require a tighter union of design and manufacturing. The information needed by designers includes layout sensitivities as well as the effect of process variability on the electrical characteristics of devices and interconnects. At the 65nm node the variability will increase significantly as a result of feature scaling and the introduction of new materials and innovative techniques such as strain engineering.

TCAD (Technology CAD) addresses these problems as it complements silicon metrology data with accurate calibrated process and device models. In combination with wafer data, the strength of TCAD lies in the accurate prediction of device and interconnect variability due to layout as well as due to random variations in the process. Variability information can then be incorporated into the design tools through appropriate statistical compact models. Ultimately, this leads to an improved design flow that addresses manufacturability issues in a comprehensive way.

Beyond traditional process and device modeling and optimization and beyond the use in DFM, TCAD also provides unique advantages in manufacturing. In a "Manufacturing for Design" approach, TCAD can be used for "global" advanced process control (APC), helping the manufacturing engineer optimize parametric product yield for specific designs without having to understand the details of the design itself.

TCAD

Closing the Gap between Manufacturing and Design

What is TCAD?

TCAD for Manufacturing

TCAD-assisted DFM Flow

Extending DFM from lithography to complete frontend and backend processing

W. Fichtner

Lars Bomholt

Dipu Pramanik

SYNOPSYS®

Outline

- What is TCAD?
- The view of industry - yield issues in deep submicron manufacturing
- TCAD for Manufacturing - the bridge from processing to design
- TCAD and design for manufacturability
- TCAD-assisted DFM flow

Outline

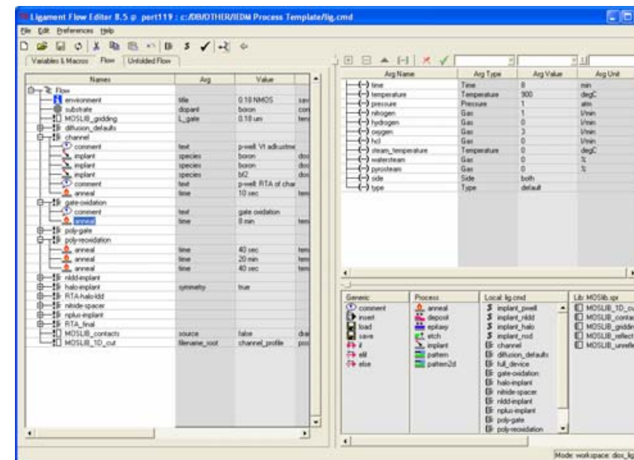
- **What is TCAD?**
- Status of Synopsys TCAD and roadmap
- The view of industry - yield issues in deep submicron manufacturing
- TCAD for Manufacturing - the bridge from processing to design
- What is design for manufacturability?
- TCAD-assisted DFM flow

What is TCAD? – A High-Level Definition

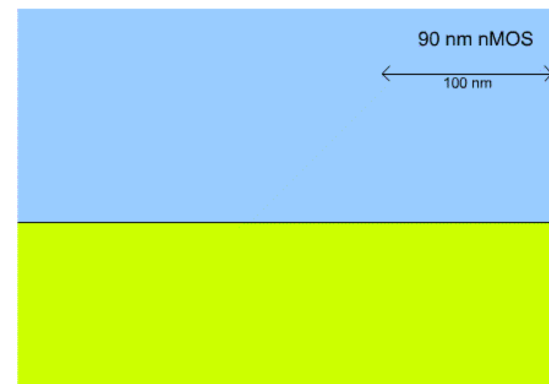
- TCAD stands for *Technology Computer Aided Design*
- TCAD represents our physical understanding of processes and devices in terms of computer models of semiconductor physics
- TCAD is used to design, analyze and optimize semiconductor technologies and devices with fundamental and accurate simulation models
- *Process simulation* models semiconductor manufacturing processes. The simulation starts with the bare wafer and ends with device structures. Process simulation includes lithography.
- *Device simulation* models the semiconductor operation. The electrical behavior can be characterized and SPICE parameters extracted. Device simulation extends to backend extraction and it can be linked with classical circuit and system simulation.

Process Simulation

- Process simulation models manufacturing steps such as implantation, diffusion, oxidation, etching, deposition, lithography,…
- Simulation starting from flow description and layout
- Focused on front-end process steps
- Implantation, diffusion and oxidation, and lithography are calibrated and highly predictive
- Etching and deposition are typically modeled geometrically



TCAD process flow editor

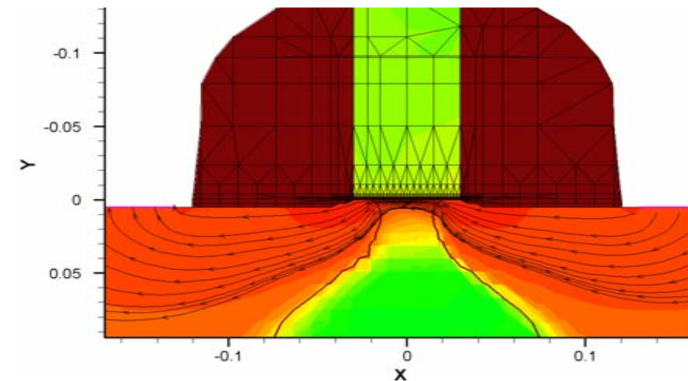


Dopant distribution in 100nm device

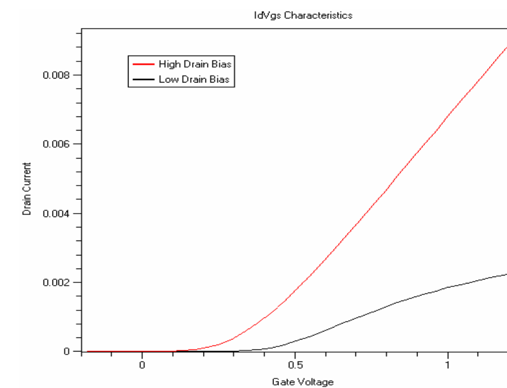
© 2005 Synopsys, Inc. (5) CONFIDENTIAL – DO NOT DISTRIBUTE

Device Simulation

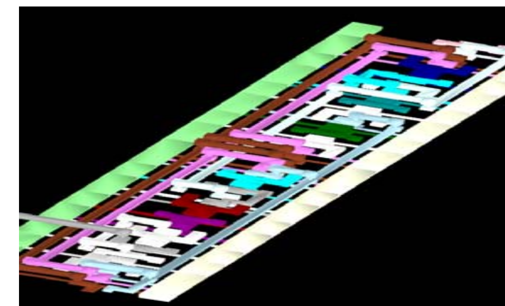
- Device simulation models the electrical, optical, mechanical and magnetic behavior of semiconductor devices
- Device simulation is typically performed on structures created by process simulation
- Simulation modes are static, time-dependent, large and small signal frequency dependent, and they include noise modeling
- From device simulation results, highly accurate CAD models can be extracted
- Device simulation includes RLC extraction of the backend



Simulated current density and flow lines in 100nm device



Simulated electrical characteristics

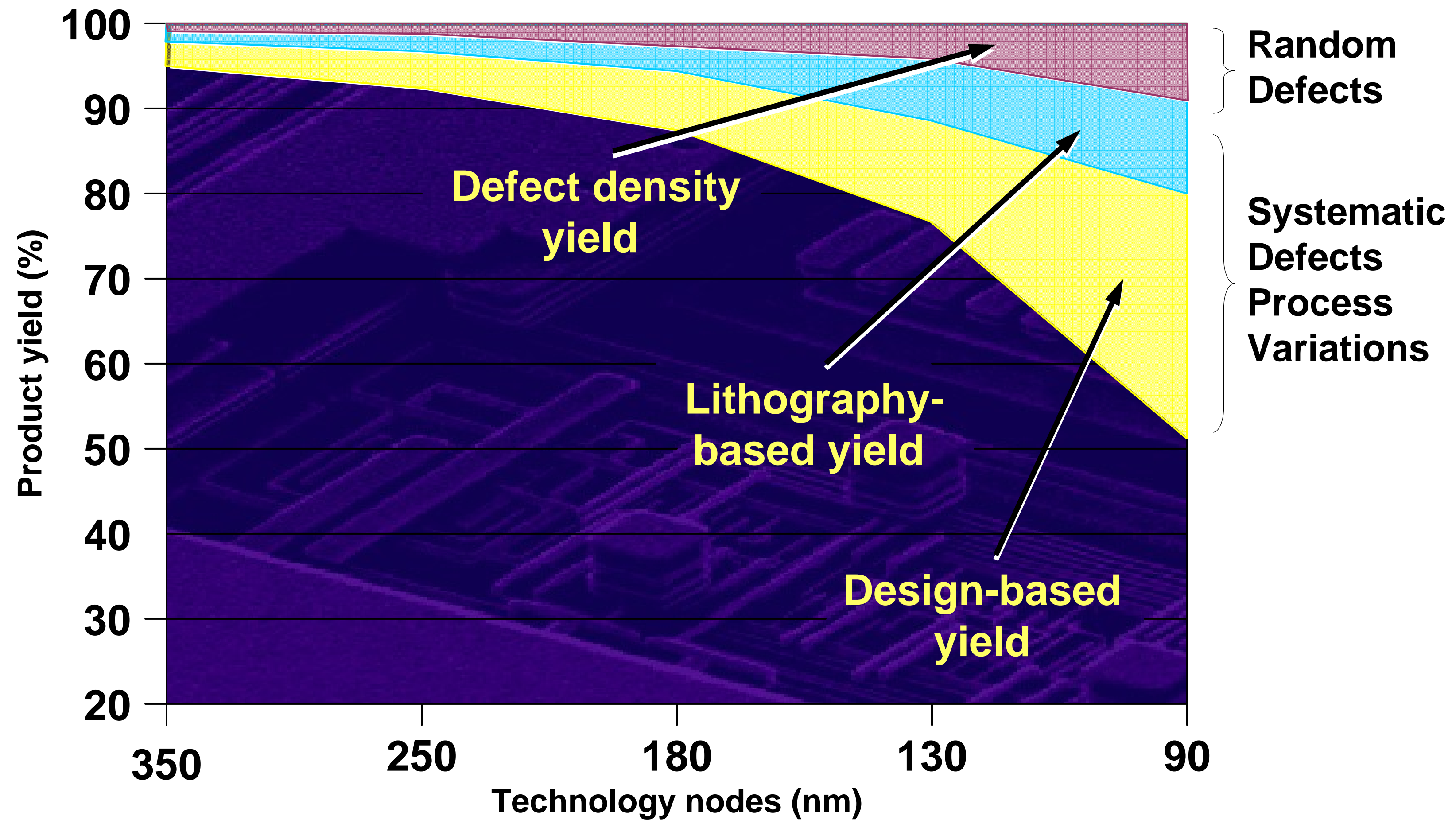


Outline

- What is TCAD?
- **The view of industry - yield issues in deep submicron manufacturing**
- TCAD for Manufacturing - the bridge from processing to design
- What is design for manufacturability?
- TCAD-assisted DFM flow

SYNOPSYS®

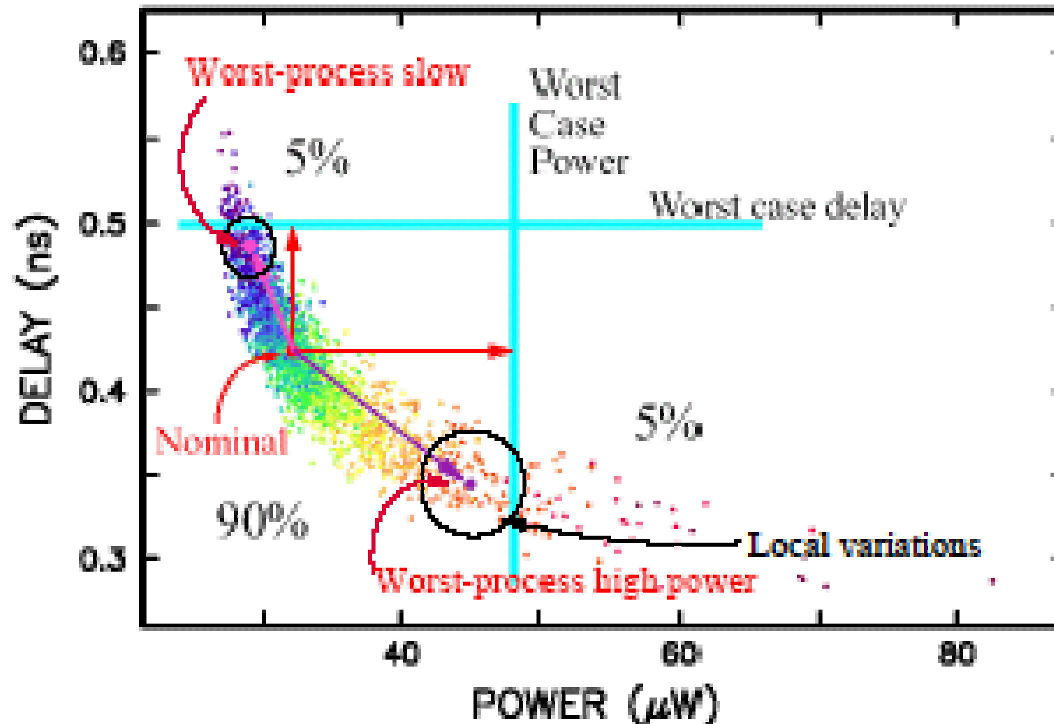
The Old Rules Don't Apply



New phenomena dominate total yield loss

© 2005 Synopsys, Inc. (8) CONFIDENTIAL – DO NOT DISTRIBUTE

Yield-Oriented Design (IBM Data)



Nominal design point must balance yield loss from opposing design targets (e.g., power and delay). Worst-process points must be chosen carefully to balance likelihood of global variation reaching this point against probability of local variations causing design to fail.

© 2005 Synopsys, Inc. (9) CONFIDENTIAL – DO NOT DISTRIBUTE
SYNOPSYS®

ITRS Roadmap

2004

2009

Table 77a Lithography Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM							
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
Contact in resist (nm)	130	110	100	90	80	70	60
Contact after etch (nm)	115	100	90	80	70	65	55
Overlay	35	32	28	25	23	21	19
CD control (3 sigma) (nm)	12.2	11.0	9.8	8.6	8.0	7.0	6.1
MPU							
MPU/ASCI Metal 1 (M1) ½ pitch (nm)	120	107	95	85	76	67	60
MPU ½ Pitch (nm) (uncontacted gate)	107	90	80	70	65	57	50
MPU gate in resist (nm)	◆ 65	53	45	40	35	32	28
MPU gate length after etch (nm)	45	37	32	28	25	22	20
Contact in resist (nm)	130	122	100	90	80	75	60
Contact after etch (nm)	120	107	95	85	76	67	60
Gate CD control (3 sigma) (nm)	◆ 4.0	3.3	2.9	2.5	2.2	2.0	1.8
ASIC/LP							
ASIC ½ Pitch (nm) (uncontacted gate)	107	90	80	70	65	57	50
ASIC/LP gate in resist (nm)	90	75	65	53	45	40	36
ASIC/LP gate length after etch (nm)	65	53	45	37	32	28	25
Contact in resist (nm)	130	122	100	90	80	75	60
Contact after etch (nm)	120	107	95	85	76	67	60
CD control (3 sigma) (nm)	5.8	4.7	4.0	3.3	2.9	2.5	2.2

We are now in the yellow and the red zones.

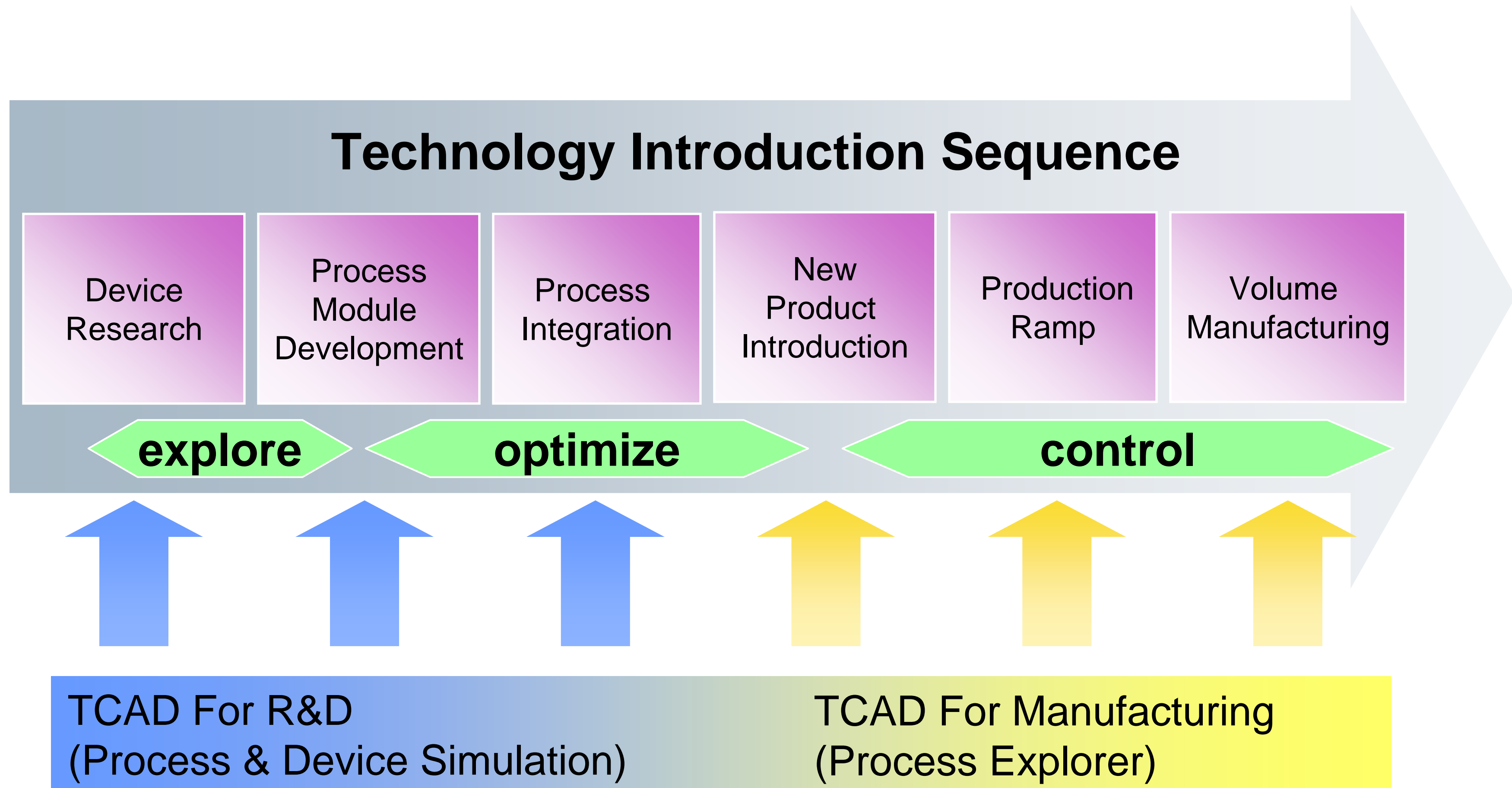
Yellow: Idea exists but no solution for production.

Red: No idea and no solution.

Outline

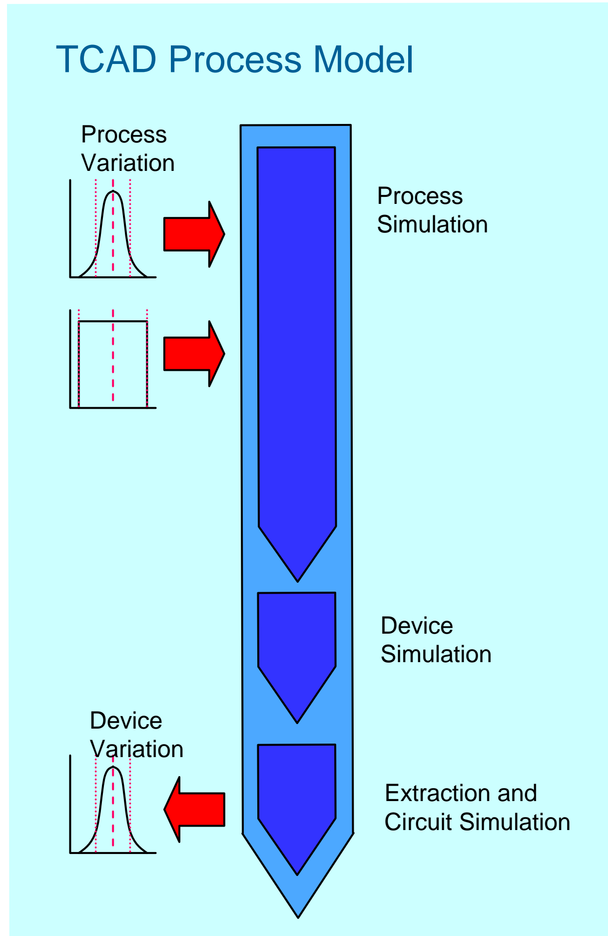
- What is TCAD?
- The view of industry - yield issues in deep submicron manufacturing
- **TCAD for Manufacturing - the bridge from processing to design**
- What is design for manufacturability?
- TCAD-assisted DFM flow

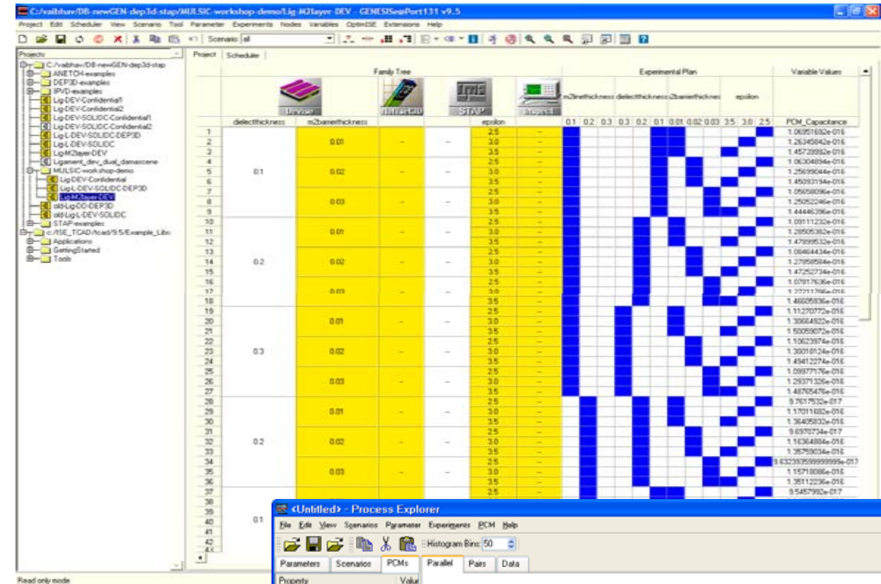
Evolution of TCAD - from research through development and manufacturing



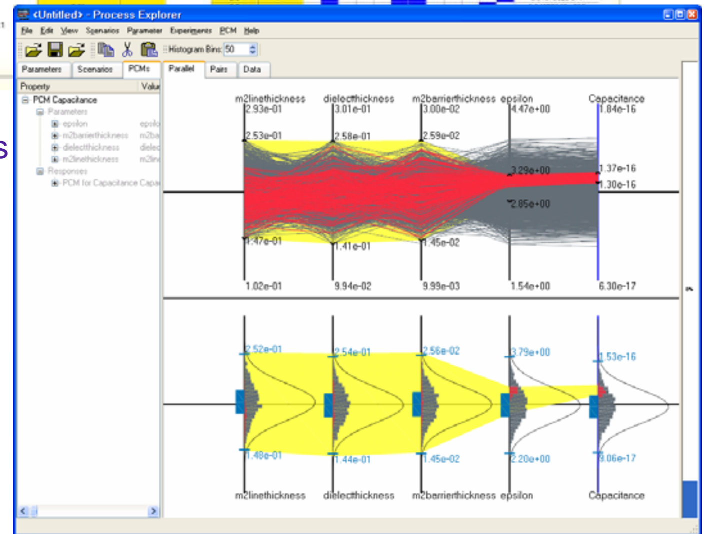
SYNOPSYS®

TCAD "Captures" Process Variability





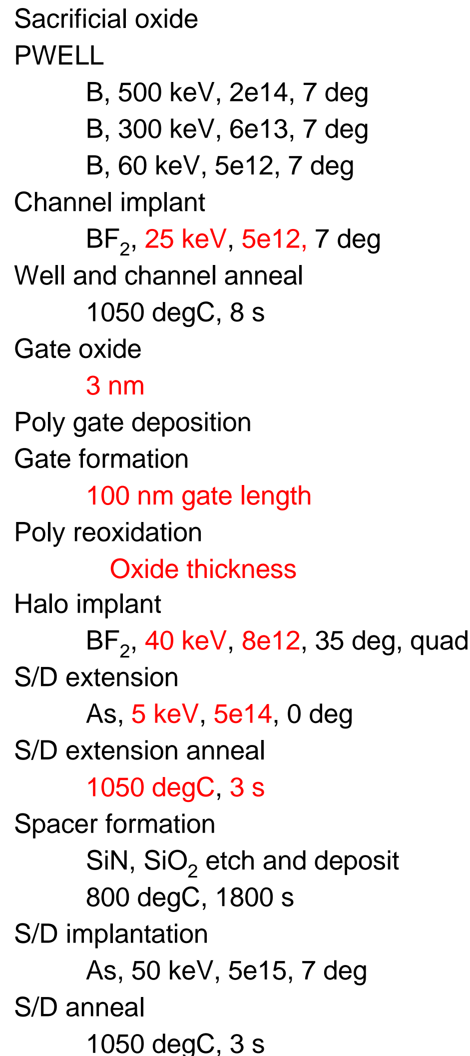
DoE for parametric analysis in GENESISe



Synopsys PCM Explorer for evaluation of process-device relations and yield

Typical TCAD Transistor Simulation

Connects Process to Transistor Device Characteristics



Sample input parameters:

- BF2 implantation energy
- BF2 implantation dose
- Gate length
- Gate sidewall profile
- Gate oxide thickness
- Variation in the gate reoxidation
- Halo angle tilt
- Extension energy
- Extension dose
- Extension tilt
- Extension diffusion time
- Extension diffusion temperature

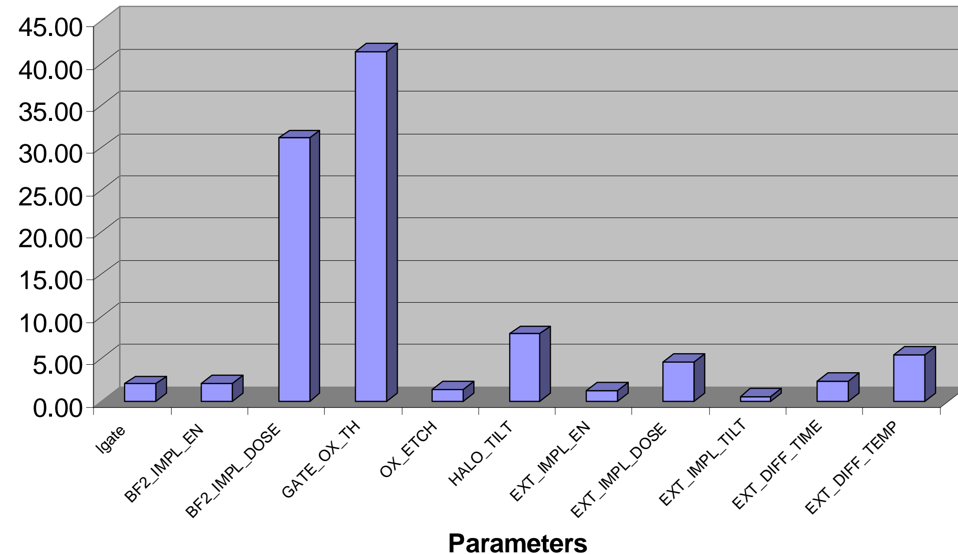
Sample Output parameters:

- VT: Threshold voltage
- Ion: Saturation current
- Ioff: Leakage current
- Transient characteristics, noise etc.
- SPICE parameters
- Circuit performance

Process Screening: Results

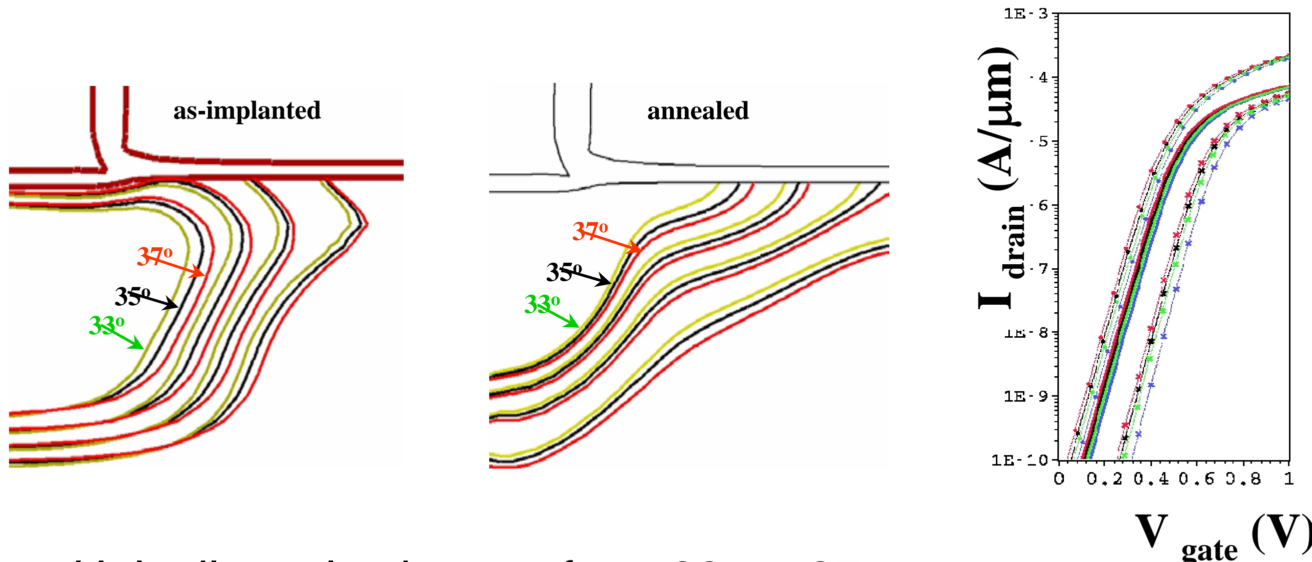
- High dynamic range of results
- More expensive analyses can be made based on a selection of parameters from screening
  - Interaction
  - Sensitivity analysis
  - Statistical analysis

Parameter	Min	Max	Scale	dVT3	dVT5	dION	Screen
Igate	0.1725	0.1875	lin				2.0
BF2_IMPL_EN	24.25	25.75	lin				2.1
BF2_IMPL_DOSE	4.25e12	5.75e12	log				31.1
GATE_OX_TH	2.7	3.3	lin				41.4
OX_ETCH	0.35	0.65	lin				1.4
HALO_TILT	33.5	36.5	lin				7.9
EXT_IMPL_EN	4.85	5.15	lin				1.2
EXT_IMPL_DOSE	4.63E+17	5.38E+17	log				4.6
EXT_IMPL_TILT	-0.75	0.75	lin				0.5
EXT_DIFF_TIME	2.7	3.3	lin				2.3
EXT_DIFF_TEMP	1045	1055	lin				5.4



Example: Halo Implant

Sensitivity analysis of halo implant angle in 0.18µm CMOS

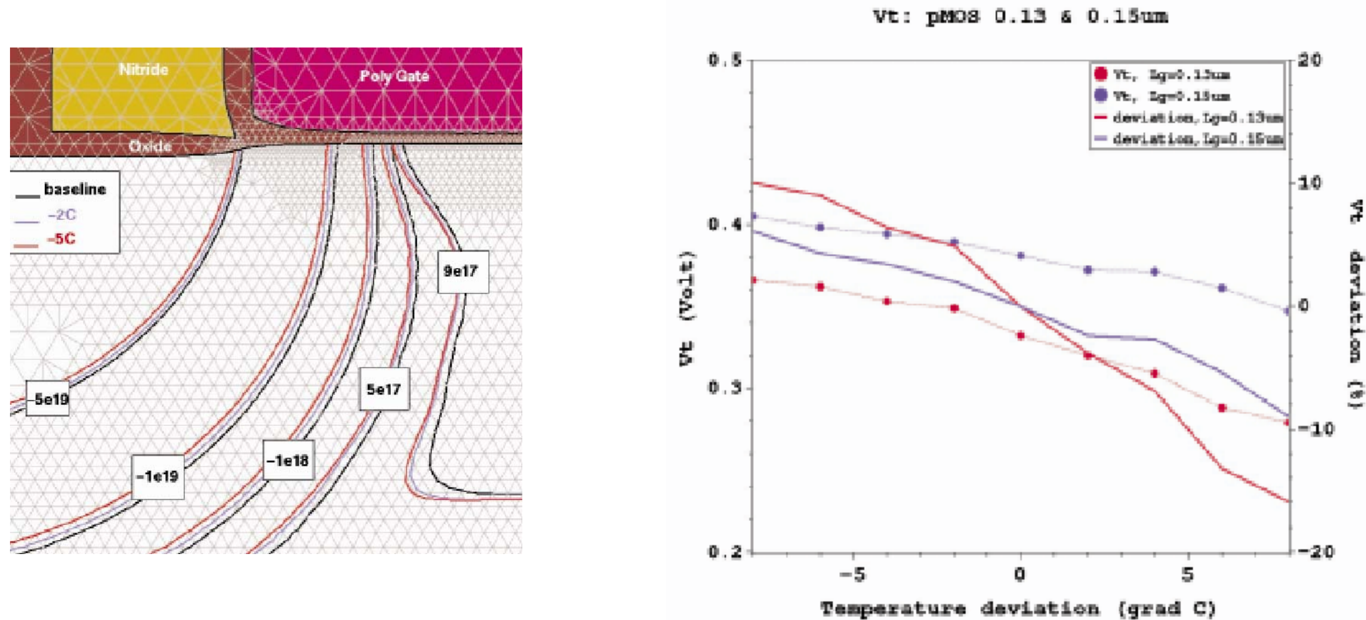


- Halo tilt angle change, from 33º to 37º leads to a decrease in leakage current (60%), DIBL (9%) and small increase in Vt (5%) and body effect (5%)
- Experimental verification of a Vt shift of 1.47%/degree vs. predicted 1.4%/degree
- TCAD is very accurate for parametric analysis

© 2005 Synopsys, Inc. (16) CONFIDENTIAL – DO NOT DISTRIBUTE

Final RPT Temperature Sensitivity

Small temperature variation in final anneal



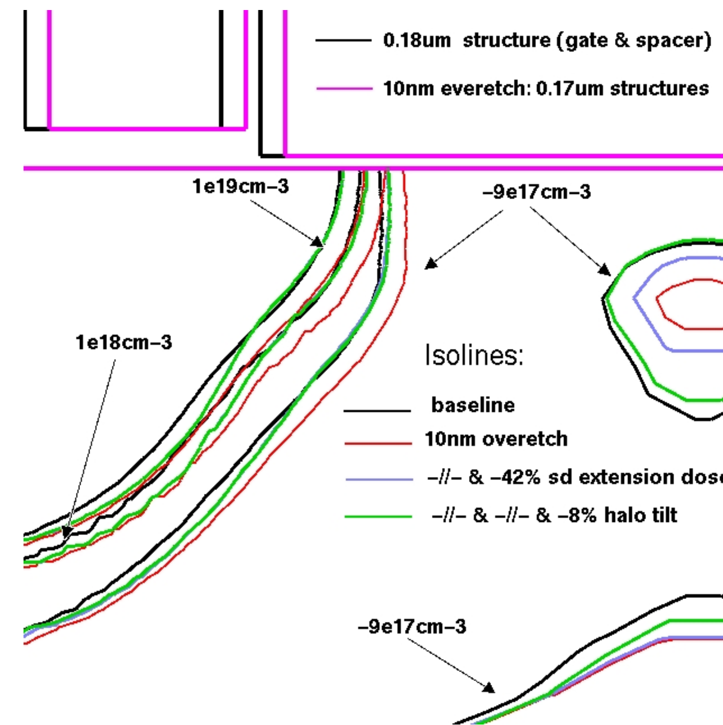
- Even small temperature variations have a strong influence on the electrical characteristics of the device.
- The effect is larger in short-channel devices.

© 2005 Synopsys, Inc. (17) CONFIDENTIAL – DO NOT DISTRIBUTE

CD Compensation

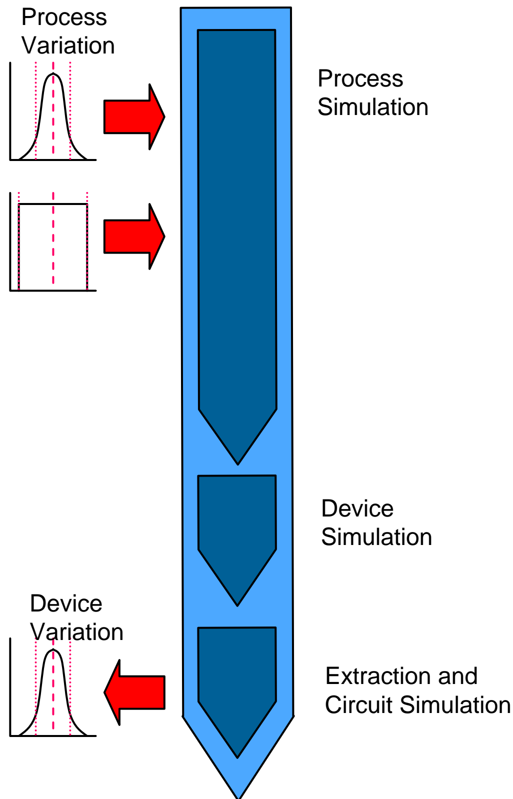
Compensation of CD variation with halo implant

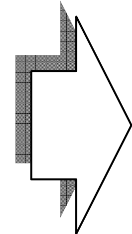
- Measurement of gate overetch
- Compensation in halo implant dose and halo tilt
- Compensation models derived from TCAD
- Changing Halo dose and angle brings Idsat closer to spec, but ΔVt increases



SYNOPSYS®

Process Compact Models





From the process model derived by TCAD an efficient *Process Compact Model* (PCM) is derived for further use

- Based on response surface modeling methodology
- Robust, fast, and embeddable into other environments
- Conceptually analogous to device compact models

Input parameters (e.g.)

- Gate length
- Oxide thickness
- Gate taper angle
- Halo implant dose
- ...

$r_i = f(f_i)$

Output parameters (e.g.)

- VTL
- VTS
- Ion
- Ioff
- Spice parameters
- ...

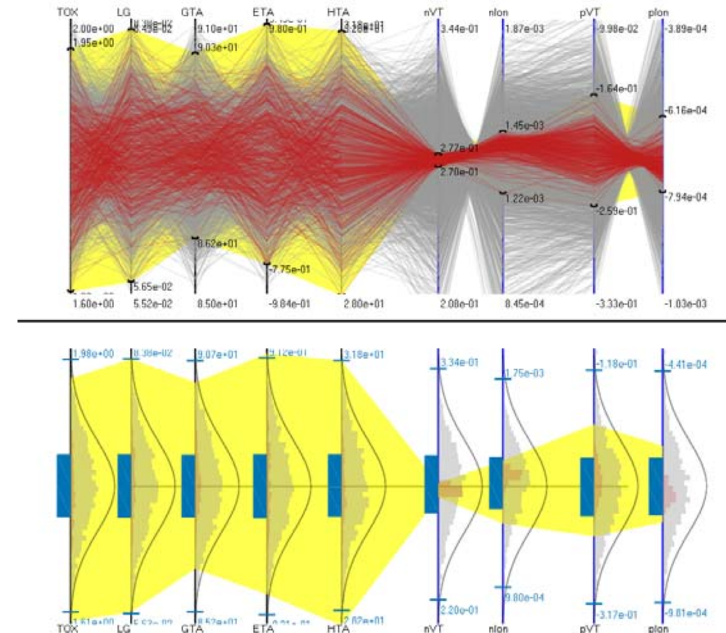
TCAD Process Model: o(1hr)

Process Compact Model: o(1ms)

© 2005 Synopsys, Inc. (19) CONFIDENTIAL – DO NOT DISTRIBUTE

Process-Device-Circuit Interactions

- PCMs can be used to explore process-device-circuit relations, for measureable/measured quantities as well as for non-measureable/non-measured ones
- Measured and assumed distributions can be combined
- PCM evaluation is extremely fast: o(ms)



Parallel coordinate plot, with the five process parameters TOX, LG, GTA, ETA and HTA as the vertical axes on the left side, and the predicted values VT and ION for the nMOS and pMOS devices, respectively, on the right side side.

Each horizontal polygonal line represents one sample. Red are samples meeting range (yellow) criteria for all factors and responses, blue lines violate them for at least one parameter. Bottom: Identical plot, showing statistical distributions (frequency). The graphs are from Synopsys PCM Explorer.

TCAD-based Statistical CAD Models

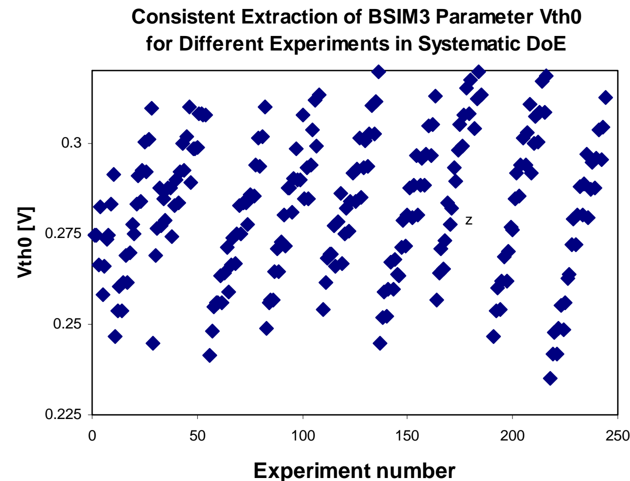
Gate length

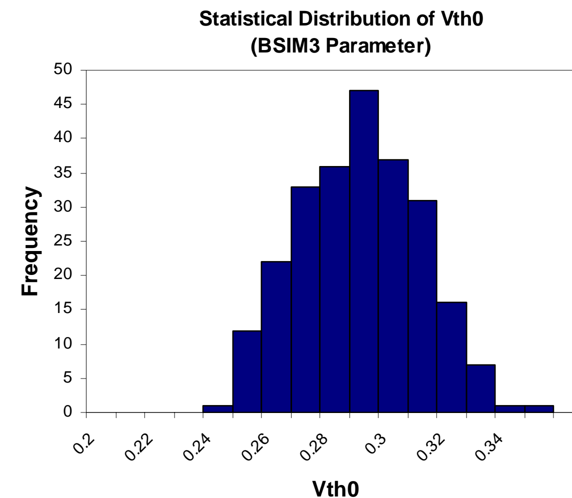
Gate oxide thickness

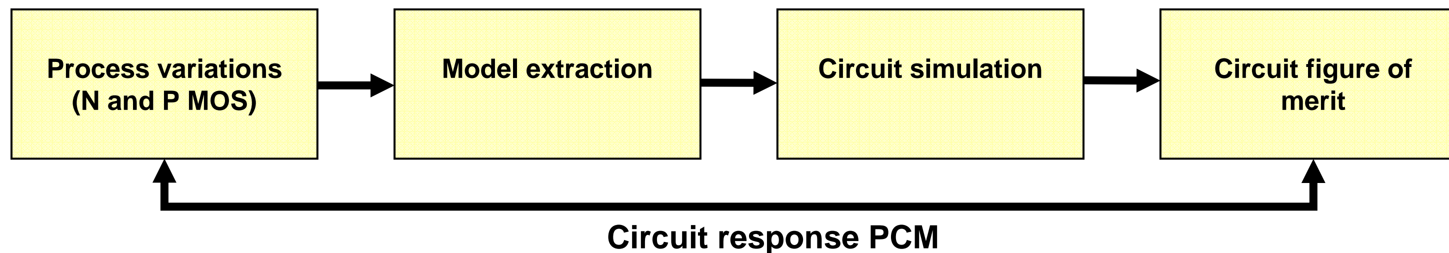
Halo I/I dose, (N, P)

Extension I/I dose

….



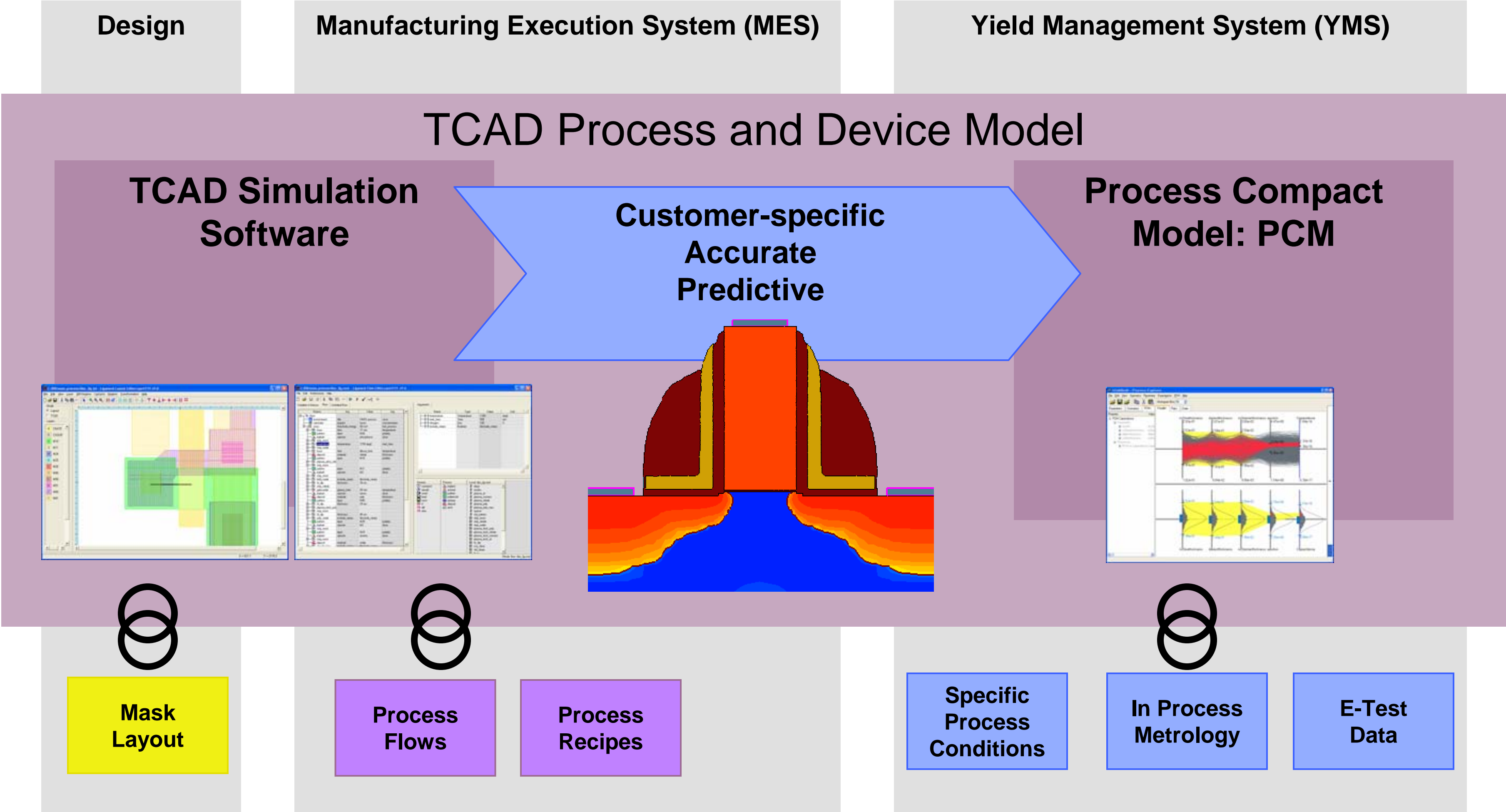




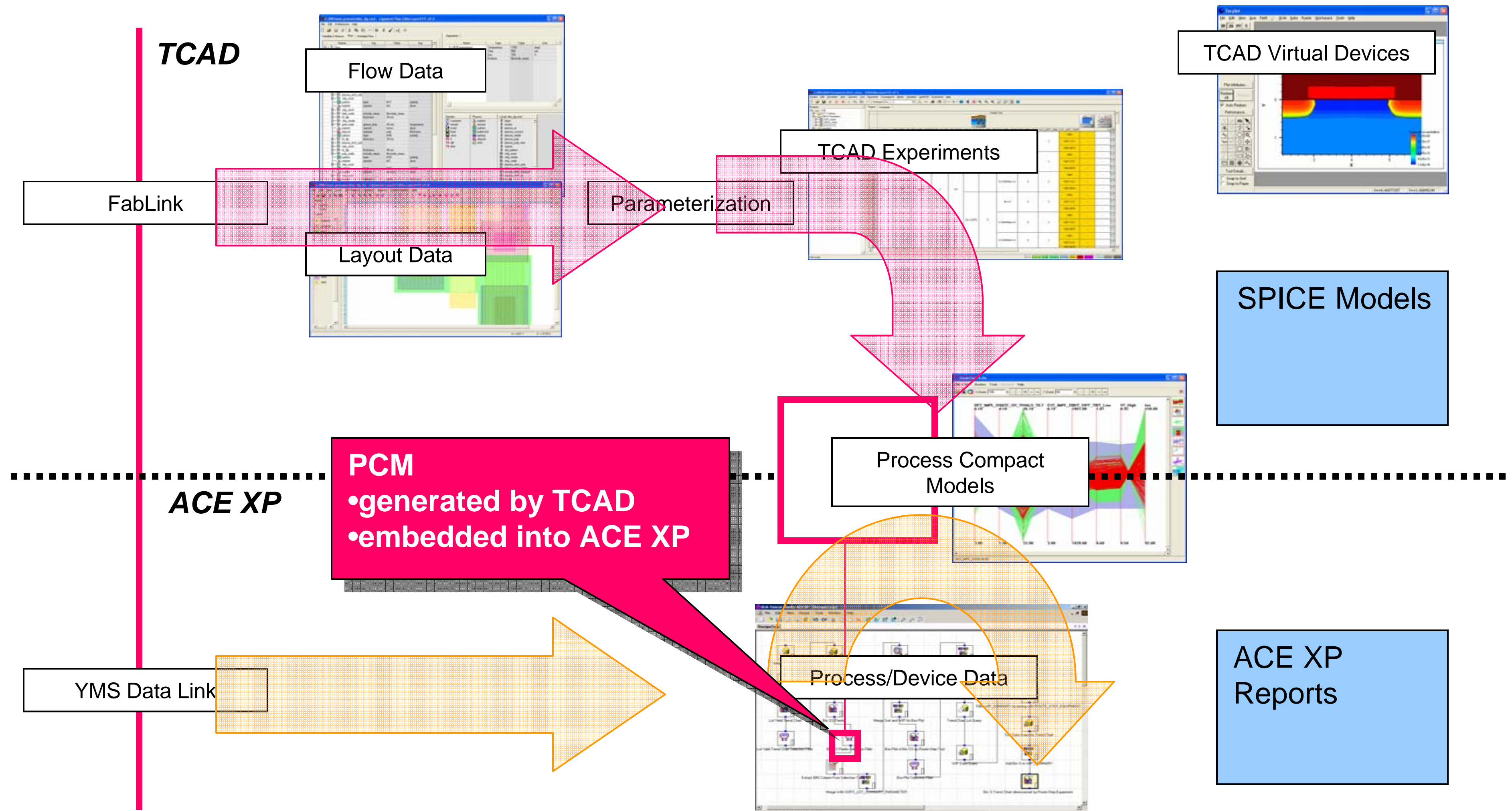
- Direct coupling of manufacturing and design with consistent model extraction
- No inaccuracy introduced in model reconstruction
- Statistical analysis of circuit and model through RSM and NN
- Recalibration of TCAD CAD models ensures high accuracy and compatibility

© 2005 Synopsys, Inc. (21) CONFIDENTIAL – DO NOT DISTRIBUTE

Synopsys FabLink TCAD



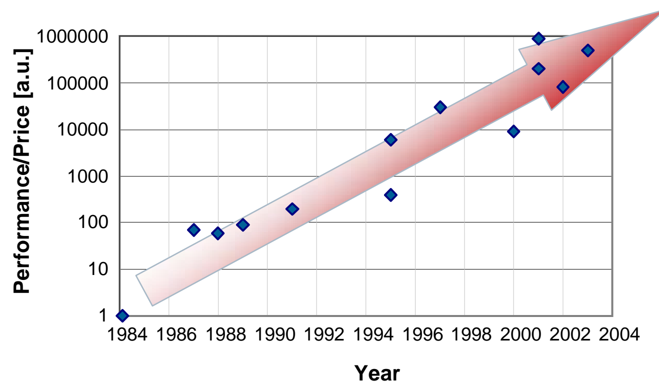
Embedding of Process Compact Models into KLA Tencor's YMS ACE XP



Computational Effort for PCM

	NMOS	NMOS	PMOS	PMOS
Model	# Sim	Est. CPU hrs	# Sim	Est. CPU hrs
PCM1 2nd order	243	240	243	480
PCM1 mixed order	324	325	324	650
PCM1 3rd order	1024	1000	--	--
PCM1 Random	100	100	100	200

Computational effort for different process compact models, using full-factorial design of experiments



Development of price-performance ratio for computing hardware over time

- Linux-based cluster computer for use by Calibration & Services.
- 62 Intel Xeon processors (21 nodes, one master), 2.4 GHz, 4 GB RAM per node.
- They are easily extendable by plugging additional nodes into the rack.
- Operates under Red Hat Linux.

Outline

- What is TCAD?
- The view of industry - yield issues in deep submicron manufacturing
- TCAD for Manufacturing - the bridge from processing to design
- **What is design for manufacturability?**
- TCAD-assisted DFM flow

SYNOPSYS®

Two Views of DFM

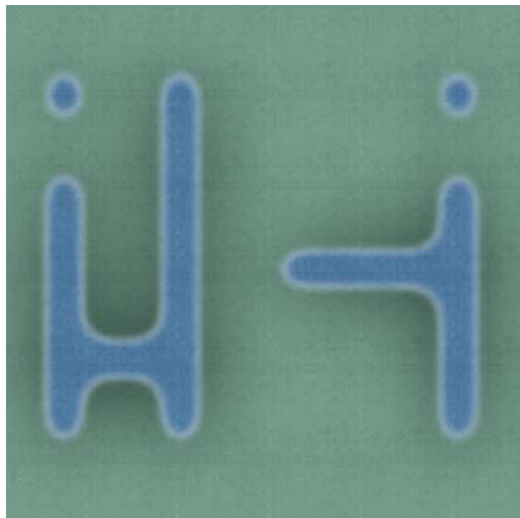
- Present: Lithography-centric DfM (OPC, PSM,….)
  - The mask correction paradigm:
  - ➲ My finally printed and processed feature should be as close as possible to my original design
  - The resolution of hotspots requires design changes
- What industry needs: Yield-centric DfM
  - The yield improvement paradigm:
  - ➲ We have to go beyond lithography and design changes and I must include process variations in the design process
  - Aspects of processing are tightly linked with design

SYNOPSYS®

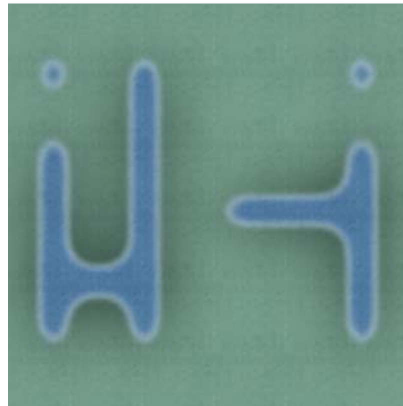
No Image = No Yield

Layout

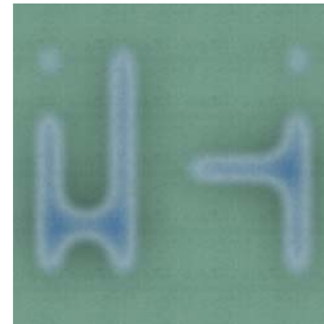
0.25µ



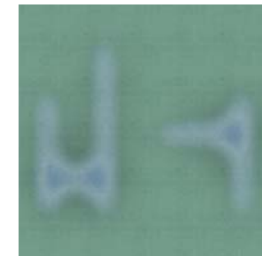
0.18µ



0.13µ



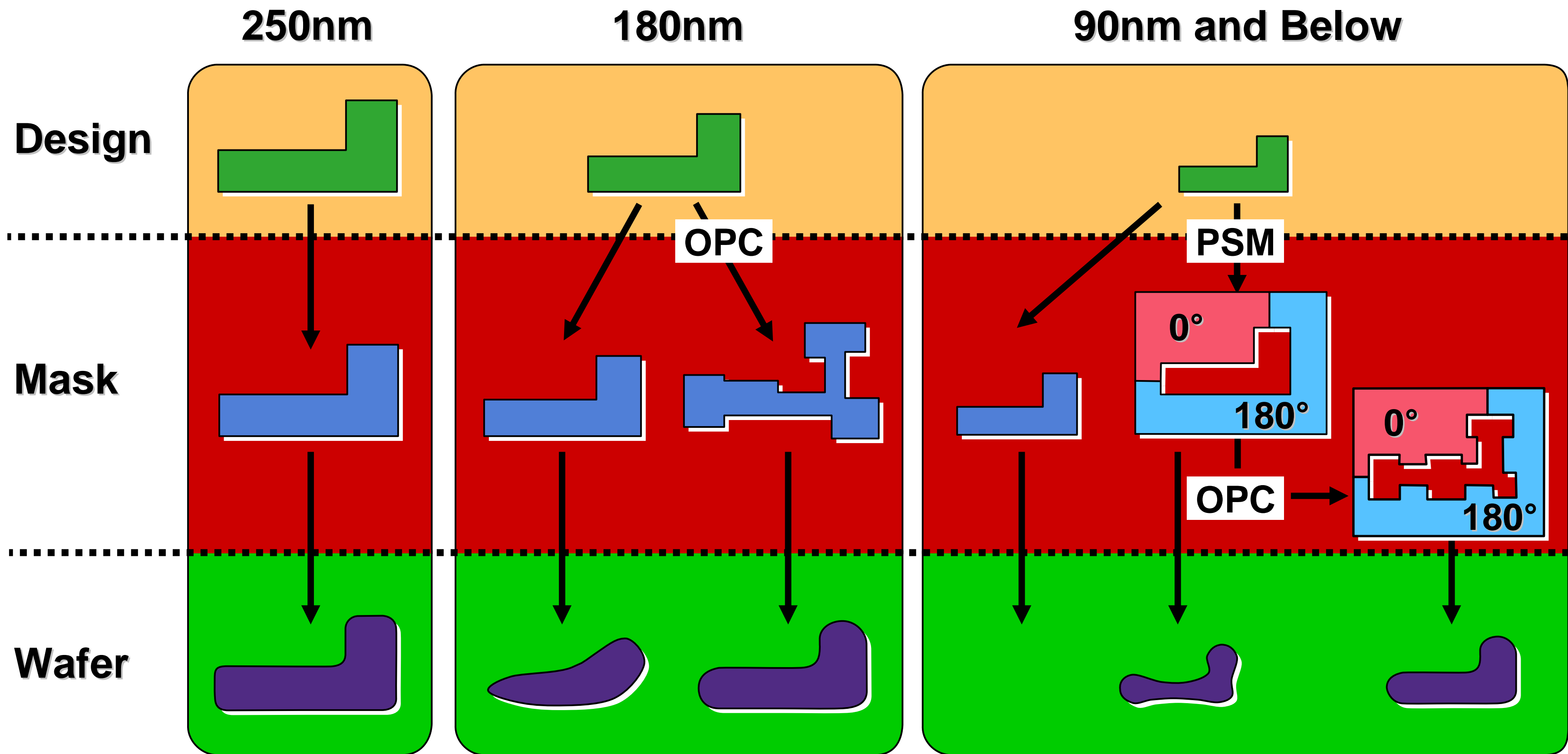
90nm



65nm

© 2005 Synopsys, Inc. (27) CONFIDENTIAL – DO NOT DISTRIBUTE

Lithography: Printability Issues



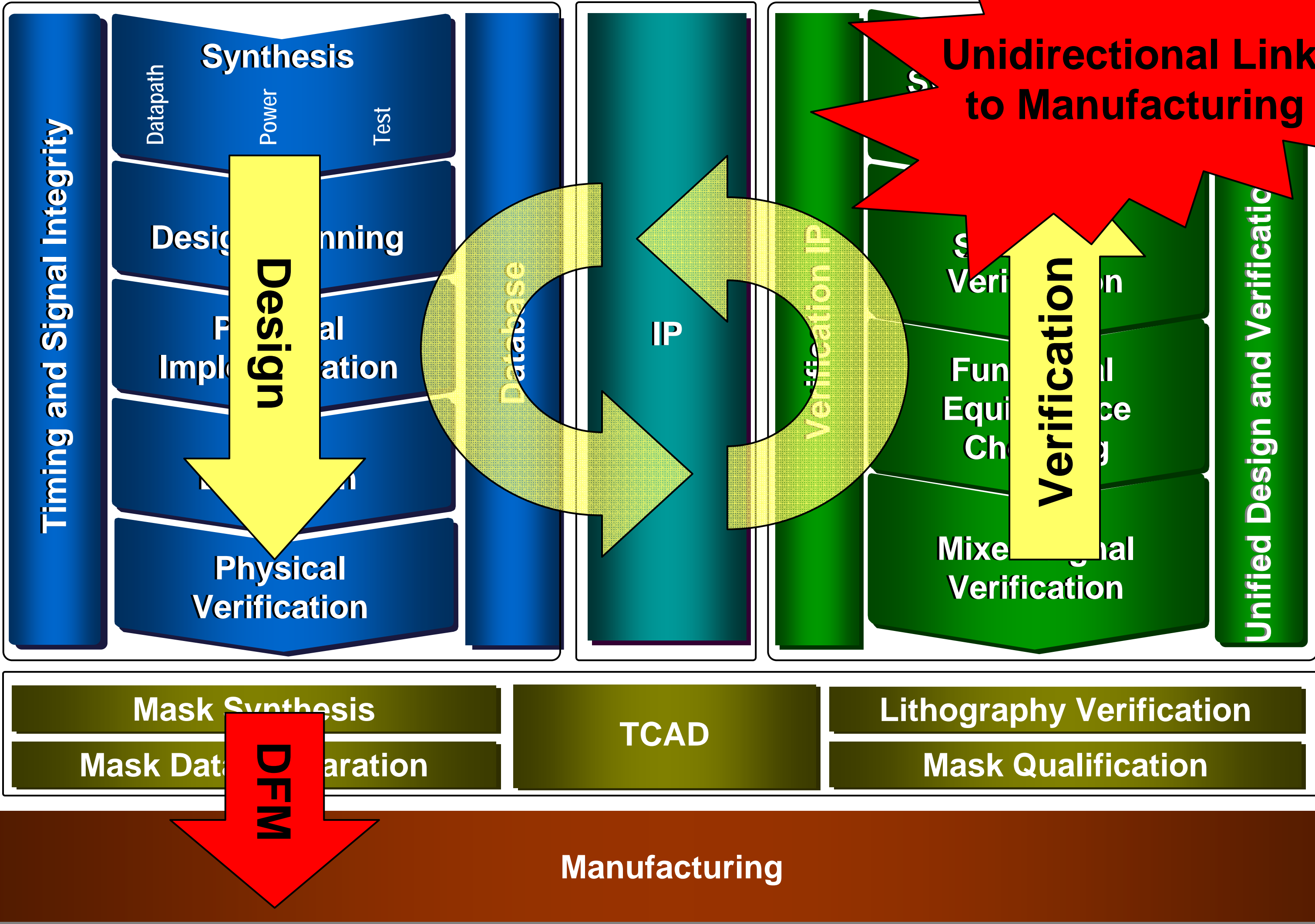
Wavelength: 248nm

RET: Resolution Enhancement Techniques
OPC: Optical Proximity Correction
PSM: Phase Shift Mask

What you draw is not what you get!

© 2005 Synopsys, Inc. (28) CONFIDENTIAL – DO NOT DISTRIBUTE

DFM: Litho-centric Flow View



Two Views of DFM

- Present: Lithography-centric DfM (OPC, PSM,….)
  - The mask correction paradigm:
  - ➲ My finally printed and processed feature should be as close as possible to my original design
  - The resolution of hotspots requires design changes
- What industry needs: Yield-centric DfM
  - The yield improvement paradigm:
  - ➲ We have to go beyond lithography and design changes and I must include process variations in the design process
  - Aspects of processing are tightly linked with design

The Need for Yield-Centric DFM

- For sub-130nm technologies, device and circuit performance, and ultimately yield, depend critically on process variations
- The current design paradigm and modern EDA tools do not capture these variations
- There is no link to in-process metrology to allow fast feed-forward correction
- Extend DFM beyond lithography to include full process flow and variations
- Build bridge head in manufacturing with TCAD for Manufacturing
- **Bidirectional Link**: Manufacturing for Design: MFD
  - Adapt process to design
  - Bring manufacturing data back to design

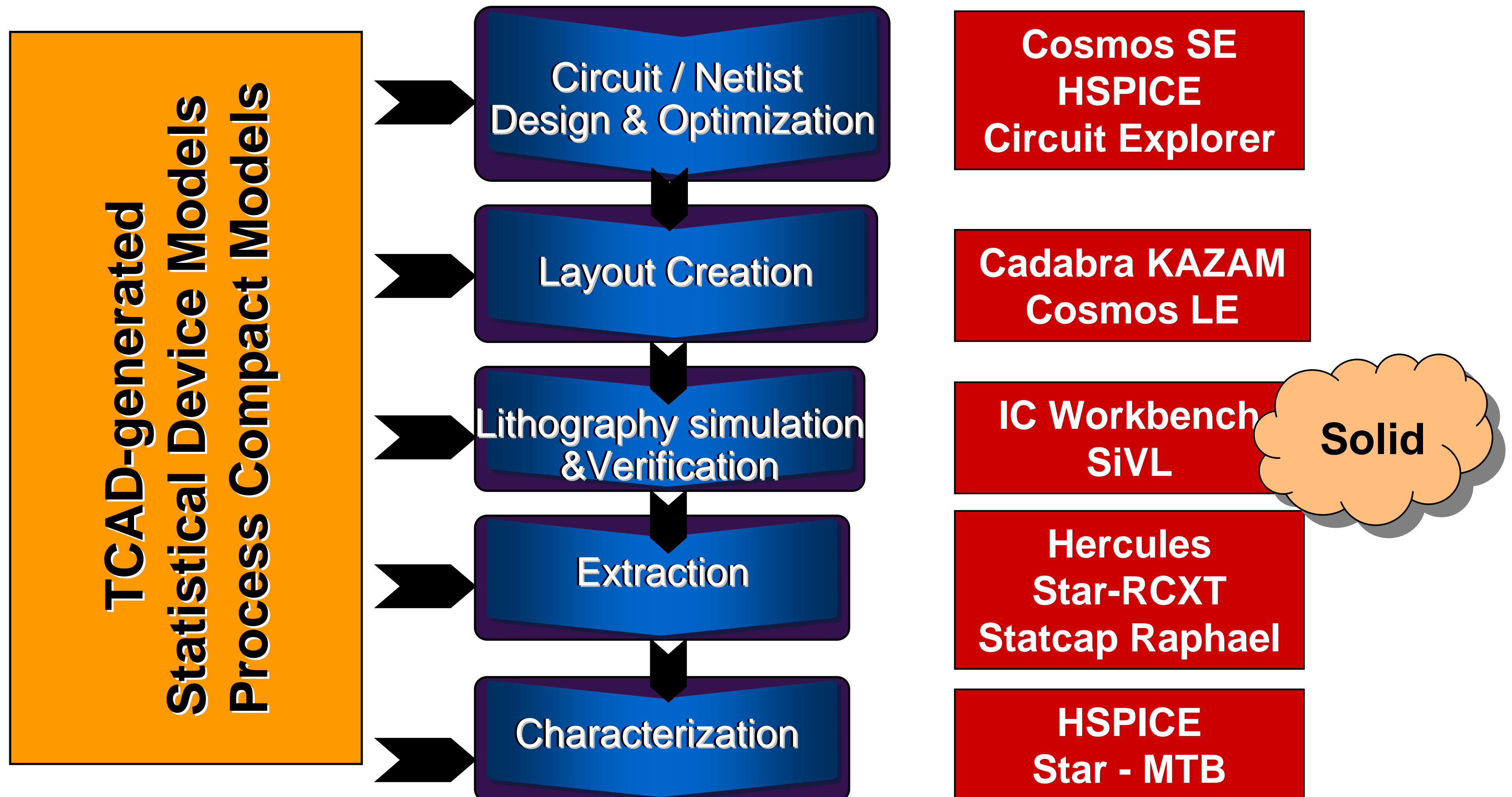
Role of TCAD in DFM

- Develop methods that use simple but accurate models to help design complex chips with millions of components
- Abstract the silicon behavior into models (PCM) that can be utilized by tools during design and manufacturing
- Detailed analysis of different physical phenomena that affect circuit components at the device, interconnect, and the small circuit/cell level

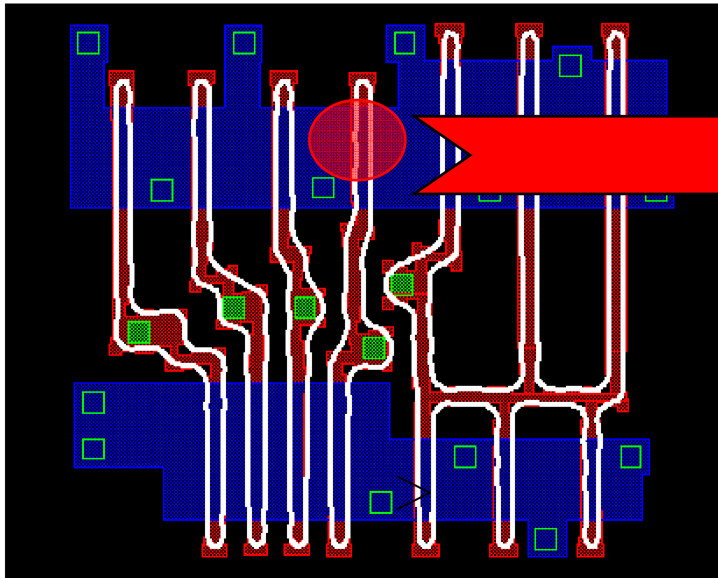
Outline

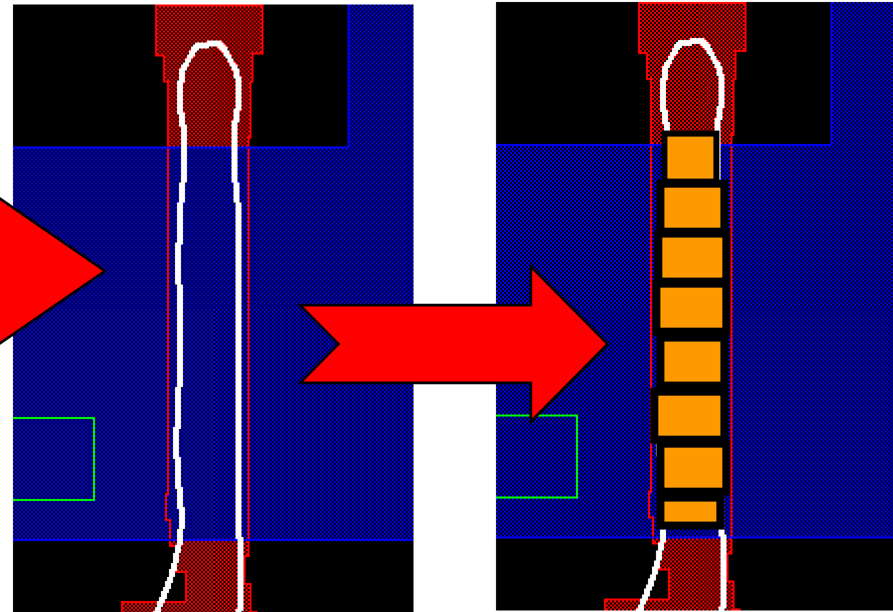
- What is TCAD?
- The view of industry - yield issues in deep submicron manufacturing
- TCAD for Manufacturing - the bridge from processing to design
- What is design for manufacturability?
- **TCAD-assisted DFM flow**

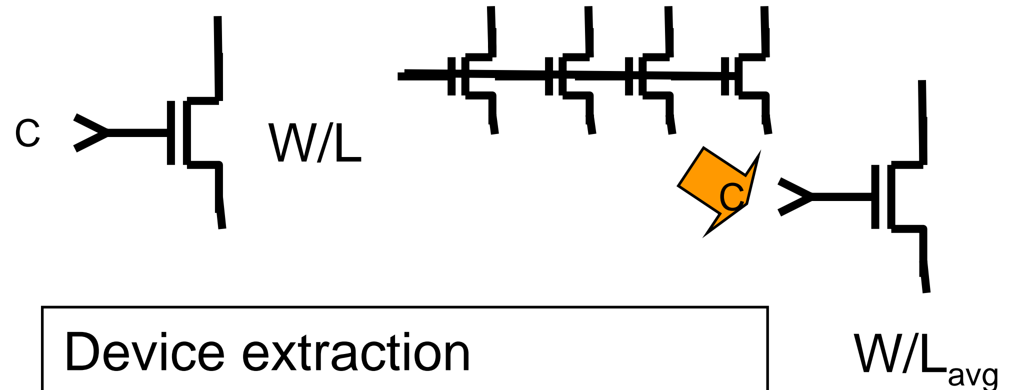
TCAD-driven Design Optimization Flow



Accurate Device Extraction from Image







Areal image of poly layers

Device extraction

W/L_{avg}

SYNOPSYS®

TCAD-based Statistical CAD Models

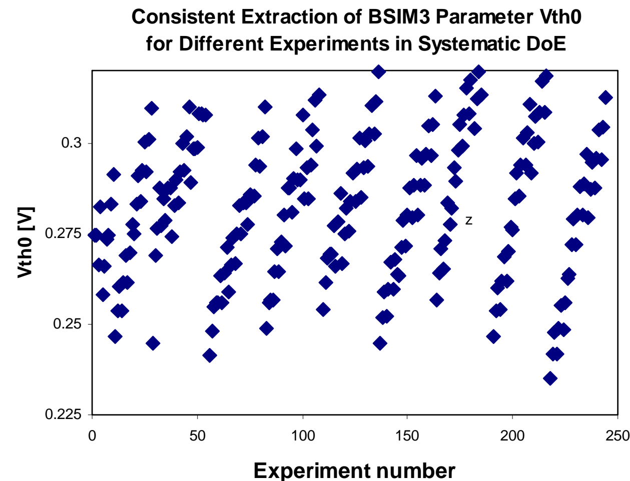
Gate length

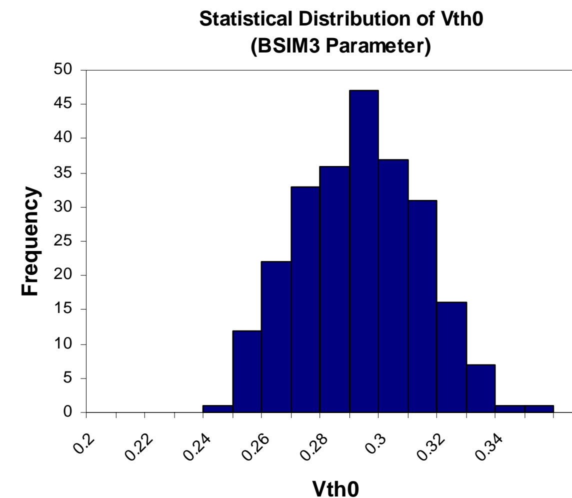
Gate oxide thickness

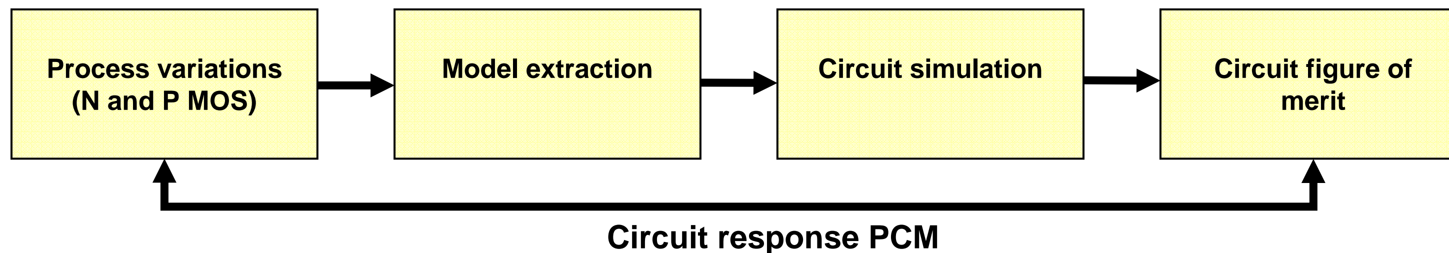
Halo I/I dose, (N, P)

Extension I/I dose

….



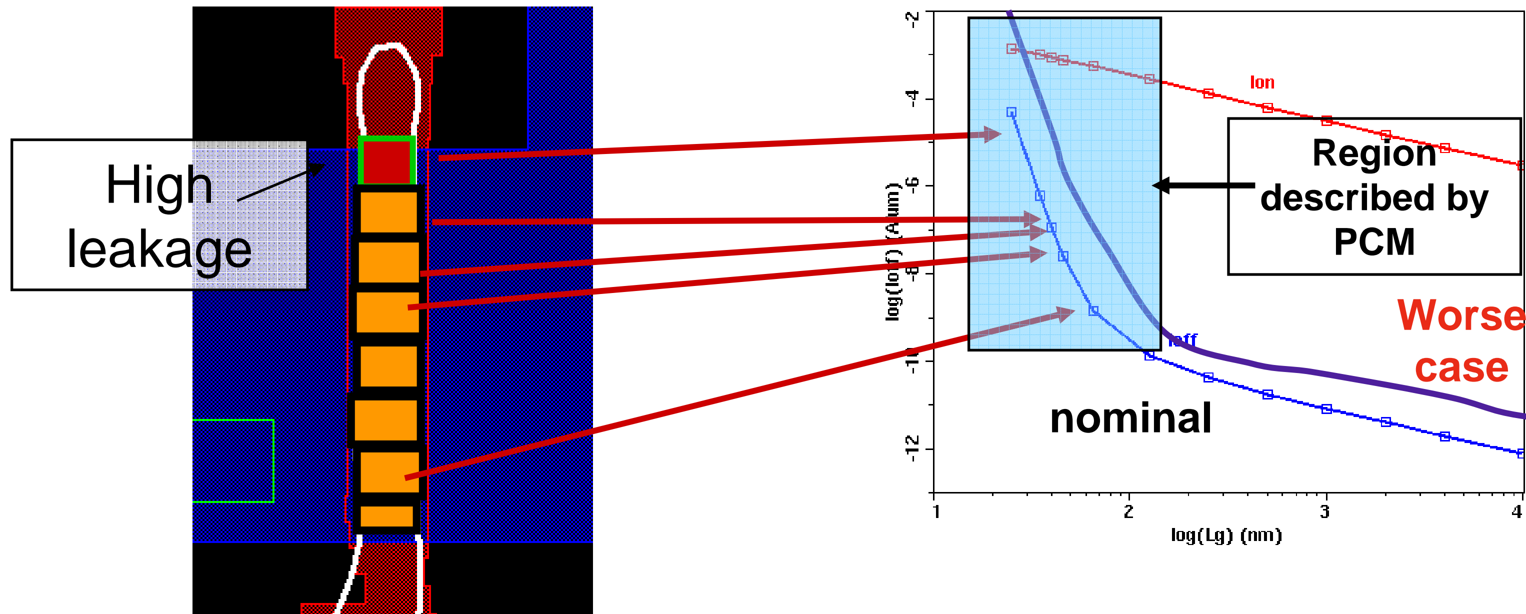




- Direct coupling of manufacturing and design with consistent model extraction
- No inaccuracy introduced in model reconstruction
- Statistical analysis of circuit and model through RSM and NN
- Recalibration of TCAD CAD models ensures high accuracy and compatibility

© 2005 Synopsys, Inc. (36) CONFIDENTIAL – DO NOT DISTRIBUTE

Identify Potential Electrical Problems



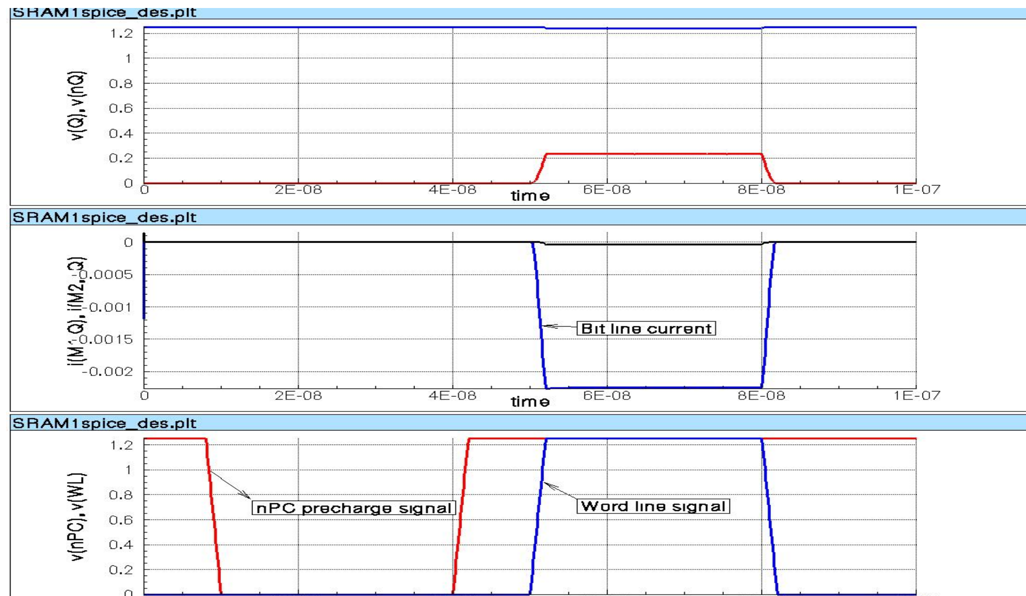
3D simulations indicate that current flow is mainly perpendicular to gate

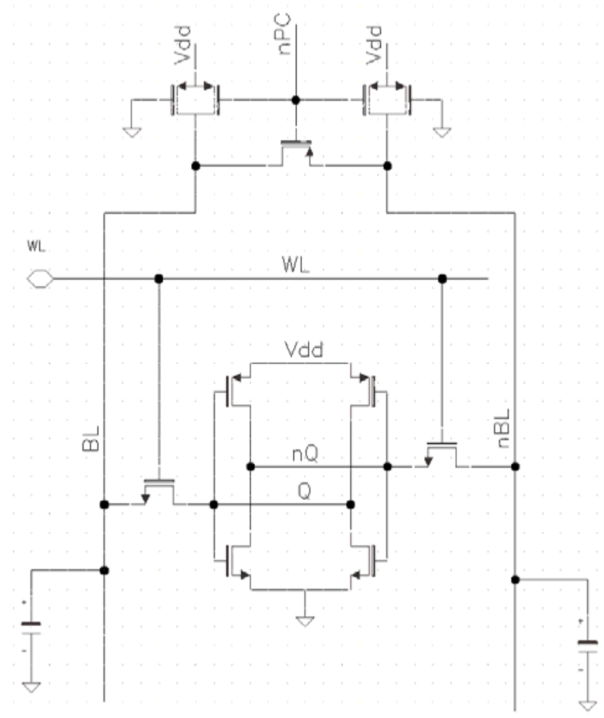
Use TCAD-generated device curves (for different process conditions) or PCMs to determine leakage and potential hot spots

© 2005 Synopsys, Inc. (37) CONFIDENTIAL – DO NOT DISTRIBUTE

Circuit-Response PCM Example: SRAM

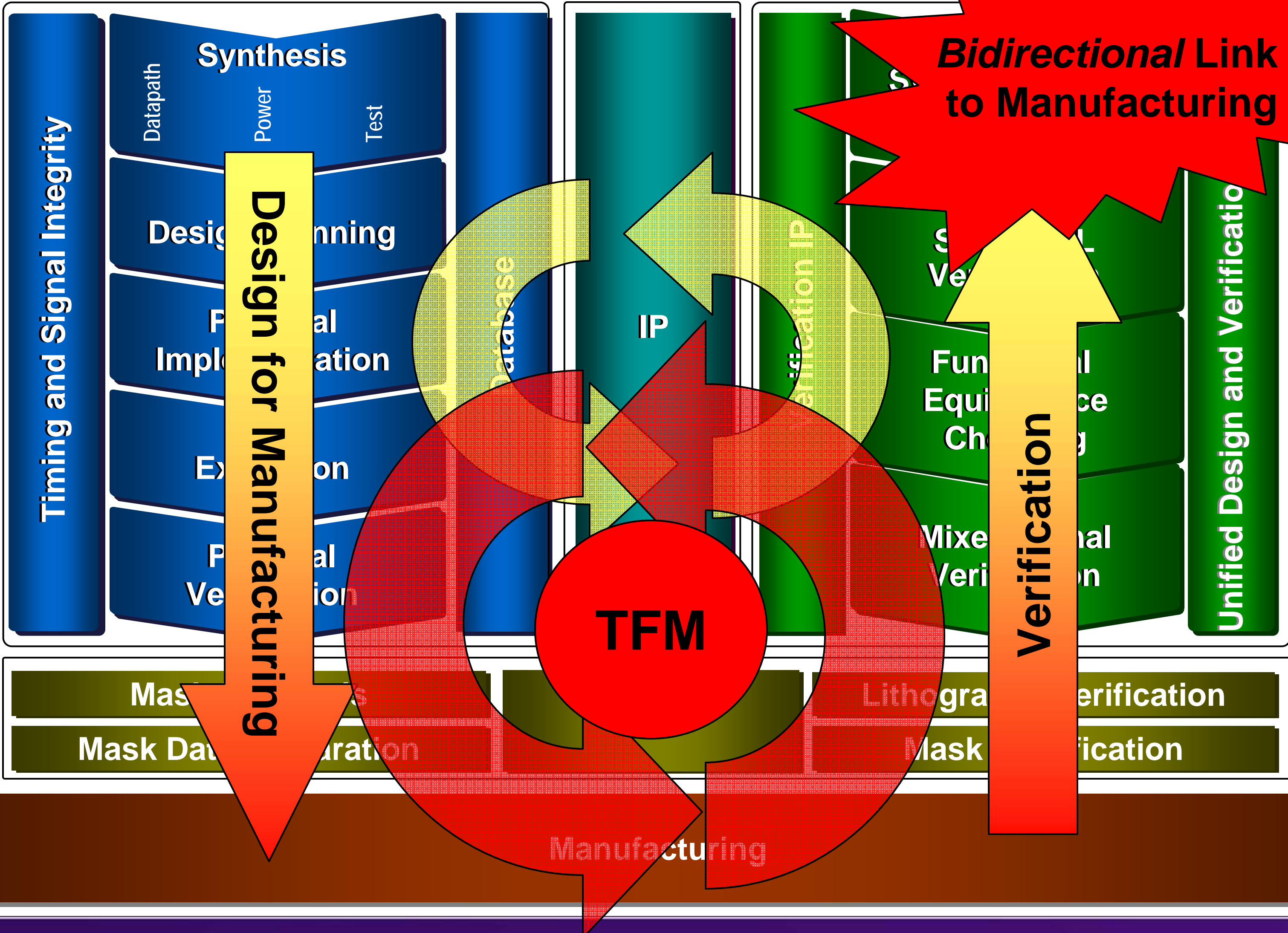
- FF DOE on 4 parameters (81 experiments), full CMOS process simulated.
- SRAM bit line current is analyzed





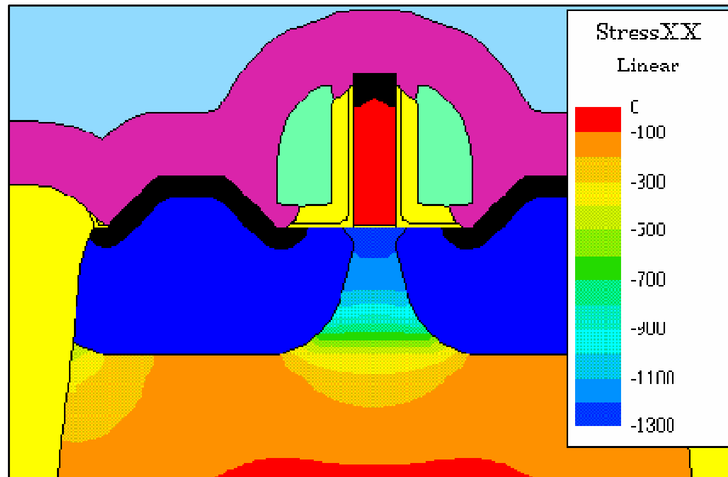
SYNOPSYS®

DFM: Yield-centric Design Flow View



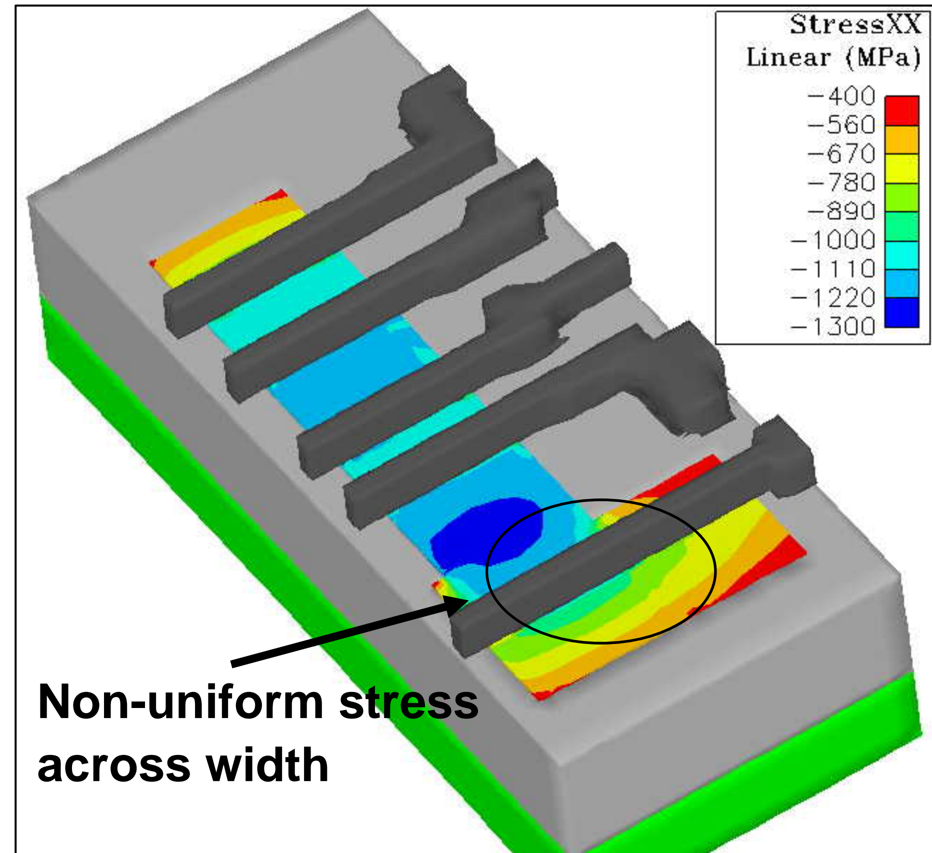
SYNOPSYS®

Layout-dependent Strain



Stresses in 2D structures from tensile STI and 20% SiGe

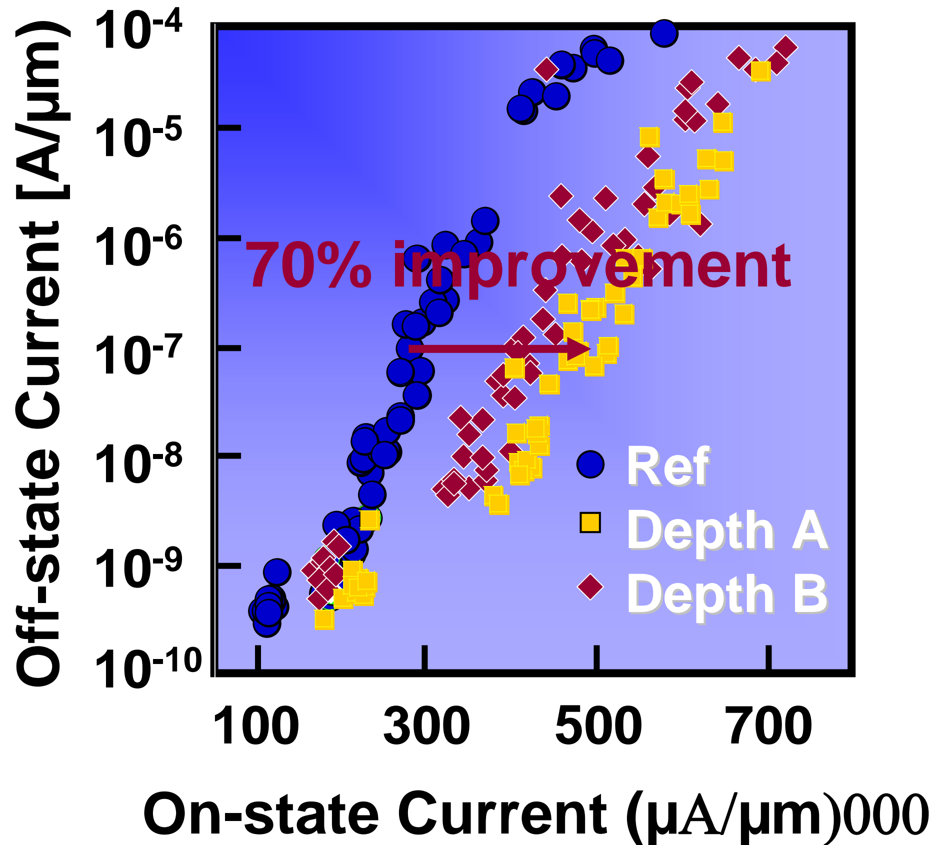
2D simulations used to optimize process parameters

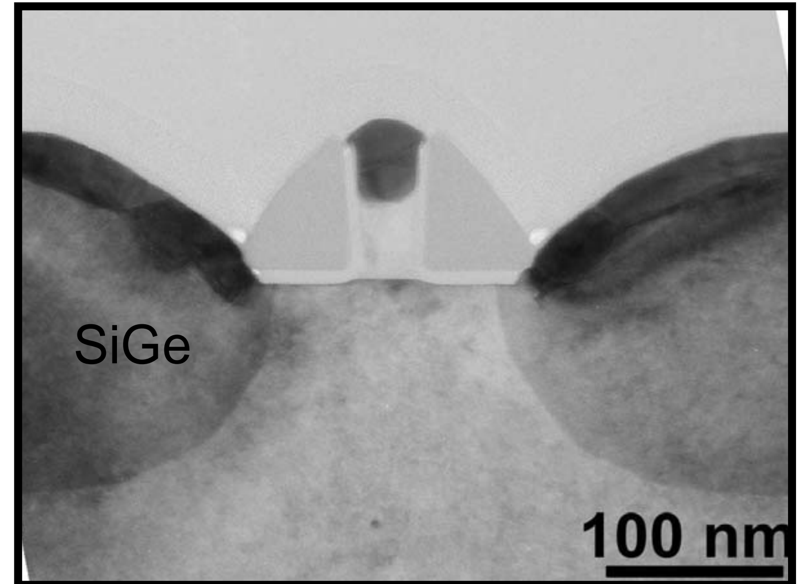


Stress contours in actual 3D layout showing lower strain near STI edges

SYNOPSYS®

SiGe Strain Engineering

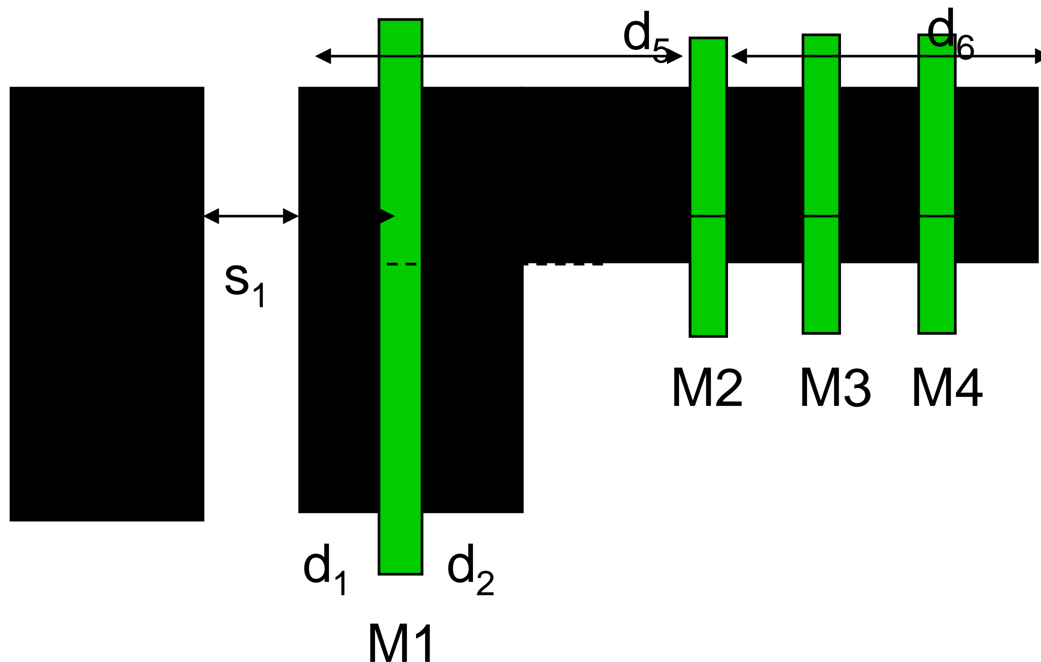




From IEDM 2004 paper co-authored by Synopsys/AMAT/IMEC

© 2005 Synopsys, Inc. CONFIDENTIAL – DO NOT DISTRIBUTE
SYNOPSYS®

Extracting Transistor Characteristics



Hercules-extracted transistors

M1 (….. w_1, $d_{1,}$ $d_{2,}$ $s_{1,,}$ w_2, $d_{4,}$ $d_{4,}$ s_1)

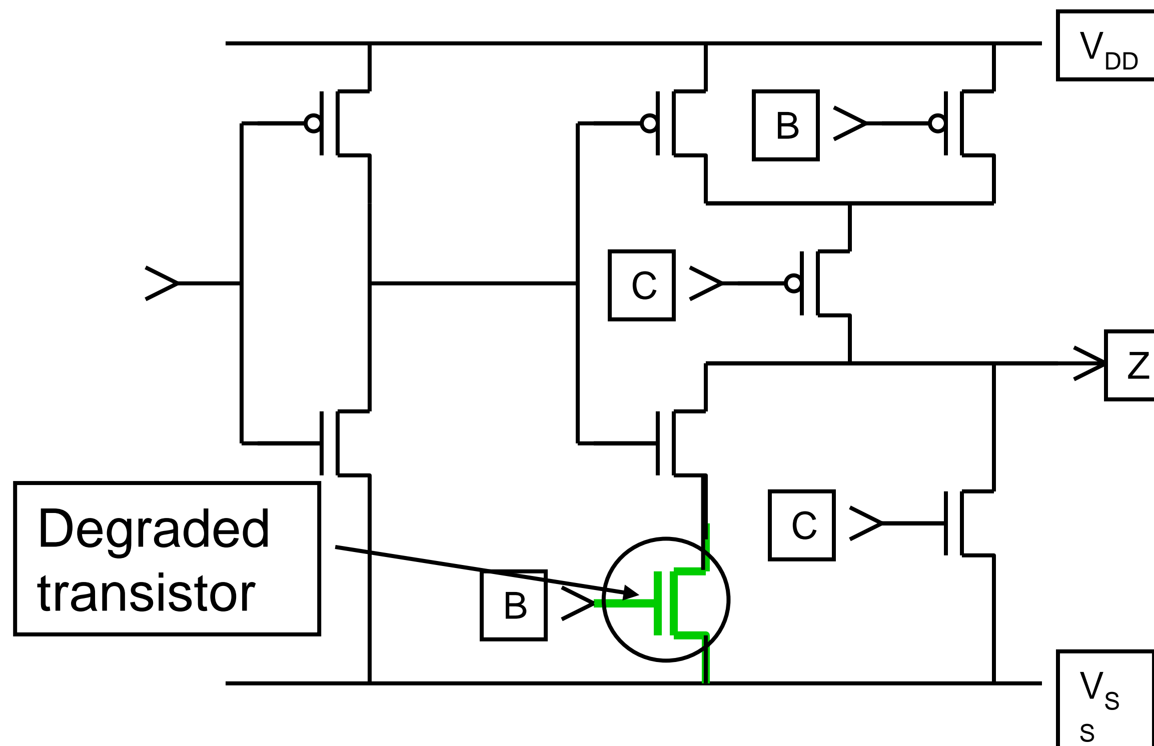
M2 (…. w_2, $d_{5,}$ $d_{6,}$ s_1,)

- Based on extensive TCAD simulations we can determine how to estimate stress from the measured layout parameters
- Modify appropriate SPICE parameters to give correct device characteristics

© 2005 Synopsys, Inc. (42) CONFIDENTIAL – DO NOT DISTRIBUTE

SYNOPSYS®

Impact of Device Reliability on Designs



- TCAD creates time-dependent SPICE models based on physical models
- Circuit analysis identifies critical transistors
- Circuit can be optimized to accommodate device degradation

Synergy Loops between TCAD and EDA