The Impact of Reuse Requirements on IP

Saverio Fazzari

Cadence Design Systems

Agenda

cadence®

- What is reuse?

- Reuse requirements and risks

- A view of reuse strategies and risk mitigation

- Examples: QIP and OpenChoice

- Other work

- Summary

Modern Design Requirements

- Marketplace demands

    – More functions: Area and speed requirements

    – Sooner: Meet the market window

- New technologies needed to achieve goals.

    – Costs are much higher

   – New sets of problems at smaller geometries.

    – Integration issues
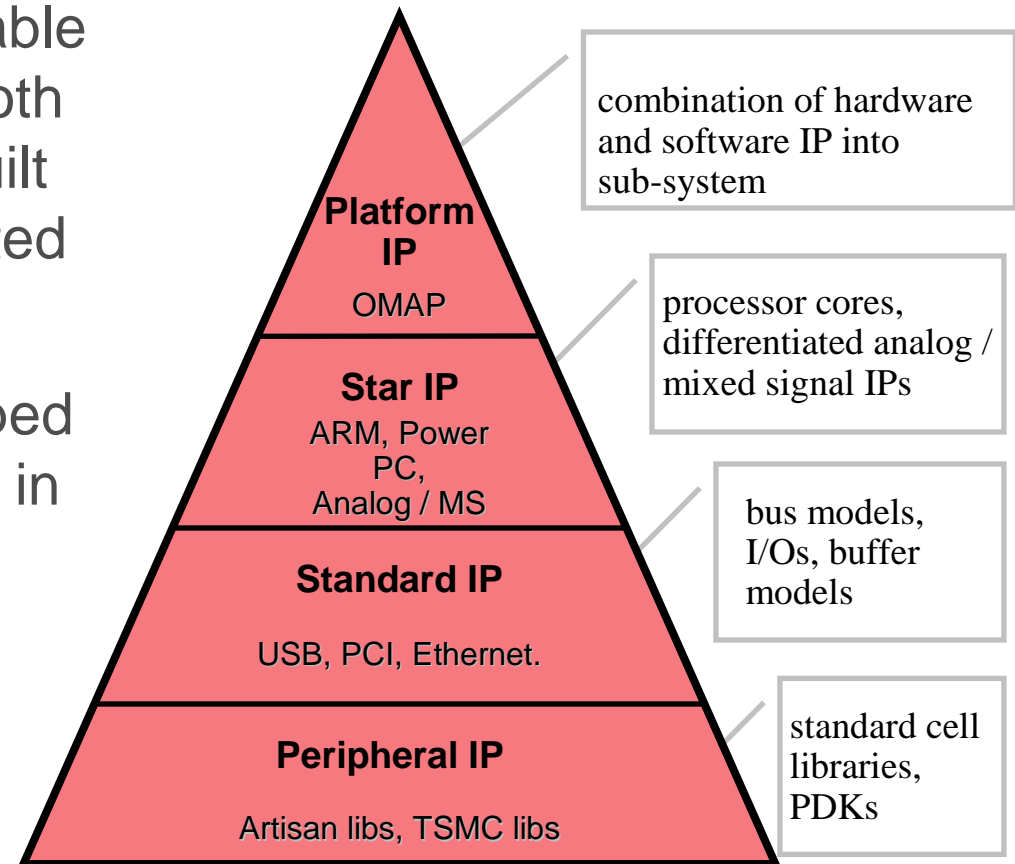
Next Generation SoC Development

- Increased design complexity

- Use of pre-designed IP can reduce design time and verification

- Potential risk with usage of IP

  – Does not integrate into the system

  – Does not function correctly

  – Does not work with existing environments.

- This can be true for IP available both internally or externally
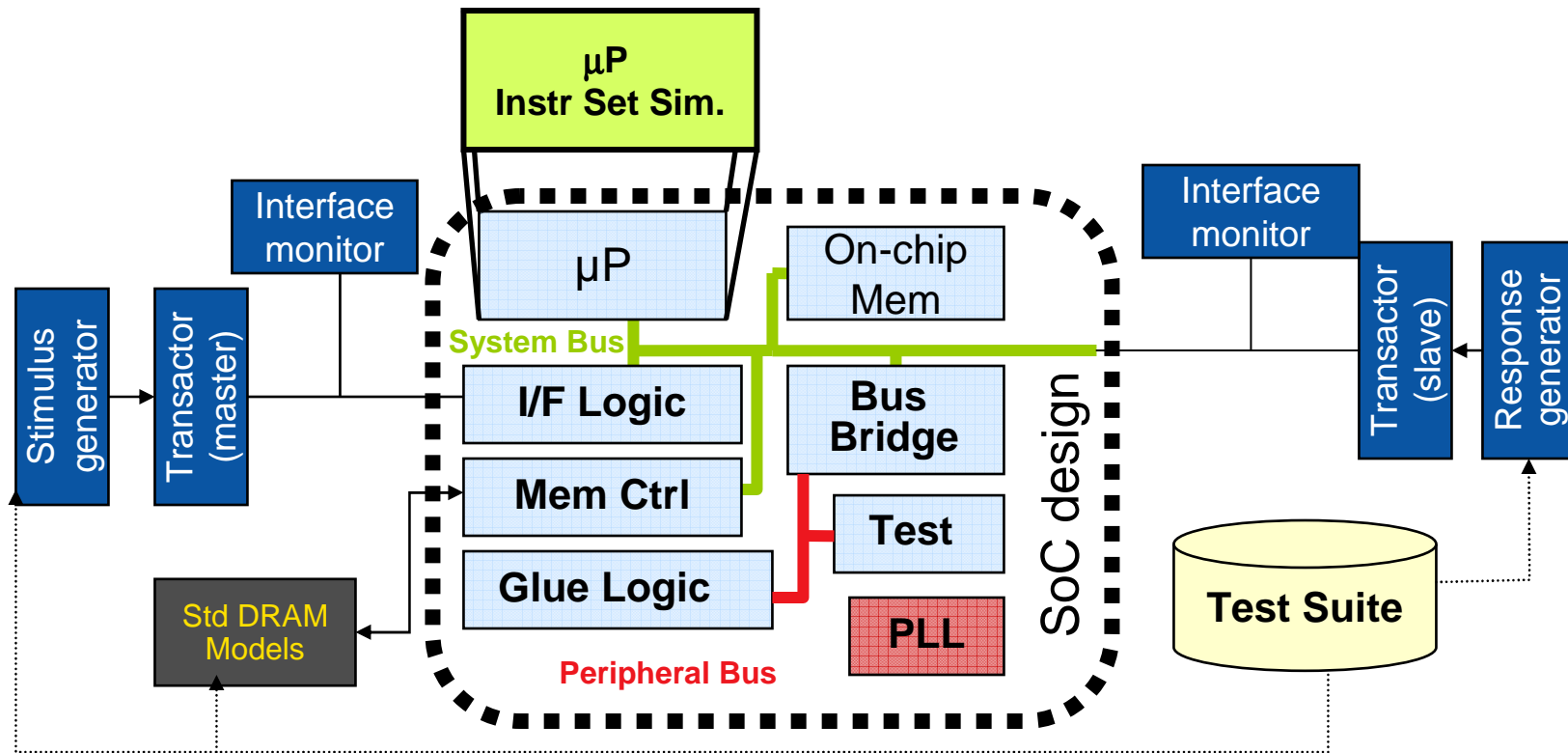

4
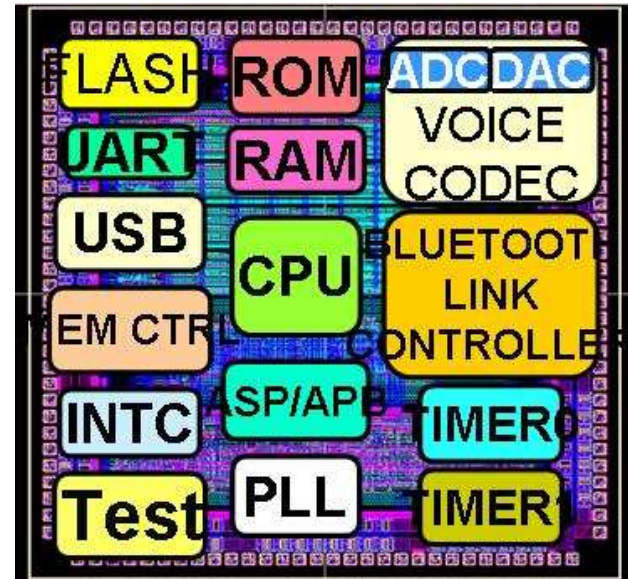
IP and Reuse

- **IP:** Pre-existing functional blocks that can exist as downloadable software, hard macros or both (semico, 03/03), and pre-built verification models associated with such blocks.

- **Reuse**: Using code developed for one <u>application program</u> in another application.

  – <u>Source</u>: *The Free On-line Dictionary of Computing, © 1993-2004 Denis Howe*

Platform IP

OMAP

Star IP

ARM, Power PC,
Analog / MS

Standard IP

USB, PCI, Ethernet.

Peripheral IP

Artisan libs, TSMC libs

combination of hardware and software IP into sub-system

processor cores, differentiated analog / mixed signal IPs

bus models, I/Os, buffer models

standard cell libraries, PDKs

IP in a Typical SoC Design Environment

```
ERROR: stackunderflow
OFFENDING COMMAND: ~

STACK:
```