Beyond P-Cell and Gate-Level Assumptions: Accuracy Requirements for Nanometer Design Simulation

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ABSTRACT

The forward march of Moore's Law has resulted in integrated circuit (IC) designs containing more and more functionality on a single chip. While nanometer technology enables expanded capability, such as analog-mixed signal systems-on-chip (AMS SoC), it brings with it a new set of design closure problems. Complex designs demand more power and higher clock frequencies; they also create more signal and power net electromigration and substrate noise. The stress effect of a single analog device with unique diffusion measurements can cause an entire chip to fail. This is a huge problem for designers; half of all AMS designs fail first silicon. [1] With mask costs reaching $1 million each, designers can no longer afford to rely on parameterized cell or gate-level parasitic extraction assumptions for analysis and simulation. Nanometer-era designs require accurate and comprehensive data to enable accurate modeling.

General Terms

Design, Verification, Modeling

Keywords

Intentional devices, parasitic devices, physical parameters, parasitic extraction, comprehensive analysis, nanometer silicon modeling

1. INTRODUCTION

Device extraction and parasitic extraction have always been issues at some level. Analog designs, which are handcrafted, are more prone to signal flaws than digital designs, which are most often created by an automated design process. At larger process technologies, such as 250nm, device extraction could be handled with an LVS tool using an assumptive method of measuring physical parameters. Parasitic extraction could be handled by using tools employing simple cell characterization at the gate level. But with the advanced functionality, complex mixed signal design and restricted chip real estate of 130nm process technology, assumptive measurement and gate level extraction were no longer enough to gain accurate mixed-level simulation or to solve the ever-increasing amounts of parasitic problems that can cause chip failure. Actual measurements of the device parameters are now required for accurate simulation and analysis models for noise, timing, power and integrity. And designers must now go deep inside the "black box" of gate-level assumption in order to mine the transistor -level detail required for multi-level analysis and simulation.

2. LAYOUT CONSTRAINTS REDUCE ASSUMPTIONS

There's a good reason that analog designers are often referred to as "analog artists." Analog devices are handcrafted, and although there are design standards to be drawn from, the finished product often displays artistic license. With the shrinking geometries of advanced process technologies, and the proliferation of systems-on-chip containing multiple millions of transistors, handcrafted analog devices and other elements that don't fit the standard mold can produce unintentional effects that can greatly affect the chip as a whole.

With 130nm process technology in production, 90nm underway and 65nm on the near horizon, chip designers are faced with less and less "wiggle room" for custom or handcrafted elements. This comes at a time when non-standard devices have a greater and greater impact on the full chip's power and electrical behavior. Yet, most device extraction tools (LVS) ignore the nuances of unique elements.

The key to managing unintentional effects is to employ an LVS tool that recognizes all parameters of all devices, including non-standard devices. This is the only way to be confident that simulations will match the intention of the chip is to measure parameters based on actual physical geometries. Unfortunately, most LVS tools do not handle device parameters in this way. Instead, they are programmed to make assumptions about parameters and spacing; they rely on parameterized cell (P-cell) assumptions.

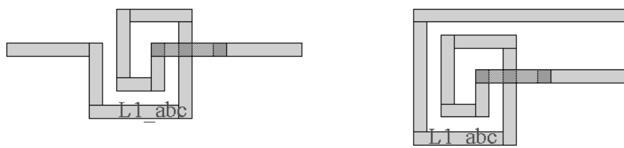
For instance, when extracting an intentional device, an LVS tool will look for an element in the layout, with text labeled "XYZ" for example, that matches that device with those in the schematic named XYZ, and assume that all will have identical parameters.

With digital designs, which are most often developed in standard repetitive format, such assumptions are acceptable; at least not as critical. Also, it is often much easier for the LVS tool to extract simple physical parameters such as length and width of transistors.

It's a different story with unique analog or other non-standard devices. A device labeled XYZ may be flattened and/or changed by the layout designer. If device extraction is generated using a parameterized cell flow, the flattened and changed device will still compare correctly with an XYZ device in the schematic; yet its parameters may differ greatly from what is in the

schematic and from what was used in simulation. If the individual parameters are not physically measured for simulation, the chip may not perform as expected. When a device is modified in the layout, the impact on chip behavior can be substantial. Common situations illustrate the problem: unique inductors, unique diffusion and non-standard transistor layout.

An inductor in the layout identified in a naming convention will be assumed to have parameters that match those in the schematic. But if the designer has added coils, or turns, to that inductor in the layout, it will not only change the device parameters, but will also affect the performance on the chip. (Fig. 1) If the change is made without also modifying the parameterized cells, simulation will not be accurate. Manufacturing a chip with inaccurate simulations will more than likely result in costly re-spins. According to recent statistics, [2] an average of 2.6 spins are required to achieve a working analog mixed signal design in silicon.



Original Pcell
Read parameter method
```
If text = L1_abc
Then T = 1.5
```

Modified Pcell
Physical Parameter Extraction
```
T = NumCorners*90 / 360
```
(Calibre method)

Case	Open-loop	Calibre
Original	T = 1.5	T = 1.5
Modified	T = 1.5	T = 1.75

Figure 1.
In the original pcell for inductor L1_abc there are 1.5 turns. In the modified case the layout designer has flattened the pcell and added a short length of line to bring both terminals out on the same side of the inductor. This effectively adds another ¼ turn to the inductor, potentially increasing the actual inductance by up to 16%. A minor change to a crucial component can cause a significant shift in the desired performance of the design.

An LVS tool that relies on P-cell methodology for comparison will not guarantee a correct comparison of the physical layout device to the schematic. This method of device extraction and comparison is not a true verification; instead, the model parameters are being compared to themselves. The only way to determine that the physical layout is equivalent to the model is to actually extract and measure the physical parameters in the layout. These physical parameters can then be compared to the parameters in the model to ensure that what is being built is indeed what was simulated and vice versa.

The main reason that parameterized cell comparison methodology is employed is that it is extremely difficult, if not impossible, for most LVS tools to properly extract the physical parameters. However, for relevant simulation, it is important to not only know the basic parameters such as length and width of transistors and other devices, but also the more unique or difficult-to-measure parameters needed for accurate simulations.

An example of this is the diffusion area of a MOS device. Simulation of diffusion gives designers an accurate picture of power and reliability; how long the device will perform before it "stresses." Most diffusion is designed with simple straight lines, represented as a rectangle. However, designers may create irregularly shaped diffusion areas to accommodate neighboring devices in a dense layout. (Fig. 2) This is common practice; however, uniquely shaped diffusion can interfere with the free flow of current.

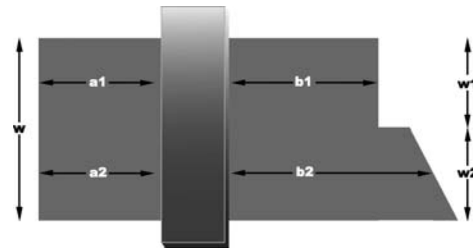


Figure 2. Irregular shaped diffusion is not accurately recognized in simulation unless exact measurement is taken of all physical parameters. Measurement of actual geometries can only be done with a LVS tool that recognizes exact physical parameters.

The only way to determine in simulation that current is being interrupted by uniquely shaped diffusion is by accurately measuring the physical parameters and feeding the data to the simulator. An LVS tool that relies on parameterized cell data to determine measurement of diffusion will wrongly assume the data for non-standard diffusion. Without extracting the physical measurement, a true verification cannot take place. Changes in diffusion occur frequently. A parameterized cell can be placed during lower-level hierarchy cell creation. Later, at a higher level of the hierarchy, a layout designer may overlap the existing diffusion with new diffusion drawn at the parent cell. (Fig. 3.) This design methodology saves space on the chip, but can also create undesirable results that will go unnoticed during simulations. These undetected changes can cause a chip to fail.

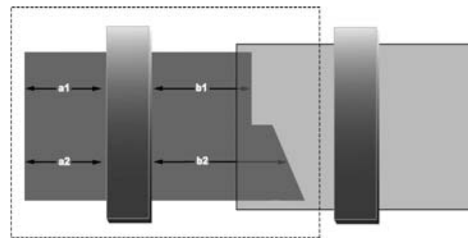


Figure 3. At a higher level of the hierarchy, a layout designer may overlap existing diffusion with new diffusion drawn at the parent cell. Left undetected, can cause chip failure.

Non-standard transistor layouts also need to be accounted for in LVS device extraction. Traditional LVS methods copy parameter information from the schematic rather than compute them directly from the layout. But if a transistor layout deviates from standard, and the deviation is not accurately measured, "from layout" device parameters are not supported, as in this example of a MOSFET (Fig. 4)

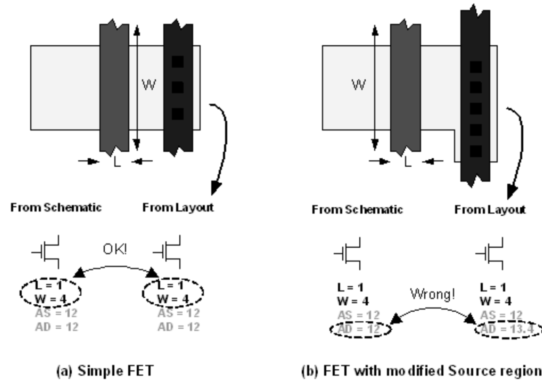


Fig. 4. Non-standard transistor layouts require an LVS tool that extracts actual device parameters. This is the only way to ensure accurate simulation.

In order to produce accurate simulation, designers require a robust LVS tool that recognizes standard naming devices, then goes deeper, measuring the device turns, wire space, core area, width, length, etc. until all physical parameter data is mined. These parameters will then be accurately compared to those in the models.

4. TRANSISTOR-LEVEL PARASITIC EXTRACTION A NECESSITY AT 130NM

In the nanometer era, a designer is faced with a host of new physical effects he must account for. In addition to coupling, a large spectrum of new capacitance and resistance interactions become relevant. Vias are now significant contributors to net parasitic capacitance, poly-contact coupling, etc. (Fig. 5) The higher operating frequencies enabled by the smaller geometries now make interconnect inductance relevant. The new copper interconnects being used to reduce parasitic resistance are harder to control dimensionally, and cause interconnect resistance variations across a die. They also require greater metal uniformity to control these variations, which means metal fill must be inserted. This too affects circuit performance.

At the 130nm process technology node, designers require comprehensive and thorough data for simulation and analysis. This means that designers need a parasitic extraction tool that provides evidence of unintentional parasitic effects at the transistor level. Only that level of detail will provide the data required for multi-level analysis, which may include: Static Timing (C or RC) for traditional timing analysis and overall net delay; Dynamic Timing (C or RCC) for propagation delay with all circuitry active; Noise (RC) for crosstalk and signal integrity issues; Power (R) for IR drop and hotspots; Reliability (R) for yield analysis and electromigration

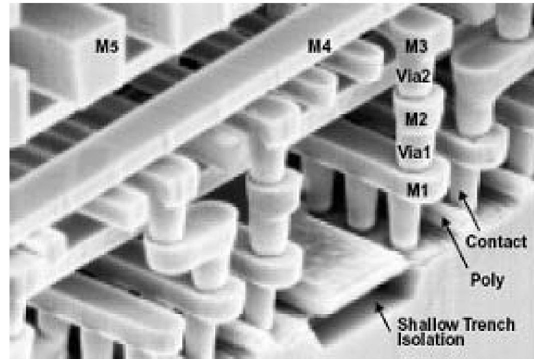


Fig. 5. Nanometer designs may include vias, conformal dielectric layers, copper wiring and non-rectangular cross-sections that need to be modeled correctly to determine interconnect effects.

SoC designers have the challenge of attempting to implement a number of different circuit element types that have a myriad of post-layout analysis requirements, ranging from transistor-level, gate-level and hierarchical simulators that require parasitic data in various formats and levels of granularity.

Traditional tool specialization forces designers dealing with analog/mixed signal components to either maintain multiple tools or use functionality that is unsuitable for a variety of design styles. Traditionally, parasitic extraction tools have been customized to handle the requirements of a specific design flow, design style and type of analysis. Typically this requires multiple parasitic extraction flows, supported by extraction tools created for different tasks.

For instance, analog designers require absolute accuracy to the transistor level. Because each analog block has unique characteristics, the parasitic extraction tool had to investigate all circuit data, including all nets in small cell, select nets on a block, and clock nets on larger designs. Although parasitic extraction is a time-consuming effort at this level, it does offer the accuracy required for analog designs. Digital designers, on the other hand, are willing to relinquish some accuracy for the sake of extraction speed and performance. They will use a tool for gate-level extraction that sacrifices some accuracy by making assumptions of cell characteristics.

Given the nature of SoCs and the various design tools used to create the components, a parasitic extraction tool must be able to easily integrate into any design flow or layout environment while still providing a comprehensive approach to extraction. That means a parasitic extraction tool that provides gate-level, transistor-level, and mixed-level analysis, plus accuracy, capacity and performance across all design styles. A single extraction tool flow would provide the best possible solution for providing accurate data of parasitic elements in AMS SoC designs. Most importantly, a single transistor-level tool will yield a consistent, confident design. It would also offer advanced data management to handle the enormous amount of parasitic elements that are extracted from current SoC designs.

5. IMPORTANCE OF A STRONG LINK: LVS AND PARASITIC EXTRACTION

Designers must be able to integrate parasitic information into their design environment, and post-layout information must be integrated as an entire circuit or subcircuit suitable for simulation. This requires accurate extraction of intentional devices, physically measured parameters and the ability to properly back-annotate devices, gates, and nets from the layout with the original design source.

To enable this, a tight integration between the LVS and parasitic extraction tools is required. Proper back-annotation for simulation in any of the multiple transistor level flows requires a connection to an LVS tool that enables multiple parasitic extraction flows. The tools need to provide accurate intentional device recognition for the variety of devices (transistor, inductor, capacitor, varactor, etc.) that will be implemented in today's AMS designs.

Tight integration among the design environment, LVS tool, parasitic extraction tool and analysis tool ensures efficient data handling for both upstream design creation environments and downstream post-layout analysis. When a hierarchical-based LVS tool is paired with a transistor-level parasitic extraction tool, it offers the designer the analysis capabilities required of an AMS SoC design: intentional device recognition (with exact device parameters); parasitic device extraction at both transistor and gate levels; highest accuracy for post-layout simulation; and backannotation of simulation results to the source schematic. These are essential to accurate nanometer silicon modeling.

6. RECOMMENDED FLOW

By streamlining the design flow with a robust tool suite that has a tightly integrated parasitic extraction and LVS tool solution at its core, designers can avoid the resource drain and technical shortcomings of a multiple tool environment. The key is to choose tools that actually measure, not merely assume. Designers should adopt a tool suite with the following attributes. [3]

- A single set of common intentional device models shared directly between LVS and parasitic extraction
- Accurate physical device parameter measurements
- Accurate parasitic extraction for both cell/block and full-chip parasitic extraction
- Design-style independence to handle the various components of AMS SoC designs
- Strong foundry support for single download, run
- Seamless integration into various analysis and simulation procedures

When Calibre® LVS, the layout vs. schematic physical verification tool, is paired with Calibre® xRC, the transistor-level parasitic extraction tool, it offers intentional device recognition (with device parameters) and parasitic device extraction at both the transistor and gate levels. By reading LVS structures directly, Calibre xRC provides complete circuit netlist information integrated to the source schematic and provides the highest levels of accuracy for post-layout simulation. (Fig. 6)

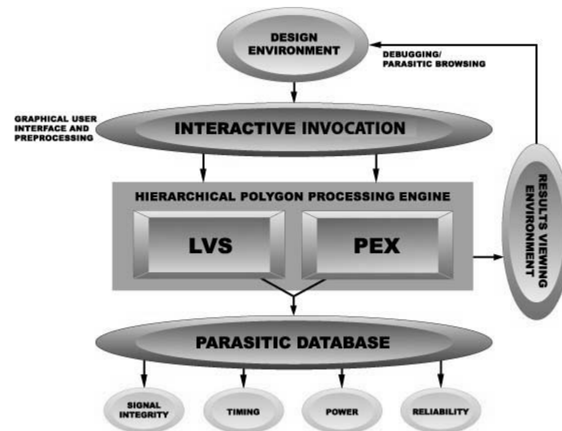


Figure 6. A tight link between LVS and parasitic extraction tools enables back annotation to the source layout. In the Calibre model, parasitic extraction is stored in a database for on-call, mixed-level analysis.

Calibre can be invoked from within popular design frameworks, such as Cadence® Virtuoso, through Calibre Interactive. This gives designers access to a single flow physical verification and parasitic extraction platform that is the internal sign-off standard of the majority of foundries. Calibre is also integrated with place-and-route flows, reading LEF/DEF and annotated GDS data, taking advantage of the connectivity information to produce gate-level netlists for gate-level simulators. The combination of Calibre LVS/xRC supports DEF with GDS and gate-level extraction on full GDS data to provide transistor-level information or to enhance the accuracy of gate-level results with parasitic information from the cells.

7. SUMMARY

Without comprehensive, accurate data, proper analysis and simulation of AMS SoCs is nearly impossible. By adopting a robust LVS tool that is tightly integrated with a full-chip parasitic extraction tool, accurate gate- and transistor-and multi-level extraction and post-layout simulation become possible. With costs of chip manufacturing and failure rates at first silicon at all time highs, designers can ill afford to overlook the effects of parasitics on the bottom line. Choosing tools that measure, and not merely assume, is key to developing working ICs. Designers achieve design closure and gain the confidence that their IC will function when manufactured. With increased capabilities, there will be no need to "over-engineer" the design to assure proper operation. The result is a design that meets operational specifications, uses space more efficiently and performs better. The result is profit.

7. REFERENCE

[1] *Collett International, 2001 IC/ASIC Design Closure Study.*

[2] *Collett International, 2001 IC/ASIC Design Closure Study*

[3] *Ferguson, J. White paper: "LVS-Parasitic Extraction Link," Mentor Graphics, 2003*