Beyond P-Cell and Gate-Level Assumptions

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Mentor Graphics®

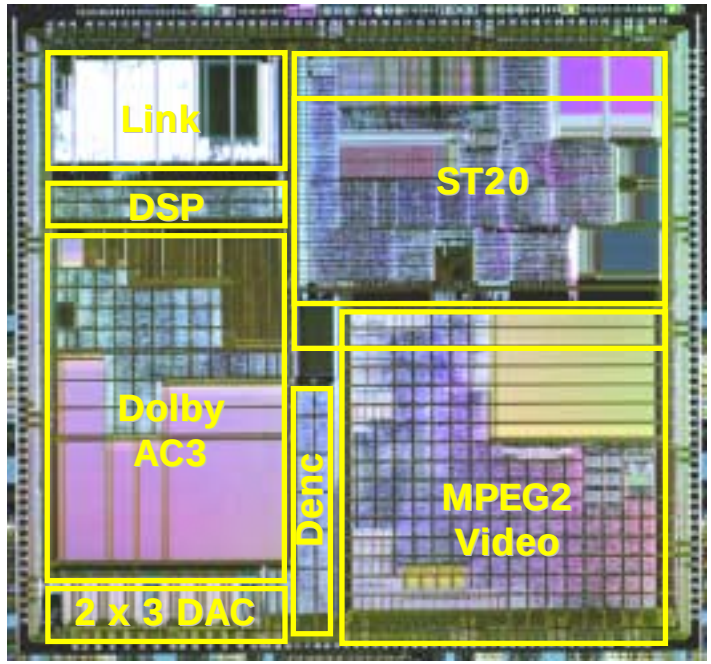
Design Complexity Drivers

Time-to-market:

Process roadmap acceleration

Consumerization of electronic devices

Aggressive adoption of 130 and 90 nm technologies



Complex systems:

uCs, DSPs, HW/SW, SW protocol stacks, RTOS's

On-Chip busses

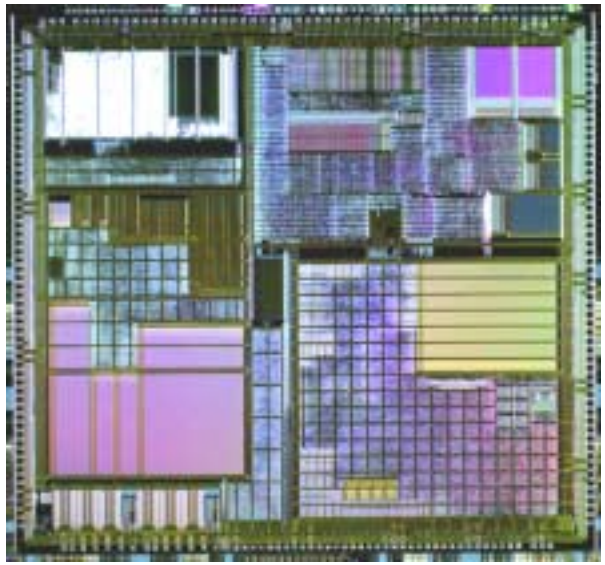
Digital/Analog IPs

AMS circuitry now found in 78% of SoC designs

Nanometer effects:

crosstalk
electro migration
wire delays
copper wires
RET, DFM

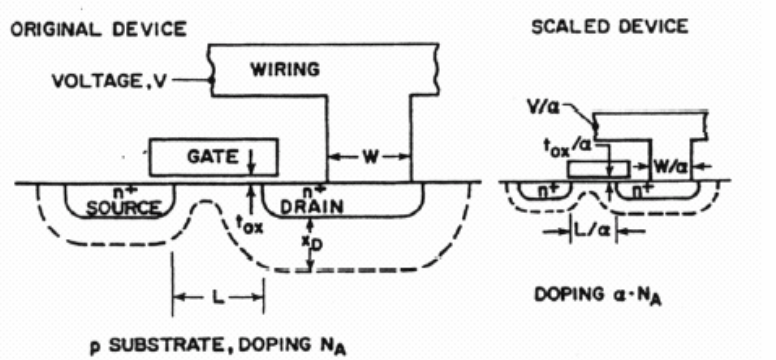
Feature Scaling: Friend & Foe



More Functionality per Chip
Network Processors
Wireless Comm
Audio/Video Systems
Imagers
Memory
Processors

Affordable ICs

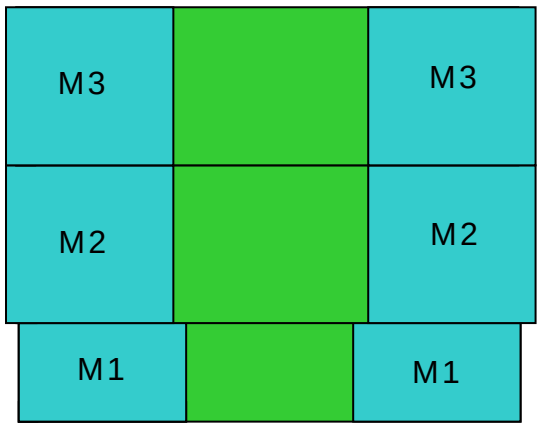
Smaller Feature Size:
50% of Annual IC Functional Cost Reduction
Sematech, IC Insights



Faster Devices & Faster Systems

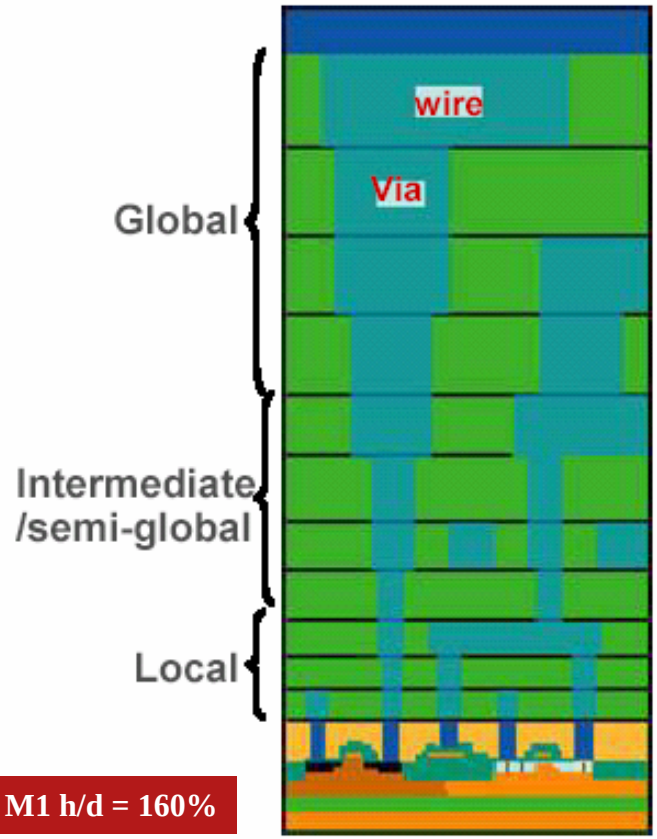
Feature Scaling: Drives Physical Design Complexity

0.6 micron Process
3 metal layers



M1 h/d = 80%

130nm Process
9+ metal levels



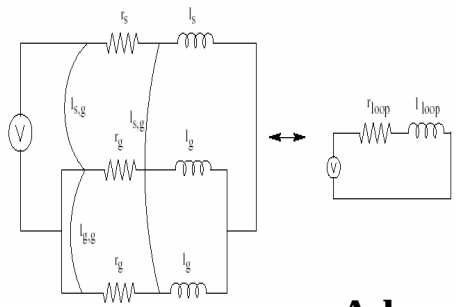
M1 h/d = 160%

Source: ITRS Roadmap 1999

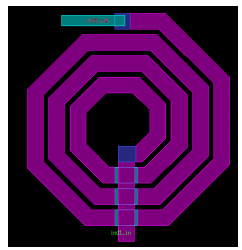
New Physical Effects of Nanometer Processes

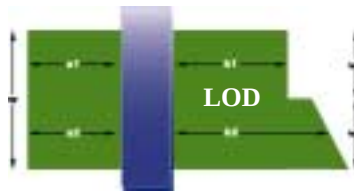
‘New’ RC Effects

Parasitic Inductance

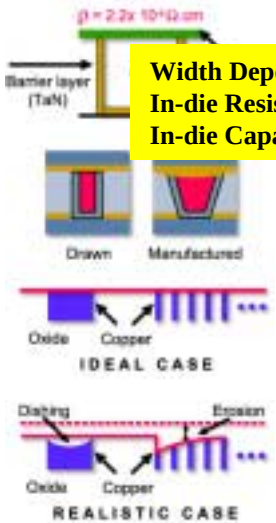


Advanced Device Parameters



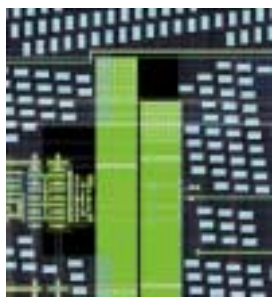


Copper Processing Issues

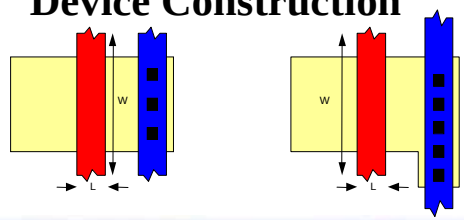


Width Dependent Resistance
In-die Resistance Variations
In-die Capacitance Variations

Planarity Fill



Actual vs. Intended Device Construction



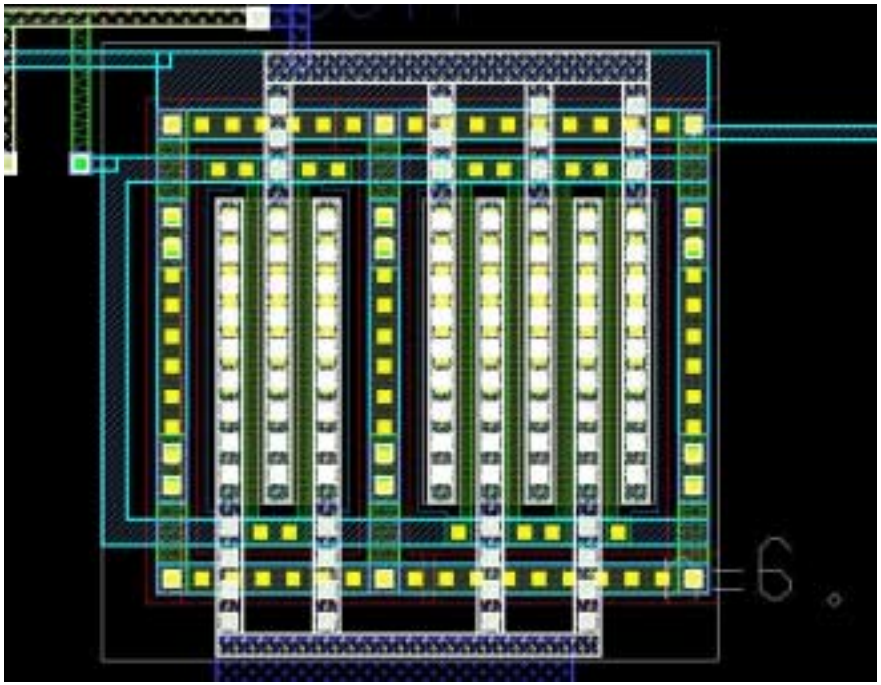
Nanometer Silicon Modeling Defined

- **nSiM = Post-Layout Circuit Model**
  - **Accurately accounts for silicon electrical effects**

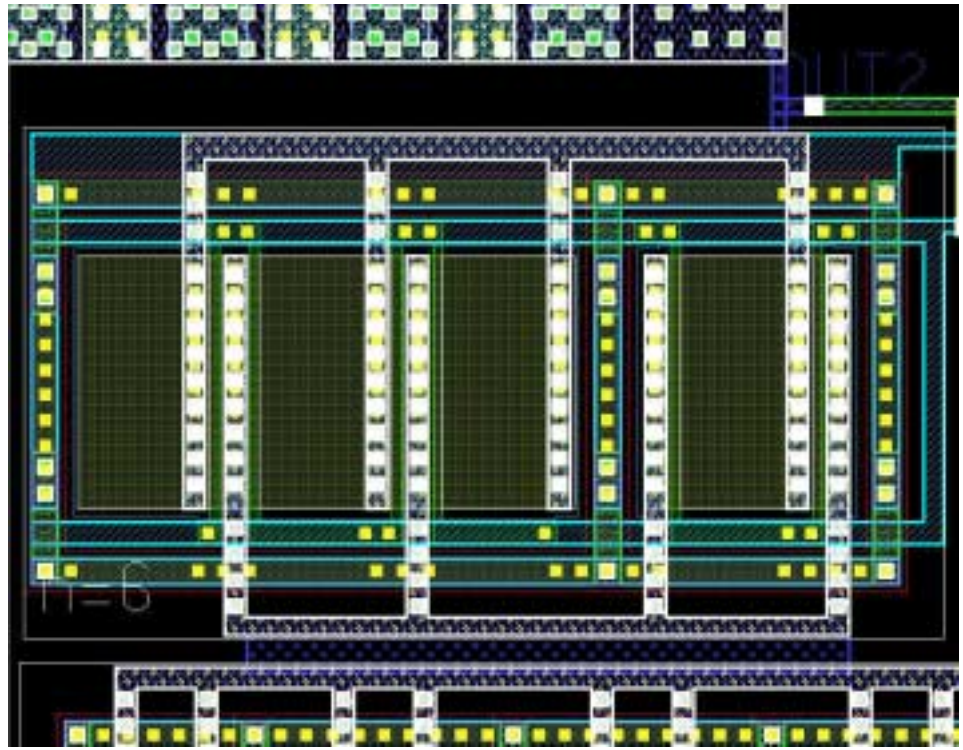
- **Two Parts**
  - **Intentional device models**
    - **Account for actual parameters in layout**
  - **Interconnect models (parasitics)**
    - **Account for nm silicon effects**

- **Essential Characteristics**
  - **Include all data relevant to target analysis**
  - **Be easily & rapidly generated**
  - **Provide compact, tractable representation**
  - **Readily feed post-layout analysis tools**

How Does Drain/Source Area Effect Output Frequency?



Transistor #1



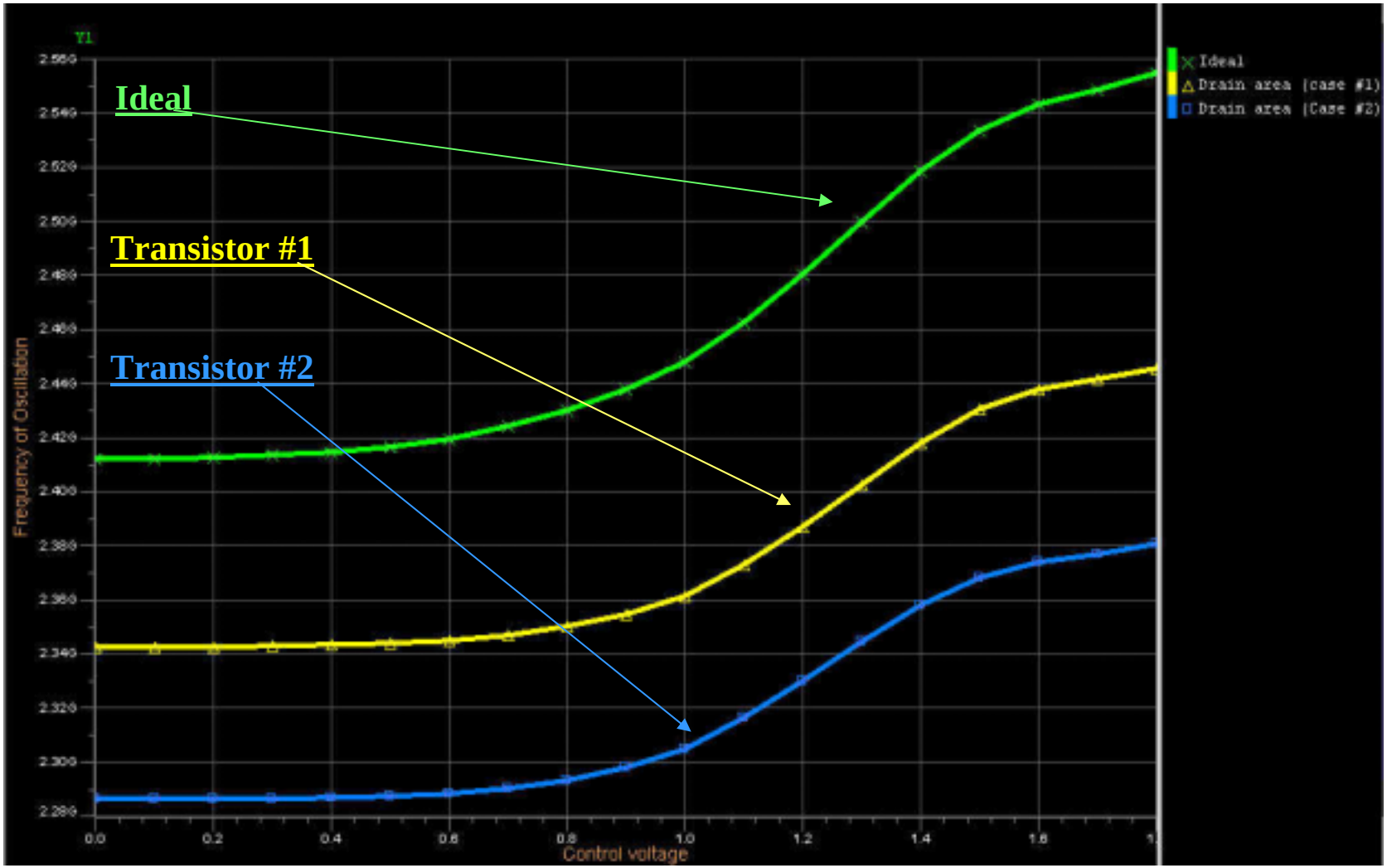
Transistor #2

Same W & L but, different drain/source area

Results/Comparisons

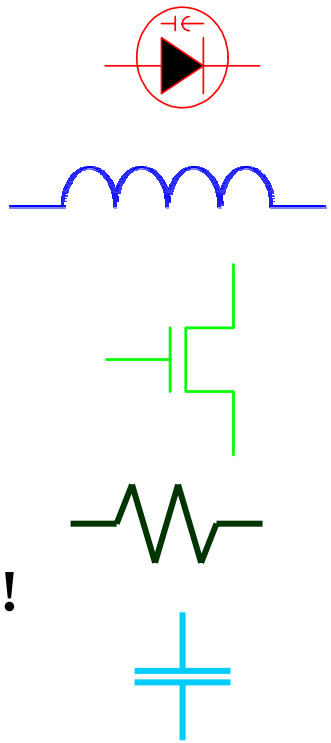
	Ideal VCO	VCO w/Diffusion	VCO w/C	VCO w/RC	VCO w/RCC
f_o	2.4119 GHz	2.34 GHz	2.203 GHz	2.135 GHz	2.13 GHz
Error	-	3%	8.6%	11.4%	11.7%
PN (dBc/Hz)	-124	-122	-121.6	-110	-103

Drain/Source Area's Effect Comparison



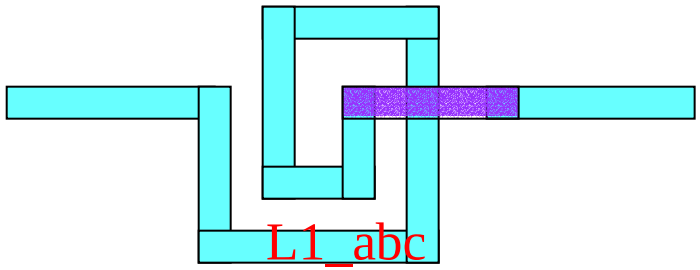
Accuracy: Device Extraction

- Transistors, Resistors, Capacitors, Inductors, Varactors
- User-Defined Devices
- Parameter Extraction
  - W, L, AS, AD, PS, PD
  - User Defined Parameter
- Device Reduction
  - User defined parameter reduction
- Accurately extract intentional devices in the circuit!

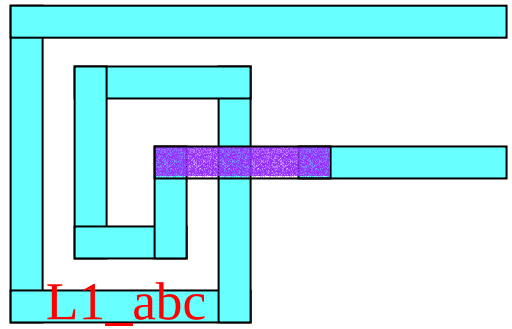


Example: Modified Inductor

Original Pcell



Modified Pcell



Read parameter method

```
If text = L1_abc
Then T = 1.5
```

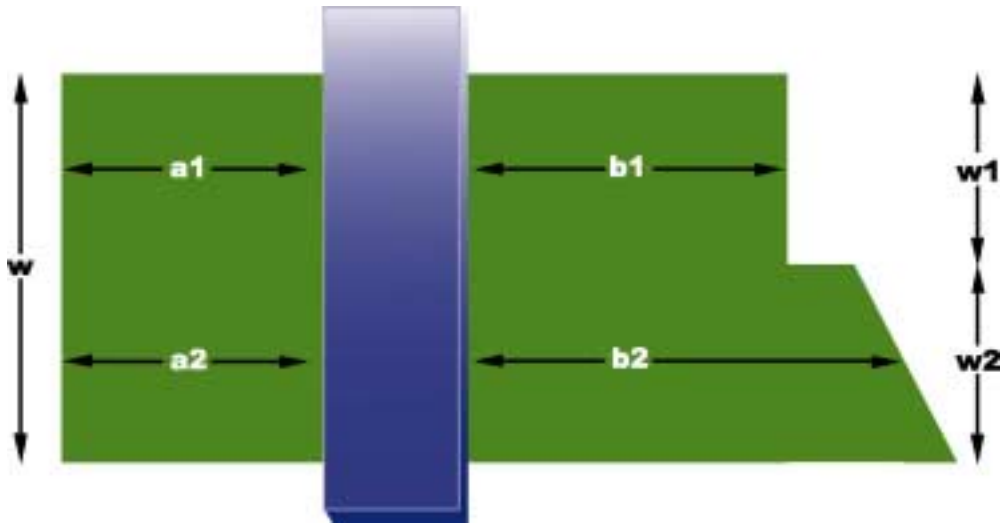
Calibre Physical Parameter Extraction

```
T = NumCorners*90 / 360
```

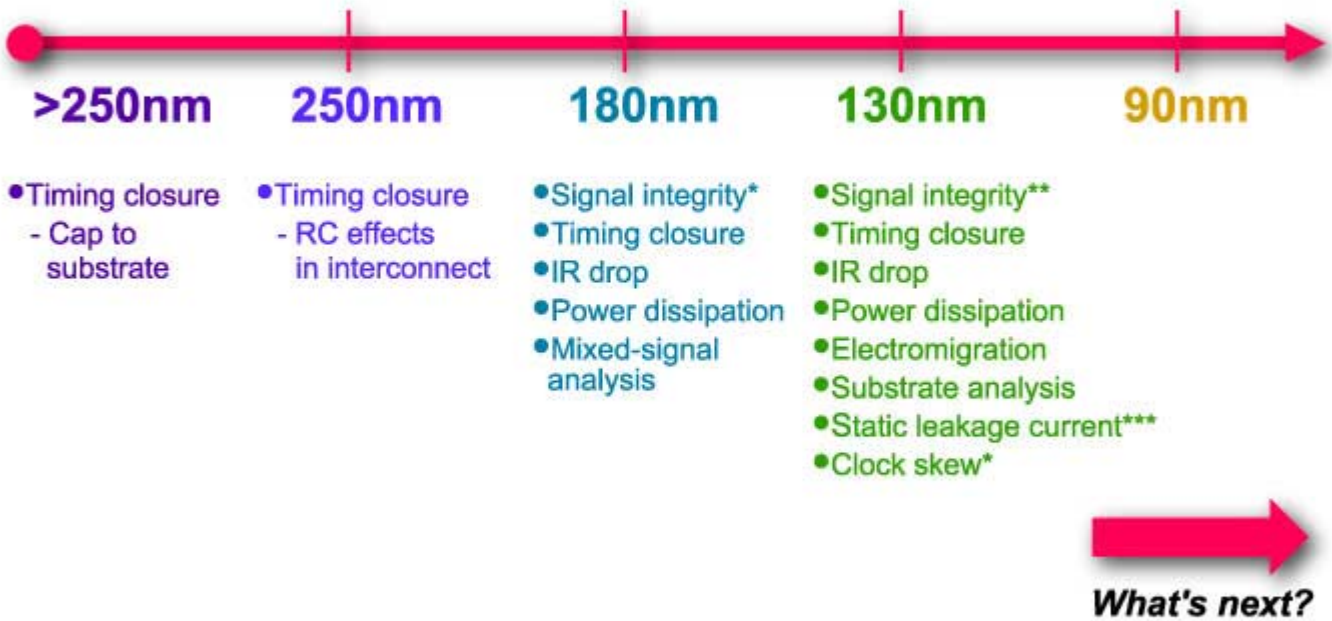
Case	Open-loop	Calibre
Original	**T = 1.5**	**T = 1.5**
Modified	**T = 1.5**	**T = 1.75**

New Parameters For Nanometer Devices

- **Length Of Diffusion**
  - **AKA Stress Effect (Stress Induced Mobility Modulation)**
- **Needed in LVS, PEX, and Simulation**
  - **Already exists in Calibre LVS/xRC, Eldo**
- **Difficult to Capture in Schematic**



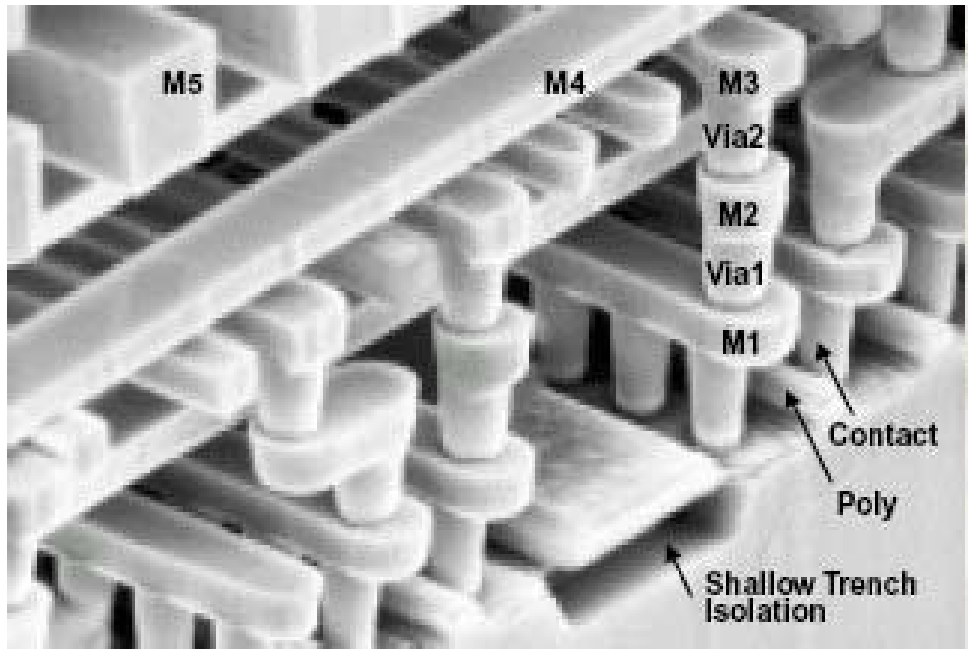
Extensive Analysis Required to Catch Nanometer Design Closure Issues



Nanometer Analysis Requires Nanometer Silicon Modeling

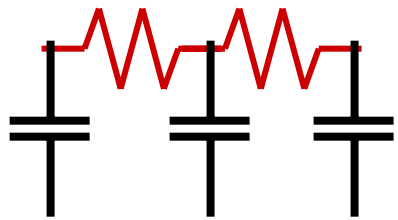
Calibre Nanometer Silicon Modeling Accounts for New Physical Effects

- Expanded set of parasitic elements
- Complex nanometer interactions
- Copper processing effects and compensation
- Actual vs. intended intentional device parameters



New Analysis Demands

- **Traditional Analysis required accurate parasitic info**
  - **RC, RCC, now RLC**

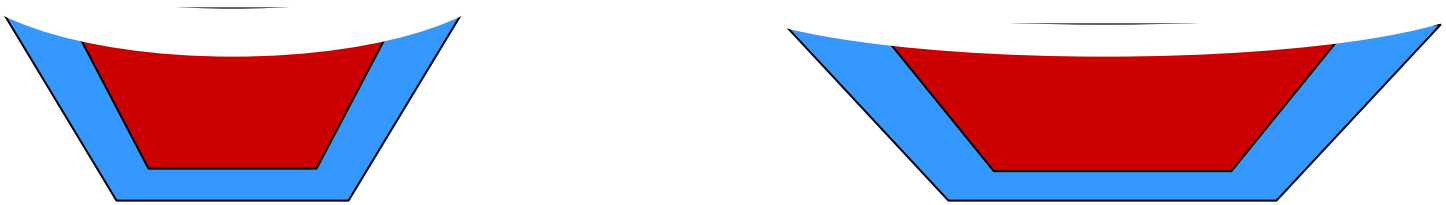


- **New Paradigm**
  - **Accurate Parasitics annotated to Accurate Geometric info**
    - **X,Y Locations**
    - **Width, Length**
    - **Layer**
    - **# of contacts**
  - **Current Density Measurements**
  - **Hierarchical**

Impact of In-Die Variation

- **Previously, fixed cross-sections could be assumed**

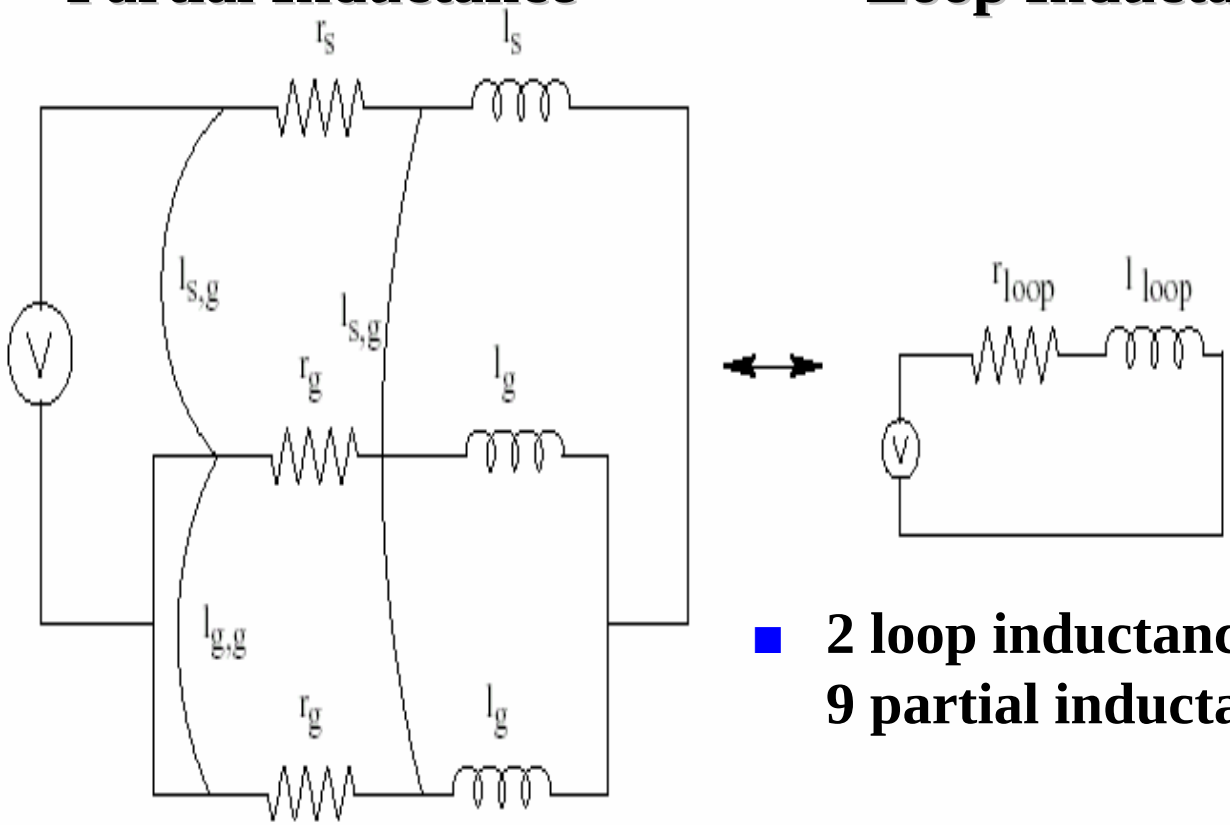
- **Height was fixed**
  - **Fixed Sheet Resistance for each interconnect layer**
- **Copper process <130 nm, manufacturing impacts cross-section**



- **Resistance now a function of width/spacing of conductors**

Loop Inductance Benefits

Partial Inductance **Loop Inductance**



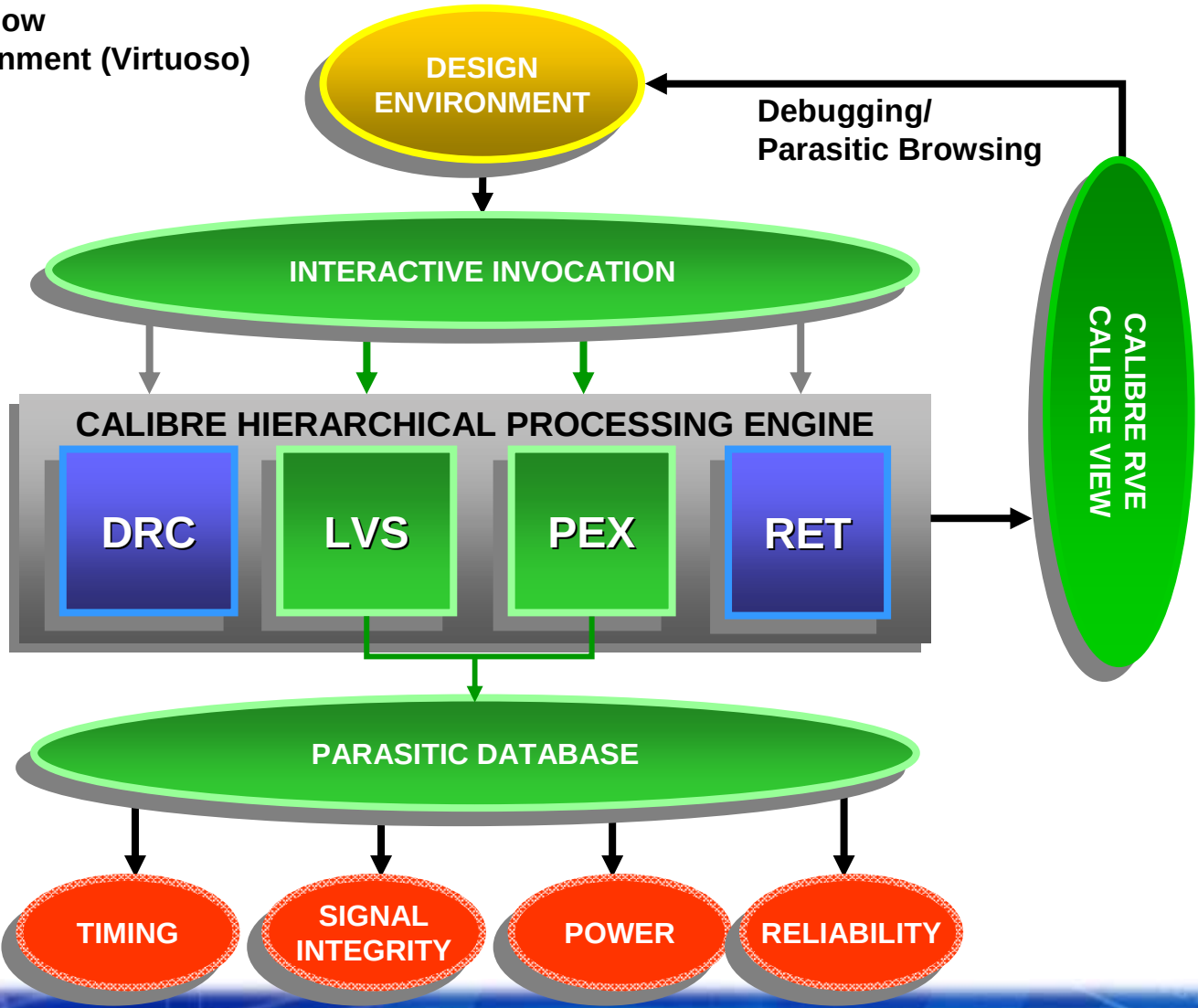
- **2 loop inductance values vs. 9 partial inductance values**

Loop inductance:

- **Smaller netlists; Improved simulation performance**

Enabling Post-layout Analysis

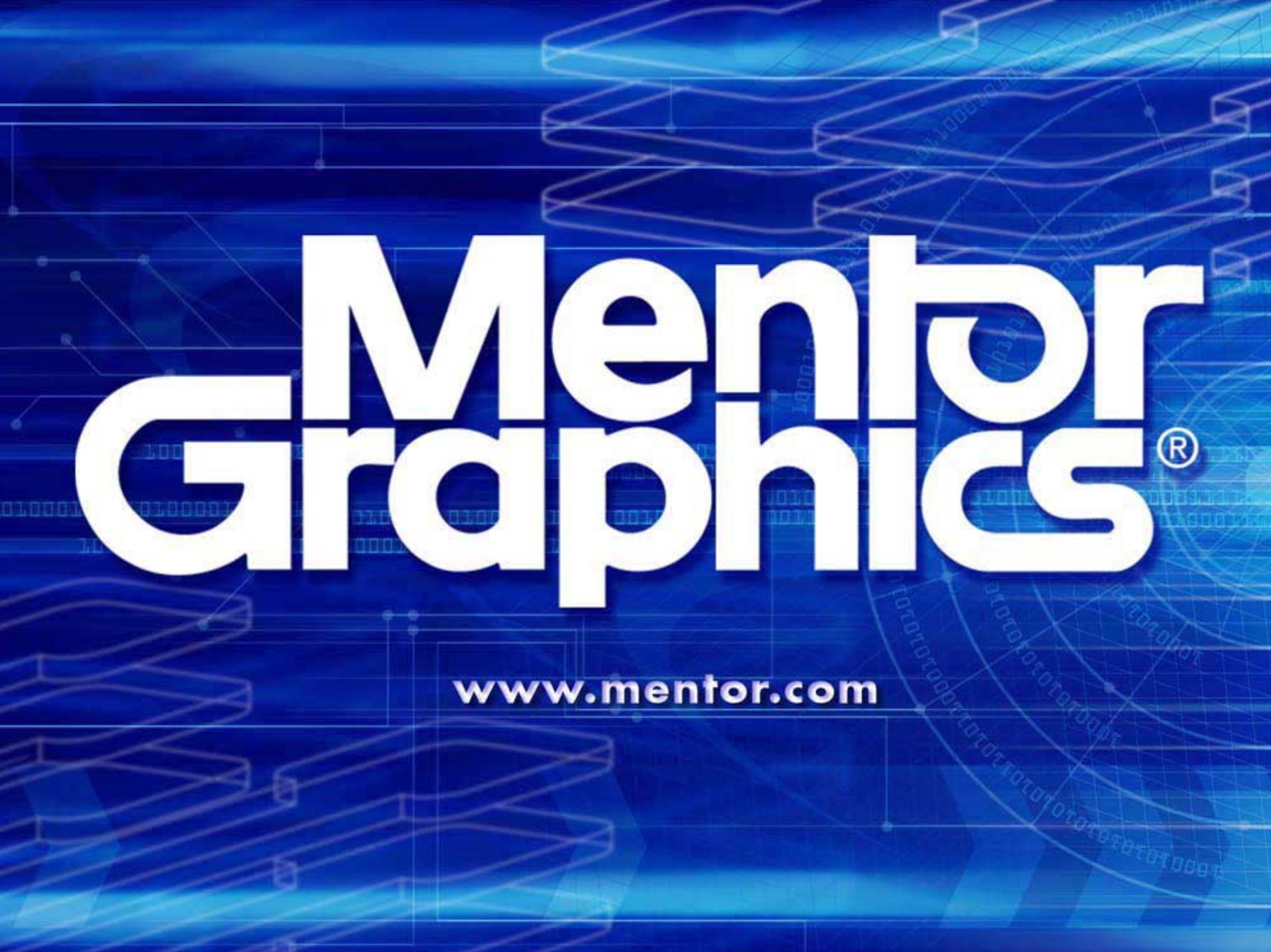
Mentor Graphics AMS flow
Cadence Design Environment (Virtuoso)
Milkyway
Magma
Open Access
Encounter



ADMS, Eldo, Mach,
HSIM, Spectre, HSPICE
Nanosim, PrimeTime

Calibre Nanometer Silicon Modeling: Enabling Analysis to Prevent Respins

- **Accurately Addressing Nanometer Effects**
  - **Resistance, Capacitance, Inductance**
- **Intentional Device Models Reflect Layout**
  - **Tight integration between LVS & xRC**
- **Performance & Capacity to Handle Large Designs**
- **Compact Si Models Enable Analysis of Large Designs**
- **Mixed-Signal Silicon Model Composition**
  - **Single Flow for Transistor & Gate Level Extraction**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