# HeatGen: A Vectorless Approach to Switching Activity Generation for IC Power Analysis

Wolfgang Roethig<sup>1</sup>, Maddu Karunaratne<sup>2</sup>, Bijan Panahi<sup>1</sup>

<sup>1</sup> NEC Electronics America, Inc., Santa Clara, CA 95050, <sup>2</sup> V-Cube Technology Corp., Fremont, CA 94359

## Abstract

This paper describes a new approach to generate switching activity for realistic worst-case power analysis of integrated circuits. The approach is implemented in an EDA tool called HeatGen.

# 1 Introduction

The impact of power consumption and voltage drop on design performance has become a significant issue in modern IC design. The scenario under which power consumption and voltage drop are calculated has to cover a realistic worst case for switching activity. Traditionally, the methods for switching activity generation fall into the following categories: simulationbased and estimation-based. Both methods rely heavily on user input. Simulation gives an exact result for a given stimulus, but the user-supplied stimulus may not provide sufficient coverage. On the other hands, static or probabilistic switching activity estimation methods give inexact results. Therefore built-in pessimism is required. Unfortunately, neither optimism nor too much pessimism is affordable for high performance designs. This paper describes a novel method to activity calculation and stimulus generation for SoC power analysis. Our method is vectorless in the sense that a user-supplied test bench with design-specific simulation vectors is not required. The stimulus is created automatically based on library models. The method is implemented in a tool called HeatGen. Instead of randomly maximizing the nodal switching activity at the boundary of a cell instance in the way of a classical ATPG tool, characterization vectors associated with particular circuit operations of a library cell are activated systematically. The characterization vectors themselves are described in the IEEE 1603-2003 Advanced Library Format (ALF). HeatGen internally generates a set of switching activity scenarios for the design and represents them in a global activity file (GAF).

The following section 2 describes the underlying library model for both simulation-based and vectorless power analysis. Section 3 describes the activity generation methods, especially the novel method implemented in HeatGen. Section 4 presents results and a conclusion.

# 2 Power library models

Our power analysis method is based on characterized energy vectors in a cell library, described in the IEEE 1603-2003 Advanced Library Format (ALF). An energy vector is an event pattern involving transitions at the terminals of a cell, associated with specific energy consumption.



Figure 1 Example of ALF model for a library cell and an associated energy vector

Associating the energy consumption of a cell with an energy vector is the most accurate way of power modeling, since the energy vector represents both logical and temporal correlation within an event pattern. Calculating the energy consumption within a design can be subdivided into the following two tasks:

- 1. Obtaining the activity of the energy vector in a given time window
- 2. Calculating the energy per vector

Power consumption is obtained by simply dividing the energy consumption by the time window of interest. In this work we are focused on task 1. For task 2 we are using a commercial power calculator, as the energy per vector can depend on transition time at an input terminal, load capacitance at an output terminal, supply voltage, temperature and other environmental parameters.

# **3** Activity generation methods

The methods for generating switching activity for power analysis can be categorized as probabilistic, simulationbased, and vectorless. A probabilistic method involves calculation of switching activity at an output node of a cell based on switching activity and state probability at its input nodes. In probabilistic switching activity calculation it is expensive to take logical correlations into account and it is almost impossible to consider temporal correlations. Therefore the calculated nodal switching activity is only a rough estimation. Furthermore, nodal switching activity alone is not sufficient. The activity of the energy vector is needed for accurate power calculation. Since an energy vector involves logically and temporally correlated events, the probabilistic method is not suitable.





Simulation-based switching activity generation is the most widely used method. The simulator is feeding an energy vector monitor. The monitor either processes the simulation events as they occur or post-processes a simulation dump file. Either way, a record of the energy vector activity is created and represented in a global activity file (GAF). Simulation-based activity generation is as exact as it can be, but the quality of results depends strongly on the quality of the stimulus.

Often it is not clear whether the user-provided stimulus represents a scenario of interest, especially for worst-case power consumption. Therefore, vectorless methods exist. A static vectorless method would not do any simulation, but simply assume that all energy vectors are always activated at the time when they can be possibly activated. Such an assumption is extremely pessimistic, but guaranteed to generate a worst-case. Some constraints, for example constant inputs, simple cases of logic exclusivity etc., can be applied to reduce the pessimism. However, it is difficult to know, how close the estimated switching activity is to reality.

Therefore we propose a new approach to vectorless power analysis. In this approach, a tool, called HeatGen, generates a stimulus for realistic worst-case switching activity automatically. HeatGen has a built-in simulator and energy vector monitor that directly generates the global activity file. The same power calculator and ALF power library as in the simulation-based method is used in this flow.



Figure 3 HeatGen power analysis flow

Stimulus generation is based on ATPG principles. ATPG is widely used today for fault simulation. However, the objective here is not to make faults observable, but to activate energy vectors. An energy vector is inherently more complex than a stuck-at fault. To observe an energy vector, a specific stimulus is required that satisfies he logical and temporal correlations described in the vector. Therefore the HeatGen tool has been created.





HeatGen compiles the design and library data and creates a database for energy vectors of all cell instances in the design. Then it picks a set of energy vectors and creates the stimulus that activates the set, based on the required circuit states. HeatGen tracks back as required to set the initial conditions for the targeted energy vectors. This procedure is repeated until all energy vectors of interest are activated.

Finally, a global activity file is generated and used for power calculation.

HeatGen works fully automatically, without user intervention. The user only sets conditions at the beginning, such as clock waveforms, constant inputs etc. HeatGen attempts to maximize the activation of energy vectors by a stimulus as compact as possible. Therefore the stimulus represents a more severe scenario for power consumption than typical user-supplied vectors. Since HeatGen has a built-in simulator that rules out logically impossible situations, the created scenario is more realistic than one obtained using a probabilistic or static method.

# 4 Results

We applied HeatGen on a real design block consisting of 15000 instances of standard cells and memory blocks. For comparison, a user-supplied stimulus was given. The user claimed that the stimulus represented the worst possible scenario for power consumption of the design block.

The same power library and the same power calculator was used in both simulation-based and HeatGen based power calculation. The constraints given to HeatGen (clock frequency etc.) were compatible with the usersupplied stimulus.





As shown in the diagrams, HeatGen created higher power consumption not only for the total design, but also for every cell type in the design. Also the break down of power consumption for each sub-block shows higher power consumption based on HeatGen.



The most interesting case is the sub-block U2, which has the highest power consumption in both the simulationbased and the HeatGen-based scenario.

The nodal toggle count (or nodal switching activity) of node 0 through 70 is significantly higher in the usersupplied stimulus than in HeatGen. However, the nodes 71 through 340 are barely activates by the user stimulus. The toggle count of the remaining nodes is comparable in both scenarios. Adding up the switching activity of all nodes, the user-supplied stimulus would yield a higher switching activity than HeatGen. However, the power consumption is significantly lower than in the HeatGen scenario. The reason is that HeatGen did not just activate nodes but energy vectors that actually caused the higher power consumption.

#### References

- G. D. Hachtel et al, "Probabilistic analysis of large finite state machines", Design Automation Conference, pp. 270-275, 1994
- [2] J. Monteiro and S. Devadas, "A methodology for efficient estimation of switching activity in sequential logic circuits", Design Automation Conference, pp. 120-17, 1994
- [3] C-Y Tsui et al, "Exact and approximate methods for calculating signal and transition probabilities in FSMs", Design Automation conference, pp. 18-23, 1994
- [4] F. Najm and et al, "Power estimation in sequential circuits", Design Automation Conference, pp. 635-640, 1995
- [5] F. Najm, "A survey of power estimation techniques in VLSI circuits", IEEE Transactions on VLSI Systems, vol. 2 no. 4, pp. 446-455, Dec. 1994
- [6] Chuan-Yu Wang et al, "Maximum power estimation for sequential circuits using a test generation based technique", IEEE Custom Integrated Circuits Conference, 1996
- [7] J. N. Kozhaya and F. Najm, "Accurate power estimation for large sequential circuits", IEEE Intl Conf on CAD, 1997
- [8] E. Corno et al, "ALPS: A peak power estimation tool for sequential circuits", 8th Great Lakes Symposium on VLS, pp. 350-353, 1999
- [9] M. S. Hsiao, "Peak power estimation using genetic spot optimization for large VLSI circuits", European Design Automation and Test conf. 1999
- [10] IEEE Computer Society, "1603<sup>TM</sup> IEEE Standard for an Advanced Library Format (ALF) describing Integrated circuit (IC) technology, cells, and blocks", published by the IEEE, 20 Feb. 2004 (Print: SH95179, PDF: SS95179)