Impact of Signal Integrity on System-On-Chip Design Methodologies

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ABSTRACT

Signal integrity has become a first-order concern in System-on-a-Chip (SoC) design. As a result, SoC design methodologies need to be fundamentally transformed. A key step in this transformation is the development of techniques to enhance block reuse while accounting for signal integrity. In this paper we describe how the standards work pursued at the Virtual Socket Interface Alliance's Signal Integrity initiative integrates with SoC design methodologies and enhances block reuse.

Keywords

Signal, integrity, design, methodology.

1. INTRODUCTION

Signal integrity (SI) has become a first-order concern in System-on-a-Chip (SoC) design [1][2][4]. The only way to effective address SoC SI issues is to modify SoC design methodologies to fundamentally incorporate SI information in the design flow, within existing tools, or with the additions of completely new design flow steps [5][6]. A key step in this transformation is the development of techniques to enhance block reuse while accounting for signal integrity.

In this paper we describe how the standards work pursued at the Virtual Socket Interface Alliance's (VSIA) Signal Integrity initiative integrates with SoC design methodologies and enhances block reuse.

VSIA standards specify and explain deliverables, data formats, associated design guidelines, and example designs for the SoC issues. Signal-integrity issues of both digital and analog mixed-signal virtual components (VC) are obviously very important in SoC design. VSIA's SI specification is focused on exactly those issues in the communication between the VC authors and integrators of digital and analog/mixed-signal (AMS) blocks, including the design of the interfaces [2]. In this specification, it is assumed that the virtual components are provided for integration as hard blocks. Such a scope for the specification clearly influences the space of SoC design methodologies that are compliant with the specification.

The scope of the work is defined by the boundary conditions, and is currently limited to supply and power grids, interconnect crosstalk, and substrate coupling, both for uniformly doped silicon substrates and silicon substrates with an EPI layer on heavily doped bulk substrates. This document also discusses the issues related to power grid and signal electromigration. Issues such as IC package noise are very important to understanding the noise SI issues in SoC design, but consistent with other VSIA specification documents, they are currently out-of-scope.

The specification referred to in this paper focuses on 0.18um processes dealing with issues that may occur down to 70 nm and beyond. The SI issues covered are experienced in processes after 0.18um, and much of the specification and this paper can be applied to help design block transfer in these technologies. The 180-nm technology node range, however, meets the design requirements of the majority of current chip integrators.

Issues are also classified and considered based on current and future severity and seriousness, verifiability before manufacturing on silicon, and appropriateness for the documented information between the component author and integrator.

2. SI DELIVERABLES AND THEIR IMPACT ON DESIGN METHODOLOGIES

Table 1 illustrates some of the deliverables that are specified in VSIA's SI specification, Version 2.0. Note that not all deliverables are there, nor are the formats of standards (e.g. Spice) referred to in each of them. The VSIA specification contains all of these

details. This specification has been agreed upon by representatives from more than 10 corporate sources.

As it can be seen on the table, there are several kinds of deliverables, including logical, timing, electrical, and physical.

Illustration of VSIA SI deliverables.

Interconnect Crosstalk (Voltage Noise and Delay Variance)	
Electrical data	Physical data
Maximum noise at ports Max crosstalk for sensitive nets Electrical characteristics for aggressors and sensitive nets Best, worst case slews at ports Max load/RC at ports	Location of sensitive polygons Location of strong potential aggressors or No-fly zones Location of top-layer/peripheral supply wires "Safe" regions for OTH signals (possibly classified by slew)
Electromigration	
Logical data	Physical data
Mutex/One-hot relationships required between signals	Layout
Electrical data	Timing data
Current density limits,metal/via Max load on ports Max slew rate on inputs Max Switching factor Drive Strength	Variation of timing arcs within VC with external crosstalk Transition windows at ports Transition windows for potential aggressors or sensitive nets
Supply and Ground Grid Noise & Electromigration	
Electrical data	Physical data
Electrical data Specification Power Model Requirements	Geometrical data of supply nets
Variation in pin timing (delay, slew, setup, hold) from IR drop	Multiple supplies for analog blocks, multi Vt circuits, pads
Timing data	Other
Substrate Noise and Coupling	
Electrical data	Physical data
Block-level impedance model Noise sources, aggressor ports Max noise for "victim" port	Regions Substrate access ports

Figure 1 illustrates how the SI deliverables impact a typical design methodology composed on custom cell design, semi-custom digital synthesis-based design, and analog design sub-flows.

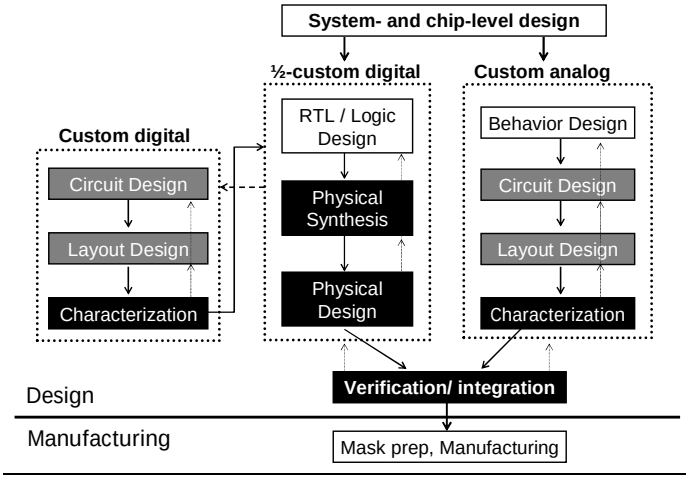

Figure 1 Impact of SI deliverables on methodologies.

In the figure, flow steps that are influenced significantly are shown in black with white fonts, steps that are moderately influenced are shown in gray, and steps that are not affected much are shown in white with dark fonts.

As the figure shows, the influence of SI issues and deliverables is higher towards the bottom of the design flow, where the electrical and physical issues are most relevant. However, SI is also important higher in the abstraction hierarchy, as early design decisions in SoC design can have a significant influence on the success of the design – and this affects SI issues intensely.

3. AN ELECTRICAL PHENOMENON

Based on the above it should come as no surprise that Signal Integrity issues in Systems-On-Chip tend to be focused on the low-level side of design tasks. This is supported by the VSIA SI specification data. As shown in Figure 1, most of the deliverables specified – out of almost 50 of them - are in the electrical and physical realm. In fact, the chart implies that Signal Integrity issues in SoC integration are fundamentally of electrical nature.

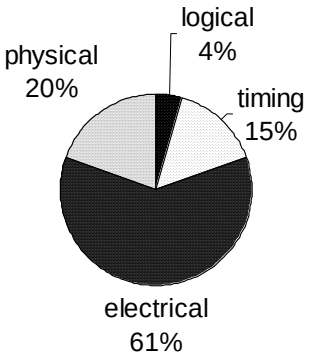

Figure 2 Types of SI SoC design task deliverables.

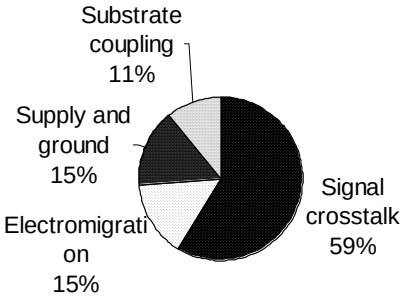

Figure 3 Types of SI SoC deliverables based on the SI phenomenon they address.

4. CROSSTALK A KEY CONCERN

Perhaps more interesting is the fact that, from all the signal integrity concerns, crosstalk seems to require more reuse support than other concerns. At least this is what the VSIA SI specification deliverable lists suggest. As shown in Figure 1, most of the deliverables specified are related to the management of crosstalk when integrating or generating SoC cores.

Electromigration and supply and ground management come right after crosstalk, and substrate coupling is the least frequent concern in the deliverable list.

There may be multiple reasons for this data:

Crosstalk is indeed a primary concern *today* for engineers trying to generate or integrate a core on an SoC.

Other phenomena such as substrate coupling are slightly less of a concern at this time for non-mixed-signal systems, but - more importantly - somewhat less understood.

Crosstalk tends to affect more wires – for example, there are usually more data-carrying signals than supply and ground wires.

5. STANDARD REUSE IN SOC METHODOLOGY

When a new standard format and/or interface is created, a substantial overhead is often required to adapt the methodology to the particular specification defined. The VSIA SI initiative has aimed at reducing this overhead while maximizing interoperability by reusing as many existing standards as possible (including de facto standards).

It turns out that there are a variety of formats that are perfectly suitable for capturing SI information necessary to generate and integrate complex SoCs. As Figure 4 shows, electrical Spice-like formats and standards turn out to be extremely useful to capture SI information, due to its fundamentally electrical nature. It is also notable, however, that “documents” have been agreed upon as a fundamental way to transport SI information between SoC IP developers and integrators. Indeed, the chart suggest that appropriate documentation is the key SoC methodology integration format when it comes to Signal Integrity information.

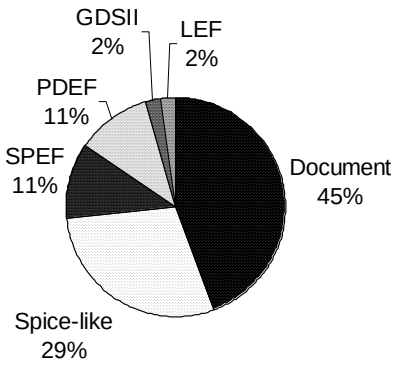

Figure 4 Formats/interfaces referred to in VSIA SI specification.

6. IMPACT ON KEY DESIGN FLOW STEPS

In this section, we outline certain aspects of the impact of SI on key design flow steps, from high abstraction levels to low abstraction levels.

6.1 Early design exploration

For early design exploration, the chip partitioning sub-flow is key for systems-on-chip. The analog-vs-digital division line is fundamental in signal integrity management, if actual spatial partitioning is done. But the mere functional division of circuits into analog and digital has a strong influence on SI impact as well –analog circuits tend to be more sensitive.

6.2 Impact of RTL/logic design

For RTL/Logic synthesis, SI only increases the need to accommodate electrical effects on synthesis. While this is not a new fact, the surge of SI effects near 100 nm has made this flow step a primary focus of SI embedding in the design flow.

As an example, crosstalk and supply noise have a strong influence on delay. Since modern synthesis is intimately related to timing, it becomes obvious that SI has become a primary factor to account for here.

6.3 Impact on circuit design

For the circuit design sub-flow, the impact of SI is obvious – SI is primarily a circuit-level phenomenon. But analog circuit topology and power are increasingly important and thus have popped up in the analog sub-flow of mixed-signal design methodologies.

6.4 Impact on layout design

For layout design, most of the SI impact on methodologies can be classified as some kind of embedding of isolation techniques in the design flow. While these techniques have been used for some time, they have become an increasingly common staple not just for mixed-signal but also for purely digital designs.

6.5 Impact on chip integration

For chip integration sub-flows, signal integrity has a renewed importance, given the rise of system-on-chip design. Floorplanning and – again - isolation techniques are some of the key steps for focus on.

7. CONCLUSION

Signal integrity has become a first-order concern in System-on-a-Chip (SoC) design. As a result, SoC design methodologies need to be fundamentally transformed. A key step in this transformation is the development of techniques to enhance block reuse while accounting for signal integrity. In this paper we have described how the standards work pursued at the Virtual Socket Interface Alliance's Signal Integrity initiative integrates with SoC design methodologies and enhances block reuse.

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