



Impact of Signal Integrity on System-On-Chip Design Methodologies

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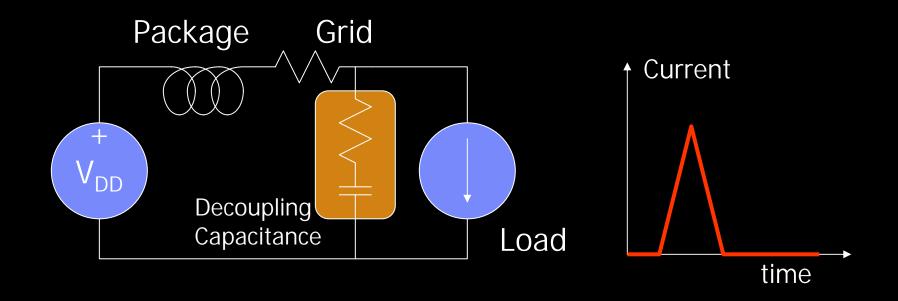
Introduction

Signal integrity

First-order concern in System-on-a-Chip (SoC) design

- SoC methodologies need to be fundamentally transformed Must develop techniques to enhance block reuse while accounting for signal integrity
- Reuse standards work can help achieve this goal
 Virtual Socket Interface Alliance (VSIA) → focus on reuse
 Signal Integrity (SI) sub-working group → focus on SI in SoC
 Work integrates with SoC methodologies and enhances block reuse

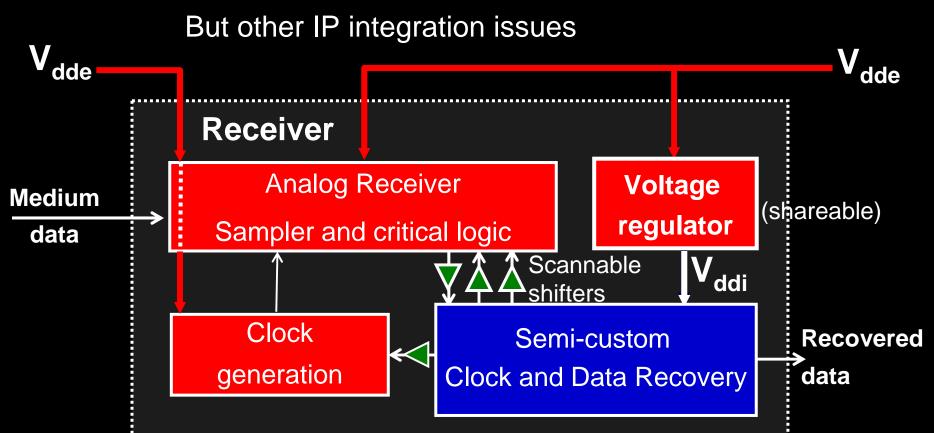
Example \rightarrow **Power Grid Issues**



• With package, maximum noise becomes: $V_{max} \approx \mu t_p R_g + \mu L - \mu R_g^2 C_d (1 - e^{-t_p/\tau})$ *DC Package Decap*

Example → Power Grid Issues Semi-custom Voltage Islands

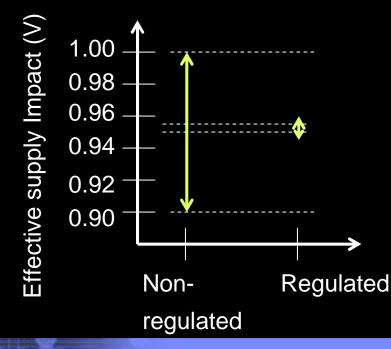
Reduce power, low overhead, better supply

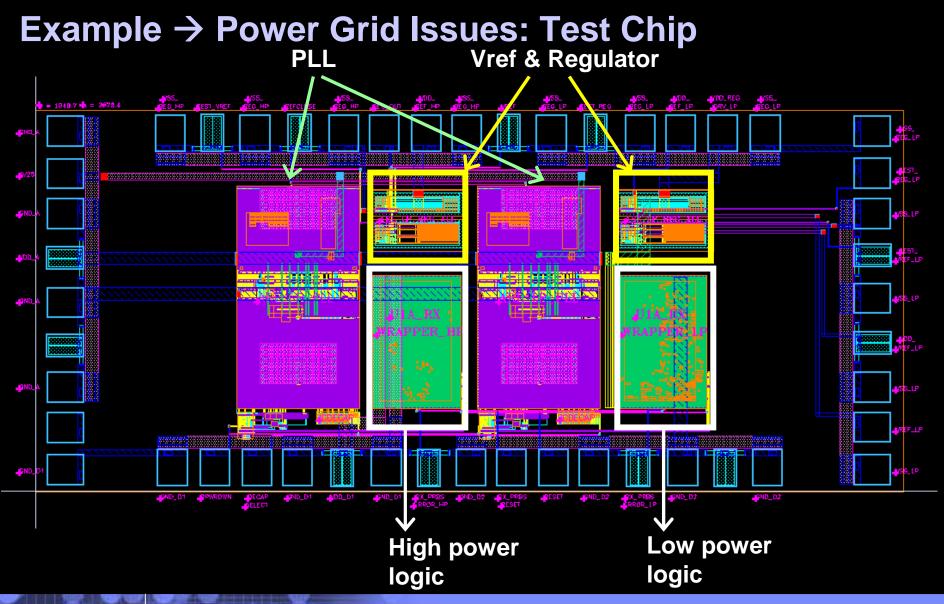


Example → Power Grid Issues Reduced Impact of Supply Variation

Effective supply variation reduced

But need to account for regulator-logic / inter-island interaction...





VSIA Signal Integrity Sub-DWG

- Part of Implementation DWG
 - Implementation-verification, AMS, SI

Scope

- Digital and analog blocks
- Signal integrity issues
 - Power grids, X-talk, substrate coupling, electromigration

Goals

- Facilitate "exchange" of digital & analog blocks in SoCs
- Improve author-integrator communication of SI issues

Assumptions

The blocks are provided for integration as hard blocks

Focus

Interconnect crosstalk

Signal Electromigration

Supply and ground grid noise and electromigration

Substrate coupling

Format

Deliverables

Include detailed tables Aid with implementation

Guidelines

Textual advice

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Example Table Entry

 Interconnect Crosstalk (Voltage Noise and Delay Variance) Electrical data

Number	Description	Format	Mandatory?	Comments
2.1.2.1.	Maximum permissible noise propagating into input ports	VC Hspice	Conditionally	If available, otherwise document in Section 2.4

Team

Main participants (not TSMC)

Motorola IBM Simplex

Intel

Startups (e.g. CommLSI)

Japan

Interconnect Crosstalk (Voltage Noise and Delay Variance)

Electrical data	Physical data
Maximum noise at ports Max crosstalk for sensitive nets	Location of sensitive polygons
Electrical characteristics for aggressors and sensitive nets	Location of strong potential aggressors or No-fly zones
Best, worst case slews at ports Max load/RC at ports	Location of top-layer/peripheral supply wires "Safe" regions for OTH signals (possibly classified by slew)

Signal Electromigration

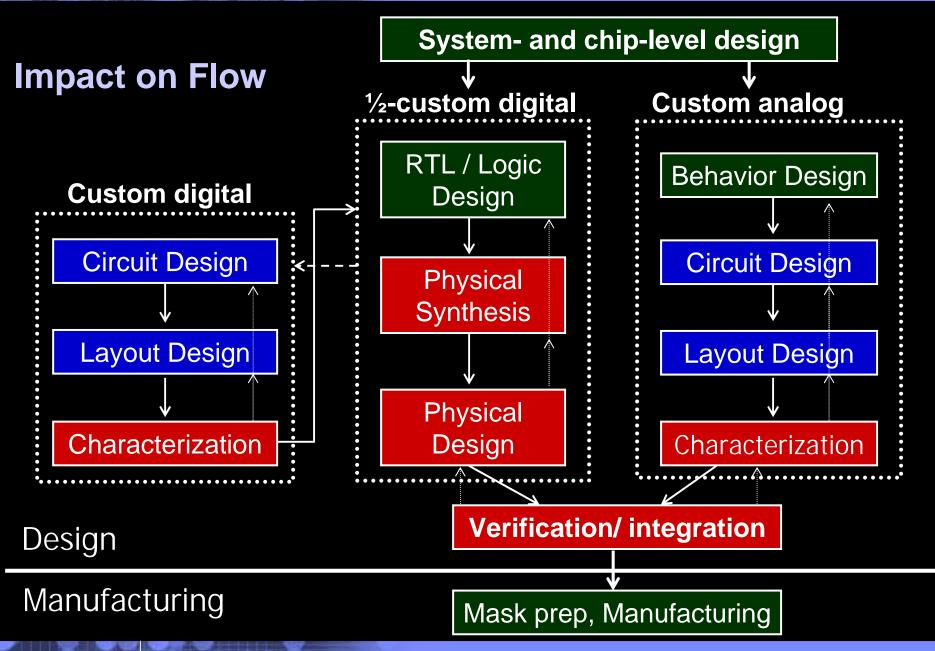
Logical data	Physical data
Mutex/One-hot relationships required between signals	Layout
Electrical data	Timing data
Current density limits,metal/via Max load on ports Max slew rate on inputs Max Switching factor Drive Strength	Variation of timing arcs within VC with external crosstalk Transition windows at ports Transition windows for potential aggressors or sensitive nets

Supply and Ground Grid Noise & Electromigration

Electrical data	Physical data
Electrical data Specification Power Model Requirements	Geometrical data of supply nets
Timing data	Other
Variation in pin timing (delay, slew, setup, hold) from IR drop	Multiple supplies for analog blocks, multi Vt circuits, pads

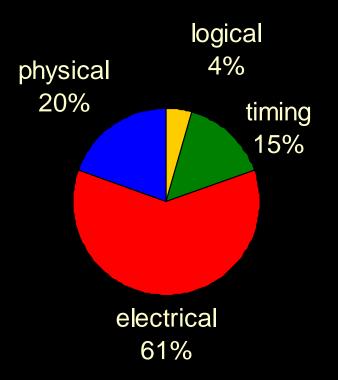
Substrate Noise and Coupling

Electrical data	Physical data
Block-level impedance model	Regions
Noise sources, aggressor ports	Substrate access ports
Max noise for "victim" port	



An Electrical Phenomenon

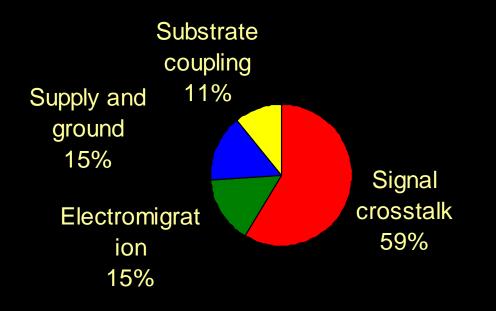
Types of SI SoC Task Deliverables



Crosstalk A Key Concern

Types of SI SoC Task Deliverables

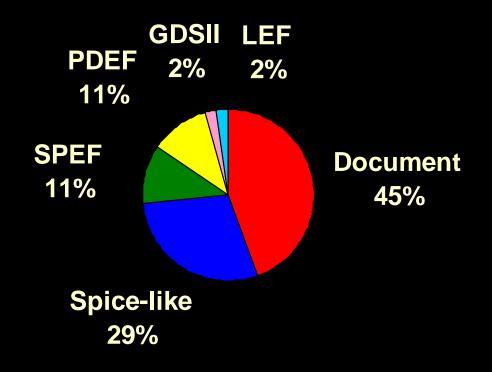
 \rightarrow based on the SI phenomenon they address

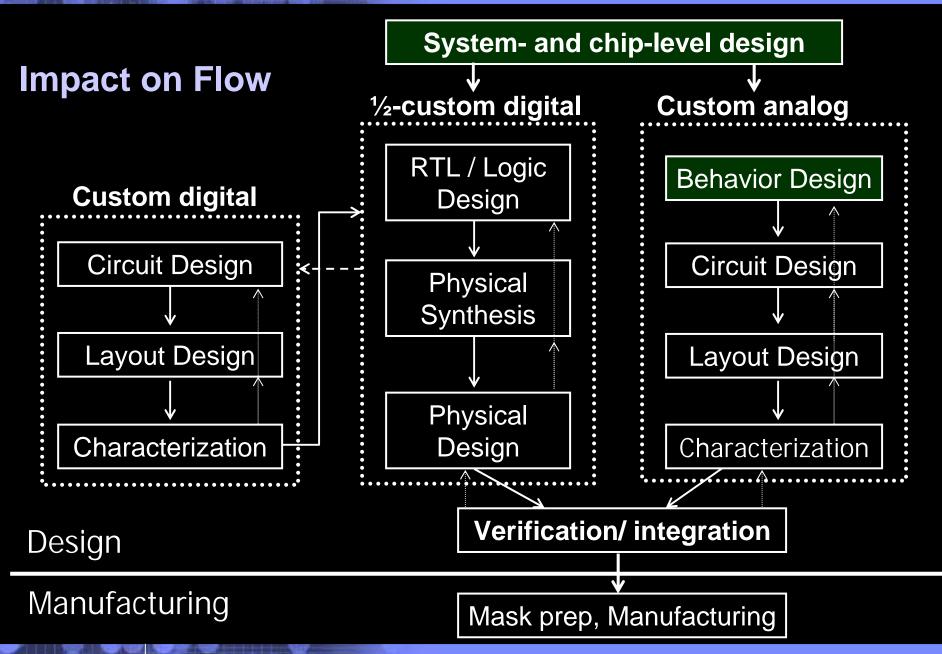


Standard Reuse in SoC Methodology

Formats/interfaces referred to in VSIA SI specification

More than 50% existing standards





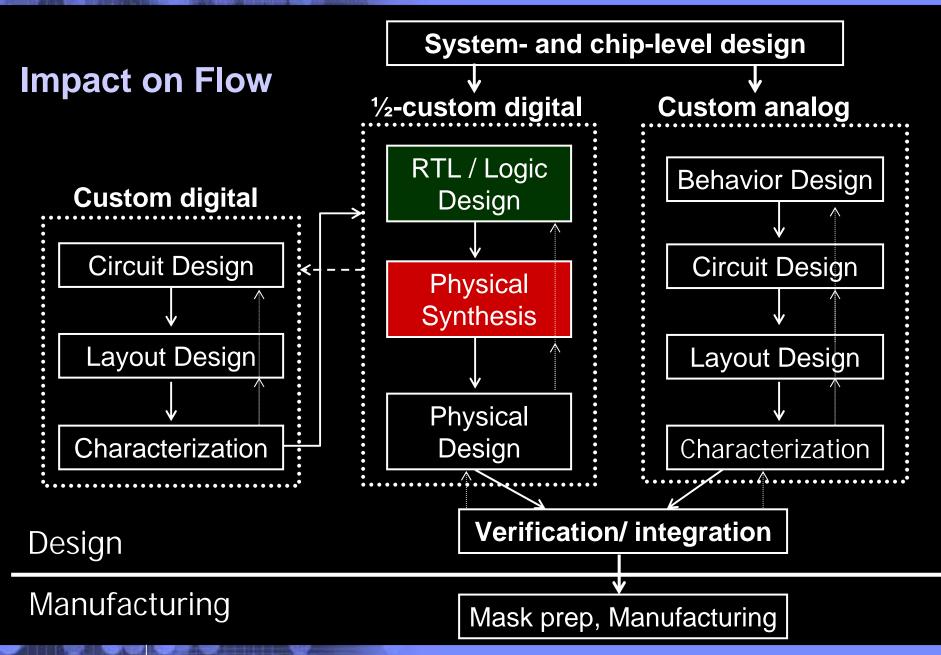
Impact on Early Design Exploration

Chip partitioning sub-flow

- → key for SoC
- → Determines wiring = electrical SI
- → Need to use standard SI block info

Analog-digital division line

→ fundamental in signal integrity management
 → if actual spatial partitioning is done
 → Functional division into A/D has strong influence on SI
 → analog circuits tend to be more sensitive.



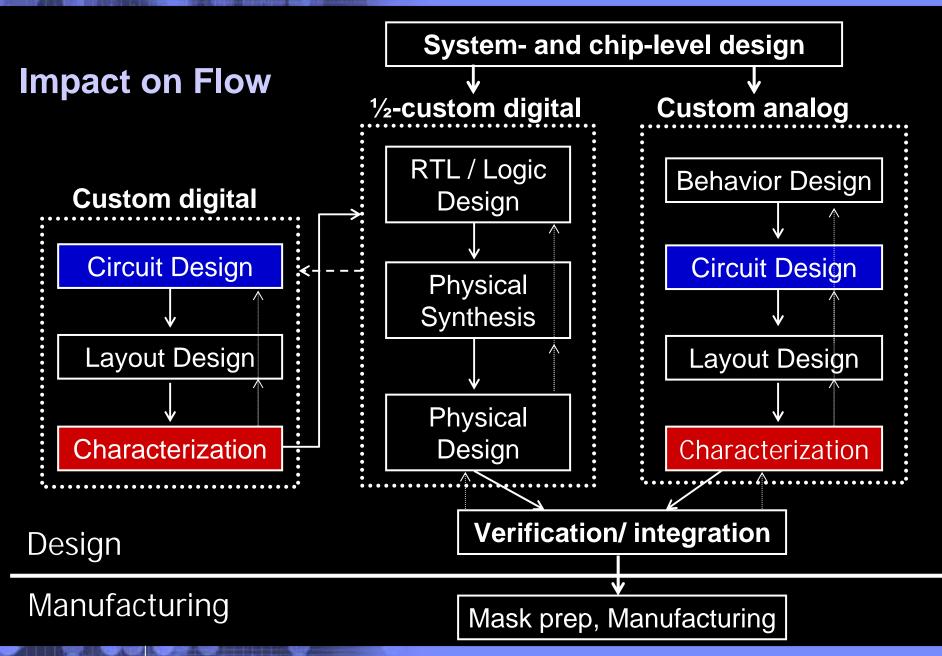
Impact on RTL / Logic Design

On synthesis

SI increases need to accommodate electrical effects surge of SI effects near 100 nm primary focus of SI embedding in the design flow

■ Example → crosstalk and supply noise

Strong influence on delay Modern synthesis intimately related to timing SI a primary factor to account for IBM Research – Juan-Antonio Carballo – EDP 2004



Impact on Circuit Design

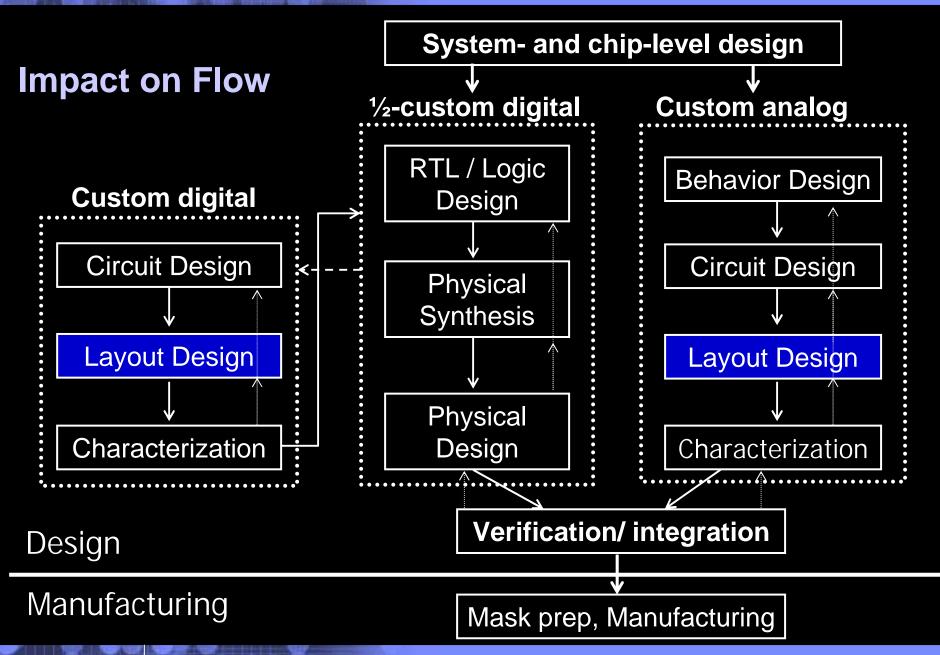
Impact of SI is obvious

 \rightarrow SI is primarily a circuit-level phenomenon

Characterization fundamental flow path for SI info

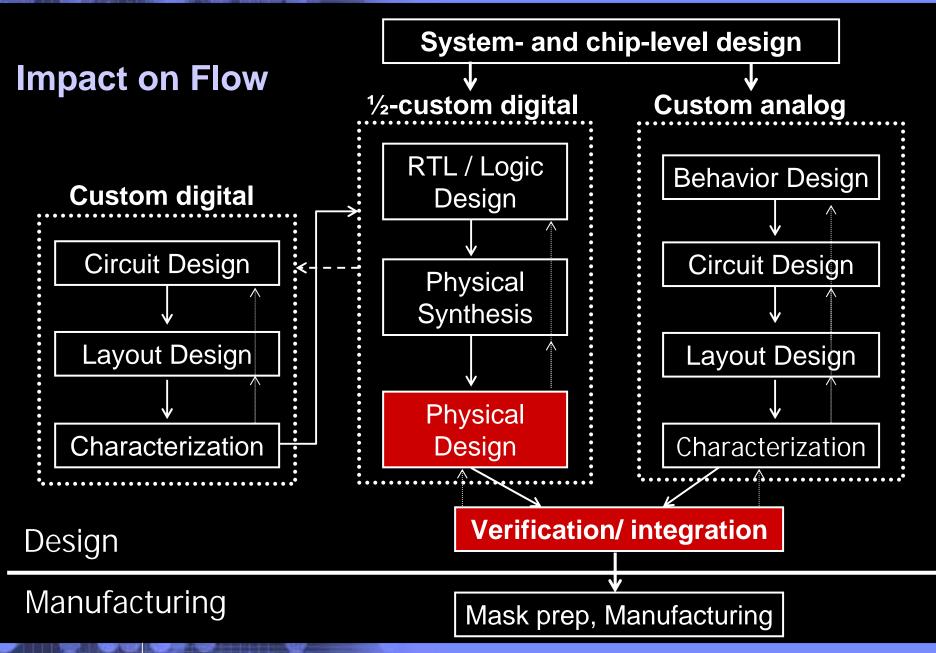
Analog

Circuit topology and power increasingly important Raised in analog sub-flow of AMS design methodologies



Impact on Layout Design

 Most of the SI impact can be classified as embedding of isolation techniques in the design flow Increasingly common in mixed-signal purely digital designs



Impact on Chip Integration

Renewed importance

Due to rise of system-on-chip design

- Key techniques
- 1. Floorplanning
- 2. Isolation

Conclusions

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Back-up Slides