Missing Analog Tools – A Proposal

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ABSTRACT
After some 50 years of analog and mixed-signal design (AMS), new analog tools and methodology are emerging to greatly improve the productivity of AMS design technology processes. These include emerging AMS synthesis, formal methods, and design languages. In this paper, we describe an area of much needed AMS design improvements that seems to largely have been overlooked. This area concerns the "lower levels" of typical AMS design processes usually handled "manually" by AMS designers using intuition, hand calculations, and simulator-aided non-automated manual approaches.

The paper first describes the several areas of analog and mixed signal design problems, the related need for productivity and impact of this situation.

The paper then proposes some specific analog/AMS tools that would greatly reduce the amount of manual detailed design effort, assist designers in keeping tabs on non-core-design mundane details with little effort, and should lead to improved productivity of analog designers. The target tools include such mundane analog design capabilities such as power, biasing, gains and margins, component value and tolerance setting, thermal, energy analysis, impedances, worst case, distortion, noise, and coupling.

General Terms
Design, Methodology, Algorithms, Verification.

Keywords
Analog, mixed signal, design, design process, tools, aids, design productivity, redesign

1. INTRODUCTION
Analog design technology has been developing in parallel to digital design technology for years. After some 50 years of analog and mixed-signal (AMS) electronics design, and with a growing demand for large areas of analog and mixed-signal circuitry on ever-larger integrated circuit chips, there is a companion need for ever-growing productivity of analog designers. The problem is to find areas in the analog design process where productivity can be improved.

2. A BRIEF HISTORY OF ANALOG DESIGN
Analog design over the years has typically focused on the techniques of circuit design, analog design innovation, the long pursued goal of high performance analog circuit simulation of larger, more complex analog circuits and systems, and intense manual detailed circuit design work by analog designers. Also, for many years, the mainstay of analog CAD tool efforts has been almost entirely on analog HDL and circuit simulation, and efforts to automated "custom" analog physical design.

In the past decade or so, however, we are finally seeing key new analog and mixed signal CAD technology work begin to emerge. Examples of these areas are analog-applicable formal methods, synthesis, and automated analog and mixed-signal physical design, including cell selection, assign, place, route, design rule checking, parasitic extraction, and post-physical-design detailed verification simulation.

3. MOORE'S LAW AND ANALOG DESIGN
A key metric of progress in keeping up with growing chip performance, complexity, density, and size for years has been the well-known Moore's Law. For a recent update of the impact of Moore's Law, see the latest Semiconductor Industry Association 2003 International Technology Roadmap for Semiconductors (ITRS)[1].

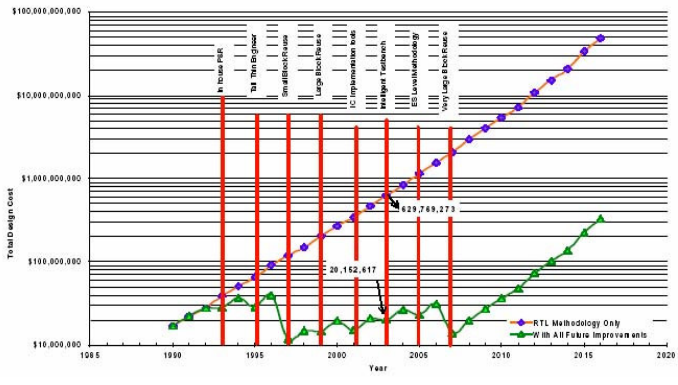

Figure 1 - Digital Design Technology Impact Over Time

Editions of the ITRS have been forecasting and tracking the required design productivity growth needed for the timely and

efficient production of each generation of ongoing reduction of feature size. The current 2003 ITRS summarizes some of the more notable AMS design difficulties as follows:

"DIFFICULT CHALLENGES - ANALOG AND MIXED-SIGNAL: Signal isolation, especially between the digital and analog regions of the chip, is a particular issue for scaled technologies. The difficulty and cost of integrating analog and high-performance digital functions on a chip are expected to increase with scaling. In particular, it will become a major issue to maintain analog performance parameters like mismatch and 1/f noise together with new high-κ gate dielectrics. Finally, the transition to analog supply voltage of less than 1.8V will pose severe challenges to circuit design."

This forecast document has traditionally focused on digital technology, chips and systems; recent editions have begun to also cover analog and mixed signal technologies. The impact of Moore's Law on electronics design is, as chip performance, density and complexity grows, design and designers have to produce denser, more complex, higher performance designs in the same time as in the preceding technology generation.

How does Moore's Law apply to and impact analog and mixed-signal chips, design, and needed productivity?

One aspect of analog design is that we have not seen the same expansion in the number of analog designers as there has been in digital design. This is especially true of those designers and design team who have to able to handle large complex, and high performance analog and mixed signal chips in a timely manner. With regard to needed productivity of analog design flows and methodology, we have seen some of the productivity improvements in AMS tools and integrated flows as we see in digital. However, to sizably improve analog design productivity, we must make sure we improve productivity across almost ALL parts of an analog and Mixed-signal design flow.

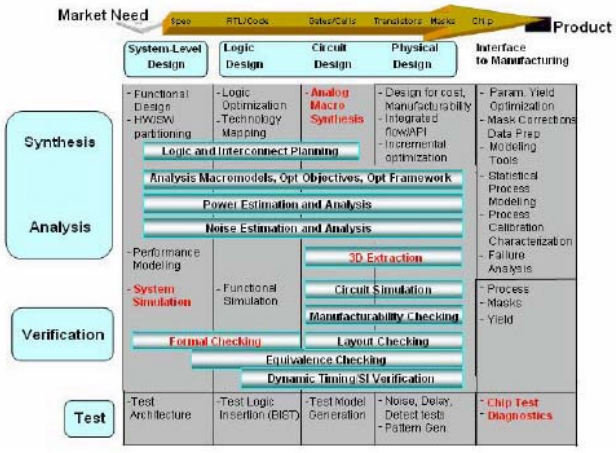

Figure 2 - ITRS 2003 Design Technology Landscape

Moving to analog synthesis and/or automated analogy physical design may provide significant productivity increases, but only for a portion of the overall analog design flow, and the overall design itself. Productivity improvements are needed in other areas as well.

4. ONE ANALOG "GAP": MANUAL DESIGN

Discussions with both analog designers and CAD technologists on analog design often leads to the observation that, after all these years, analog design is pretty much done the same way it was years ago.

A question this paper attempts to resolve here is which design activities exactly has not changed and what productivity improvements can be made to those areas.

It is this author's belief that one key area that continues unchanged is the large amount of detailed 'manual' circuit design work that 'surrounds' (or 'underlies') the core work of a typical analog design.

A large portion of analog and mixed signal design still is done using largely manual methods. In addition to using productivity improvements such emerging synthesis, formal methods, automated cell selection, placement, route, design rule checking, parasitic extraction, detailed verification, etc., much analog design work takes the form of circuit design work done mentally, visually, and analytically using hand calculations and detailed highly-time-consuming analog simulations for detailed point design results.

That is not the worst part. The really bad news is that, every time there is ANY circuit change throughout an analog design, all the manual work has to, at least in part, be repeated and verified again. For instance, after a circuit change, the bias has to be reset or restored, power and supply currents have to be rechecked, substrate parasitic effects have to be again be validated as being manageable. Gain, phase and stability have to be checked and margins verified. Peak voltages and currents have to be reestablished for reliability. Open loop and short circuit gains have to again be verified. Instantaneous and longer-term thermal effects, heat sinking, and packaging have to be rechecked and adjusted. Drive and load Z has to be rechecked. Detailed analog aspects of the product specifications and assertions have to all be accurately calculated, verified to be within range, and adjusted as necessary. And more…

One may see the above as simply a core part of a normal analog system and circuit design methodology. Sometimes that's true. However, sometimes all the above are merely background activities and effort to keep the main analog product design set within the circuit design bounds needed to meet the product requirements.

5. LESSONS FROM DIGITAL'S HISTORY

This author was fortunate to have participated in the early days of both analog and digital design, as both a designer and lead CAD developer. In considering how to might tackle areas of analog design not yet being supported with high productivity, the parallel history of the development of digital design, CAD and productivity has led to a realization that a key part of the digital history was the innovation of several key but simple digital CAD tools that greatly improved productivity.

For this writer, the development of one tool in particular illuminated a key digital design technology improvement, and led in part to the proposals within this paper.

In the 60's and 70's, digital designers had to develop large numbers of detailed timing diagrams to establish both the overall system and local timing, and the correctness of the desxign of control logic and registering. In 1971, this author developed the first hierarchical worst-case min/max timing analyzer for use in the design of large-scale computers. This tool ran directly from the hierarchical design definition in a high-performance CAD database, using accurate detailed circuit information, and adding detailed worst-case timing information to both the design definition and schematics block diagrams.

Timing diagrams, when required, were automatically generated or updated. This tool then allowed large digital design teams to always have the latest detailed timing information without any effort on their part.

The lesson from the history of digital CAD therefore that led to this present work was this: A simple analytic tool was used to recursively do massive amount of accurate circuit timing analysis without the designer having to take the time to do large amounts of repetitive manual calculations and/or simulations.

6. IDENTIFYING AREAS OF NEED

Several initially rhetorical questions then come to mind. These questions in turn led to the specific analog tool proposed in this paper.

- What are the parts of a particular analog design process flow that take away or limit design productivity and capacity from the analog designers? For which of those process steps do current analog CAD tools and flows not support, or support very well?
- Especially, which of those process steps are essentially fully manual, and/or, at best, are only manual-like use of individual simulation-based analysis activities.
- Finally, which of those process steps have to be repetitively done for every design change, and as the design is being 'retuned' to meet the product specifications and requirements.

There are probably several areas of the overall analog design flow one can focus on that would meet the requirements underlying the above questions.

However, for this work, we propose to limit the scope of our focus to tools that can improve the productivity of normally manual simulation-based design analysis calculations done within detailed analog design flow steps.

7. PROPOSED ANALOG TOOLS

The rationale for proposing the following tools is, of course, to reduce and eliminate the 'manual' effort of designers working on an ongoing analog and mixed-signal design process. We especially focus on those repetitive design analysis and simulation activities that are done as the design is iterated in support of the main design effort.

In other words, we seek to define straight forward, "Static Timing Analysis"-like tools for the analysis and circuit design work that surrounds and underlies an analog design..

For example, this would include those tools needed to keep a design properly powered, biased, and with proper phase and gain margins, as the design is iterated towards meeting its design specifications and requirements.

In this paper, we do not propose any completely new analog tool functionality.

Instead, we propose **recasting** existing tools and related analysis capabilities in such a way that their use requires little or no designer effort, setup, or post-execution reformatting. Where possible, we propose recasting them so that, as often as possible, they will do their work largely on their own, with the designer typically only having to either verify that they ran OK, or to only deal directly with those few results that actually require the designer's direct involvement or intervention.

- This approach is exactly analogous to that used with well-implemented Static Timing Analysis (STA) tools. While the STA does an exhaustive timing analysis, in good STA tools, the designer only sees the results of those timing arcs that do not meet proper timing design criteria of e.g. register-to-register design requirements, setup and hold, and initialization.

Long range, a goal later for this work might include bringing such tools into a fully synthesis-based automated flow.

7.1 Necessary CAD Environment

The tools described in the following subsections will need to be created or setup so that they can be used within a normal analog design environment, whether integrated into a 'cockpit' environment or in a typical schematic-edit-and-simulate more open analog design environment.

7.1.1 Automatic Re-execution On Incremental Change

A key attribute of the environment holding these tools is, whenever any aspect of the design changes, the appropriate tools must ***automatically*** and *incrementally* reexecute.

7.1.2 Automatically Available Results

Results must be immediately available as an integrated part of overall design information. The UI and GUI windowing will be needed to show which results changed, how much they changed, and in which direction.

7.1.3 Assertions

All results should be available for use within assertion statements about the design. As assertion-based methodology for analog becomes better understood and better integrated into the design description, such results should begin to be automatically processed as part of moving to 'live', 'self-designing' design definitions, specifications, and requirements.

7.1.4 Designer Controllable

The designer must be able to prescribe circuit conditions and analysis results that should not change or change within a range.

7.1.5 Parameterized Circuit Design

To provide the variational information needed by some of the following proposed tools, circuit elements and constraints will need to include element variational information, including value tolerances, correlation, statistical distribution shape, and reliability information.

Note: The following descriptions of proposed needed analog tools assumes the reader has both an analog circuit design and analog CAD development background.

7.2 Circuitry Startup Initialization

Proposed tool: Provide automatic means for properly bringing an analog circuit design up to full power and biasing. For each incremental design iteration, this means attempting to bring the circuit back up to the same circuit conditions, states, and modes as before the change.

7.3 Circuit Biasing

Proposed tool: Provide automatic means to keep a circuit biased within range while making incremental circuit element changes per constraints (values, tolerances and correlation) of the changeable elements.

- For a design iteration, this means bringing the target analog circuit design back up to the same circuit conditions, states, and modes as before you made the change. The term, 'states', here refers to both 'states' in a logic latch sense, as well as having each device returned again to the same biasing conditions and modes, e.g., for MOS devices, having drain, gate, and source voltages and current values and relationships for a device forward biased in normal saturation, etc.

7.4 Power Dissipation

Proposed tool: Provide automatic means to analyze all aspects of power dissipation for the whole or any aspect of a circuit. The results should be able to show which devices and circuit conditions and modes have changed to unusual or unwanted circuit power conditions. Those types of results should be reported directly to the designer, especially emphasizing those areas now requiring the designer's immediate design attention.

7.5 Analysis of Energy

Proposed tool: Provide automatic calculation and analysis of instantaneous, RMS, average, and peak values of coulombs, power, including electrical, magnetic, thermal (temperature, calories), and other forms of energy that may be needed for a given analog design. This especially applies to switching, power, and other circuits with nonlinear states, conditions, or modes.

7.6 Zin, Zout, Voc, Isc

Proposed tool: Provide automatic analysis of input and output impedances, and open and short circuit drive and loading information. The reporting of results should emphasize that input and output drive and loading information that changed in sign or past some preset limit values.

7.7 All Gains

Proposed tool: Provide calculation and analysis of stage, cell, block, loop, and device gains. This capability should include means for doing all the usual circuit theoretic gains (A, B, C, D, etc.) As needed, this capability should be instrumented using the following virtual loop opening and constraining capabilities.

7.8 Driven & Driving Circuit Conditions

Proposed tool: Provide calculation and analysis of power up, biasing, DC, transient, AC, and other circuit conditions of both the driving and driven systems, blocks, cells, devices, or elements of a circuit. This requirement focuses on providing circuit interaction information at a hierarchical block level, across the circuit design hierarchy.

7.9 "Virtual" Loop Opening

Proposed tool: Provide means to automatically instrument an existing analog or mixed-signal circuit design to open any arbitrary circuit loop and performing various calculations and analyses on those loops without explicitly changing the target circuit design.

7.10 "Virtual" Circuit Constraining

Proposed tool: Provide means to apply of both assertions and circuit and element constraints on a circuit design without having to necessarily make specific changes in the circuit hierarchical schematic block diagram and HDL description to 'instrument' the assertions and constraints into the circuit definition and specification.

7.11 Analysis of Circuit Linearity

Proposed tool: Provide means for accurate calculation and analysis of circuit linearity based on use of accurately modeled circuit elements, packaging, power, grounding, and substrate effects. Updated results of linearity should be reported as incremental design changes are made, especially emphasizing those circuit linearties that significantly changed or no longer met preset limits.

7.12 Analysis of Circuit Nonlinearity and Distortion

Proposed tool: Provide accurate calculation and analysis of circuit nonlinearities including harmonic and other measurements of distortion, based on use of accurately modeled circuit elements, packaging, power, grounding, and substrate effects. Updated results of nonlinearity should be reported as incremental design changes are made, especially emphasizing those circuit nonlinearities that are significantly changed or no longer meet preset limits.

7.13 Analysis of Noise

Proposed tool: Provide calculation and analysis of noise generated by physical circuit elements and routing, including thermal, accurate circuit element models, substrate, packaging, power, and ground busing. Updated results of noise should be reported, especially emphasizing significantly changed amounts or noise, or those values which no longer meet preset limits.

7.14 Analysis of Coupling

Proposed tool: Provide calculation and analysis of coupling between accurately modeled signals, circuit element, substrate, packaging, power, and ground busing. Again, results should emphasize significant changes or those results that no longer meet preset limits.

7.15 All Sensitivities

Proposed tool: Provide means to do calculations and analyses of all rates of change from any circuit element, parameter, or aspect to any other, including across the circuit design hierarchy.

- Sensitivities are of themselves an extremely important 'missing' capability needed for improving the productivity of analog and mixed signal hierarchical circuit design. In spite of a number of analog CAD sensitivity having been developed through the years (for example, see [2], [3], [4], and [5]), this capability today is available from just a small number of analog tools.

With sensitivity information available for literally any aspect, and combinations of aspects of an analog design, a designer knows immediately

- Which way to change the design
- What to do to reduce design and manufacturing process variations.
- Which circuit elements, element values and tolerances, and manufacturing process variations have a critical impact on meeting the design's specifications, which the designer was not aware.
- Without sensitivities, the designer is left to searching the design and manufacturing process variation space on his/her own.
- A powerful analog design process tactic seldom considered is to use sensitivities as a driver for exploring the design and tolerance space using Monte Carlo methods [6].
- Sensitivities are also a very necessary technology for doing worst-case variational and manufacturing process range design. More on that issue in the following section.

7.16 All Worst Case

Proposed tool: Provide means to calculation and analysis of all minimum and maximum extremes of an analog / mixed-signal hierarchical circuit design. Such capability should means to use of all the usual standard variational distribution approaches, including normal, bi-normal, uniform, and measured custom statistics [6].

Once a set of worst-case results vs. circuit and process variation ranges and correlations have been identified, worst-case results should be simulated and calculated (using incremental means as may be available) and presented to the designer, emphasizing especially those results that changed significantly, or no longer are within preset limits.

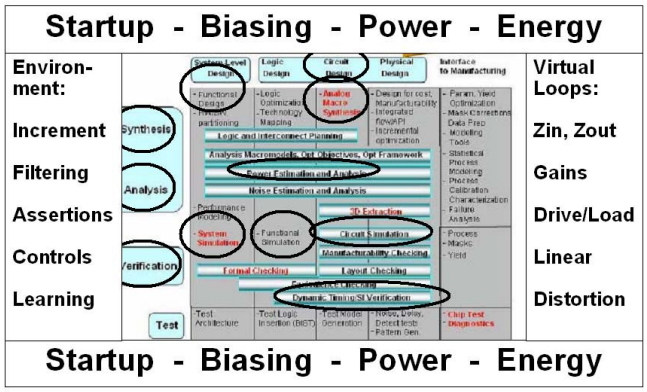

Figure 3 - Proposed Analog Design Landscape

8. CONCLUSIONS

A group of analog tools has been proposed that are needed to help resolve areas in an analog design flow needing greater productivity. See Figure 3.

The realization of the particular gap, approach and tools covered within this paper arose from first trying to look at how to adapt the paradigm of a digital hierarchical static worst-case timing analyzer tool for use on analog design. This then led to considering the role STA had on freeing up both the time and mental capacity of those designers.

In particular, the identified tools are intended to be usable within a normal analog design environment, whether integrated into a 'cockpit' environment or in a typical open schematic-edit-and-simulate environment.

None of the proposed tools require new or unusual CAD technology or instrumentation. Instead, the whole purpose for them is to eliminate the need for the designer to take the time to separately reanalyze the results they produce. Many of them require adding a simple layer to an existing CAD environment to automatically provide an analysis or simulation result whenever the circuit changes such that the result would change.

All tool results should be available through both cockpit style design instrumentation and through the visual design viewing means of schematics and block diagrams.

All results should emphasize what has significantly changed or that fails to meet preset limits.

The bottom line of providing such instrumented tools is to have zero or minimal efforts to produce just those results that are needed to best aid the designer in most quickly meeting the target design requirements.

9. ACKNOWLEDGMENTS

This paper is, in part, the result of years of conversations with analog designers and managers, CAD system and tool technologists, many thought-provoking editorials on EDA/CAD, stints at Honeywell/Bull Computer Systems, MCC, and SEMATECH, working with SI2, and discussions at numerous DAC, ICCAD, and CANDE meetings, specifically on coming (digital) design productivity gaps. In particular, this included conversation (and editorials) with Steve Sapiro, Paul Weil, Rick Bushroe, John Hanne, Steve Shulz, Deo Singh, Don Cottrell, Gary Smith, Richard Goering, and others.

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