# Missing Analog Tools – A Proposal

Steve Grout
CAD Consultant

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# A BRIEF HISTORY OF ANALOG DESIGN

- **Analog design for years has focused on circuit design and design innovation**
- **Main analog CAD tool efforts has been on high performance analog HDL / circuit simulation, and efforts to automated "custom" analog physical design.**
- **We are finally seeing new analog and mixed signal CAD beginning to emerge:**
  - Analog-applicable formal methods
  - Synthesis
  - Automated analog and mixed-signal physical design.
- **Still Includes MUCH Intense MANUAL detailed circuit design work by analog designers**

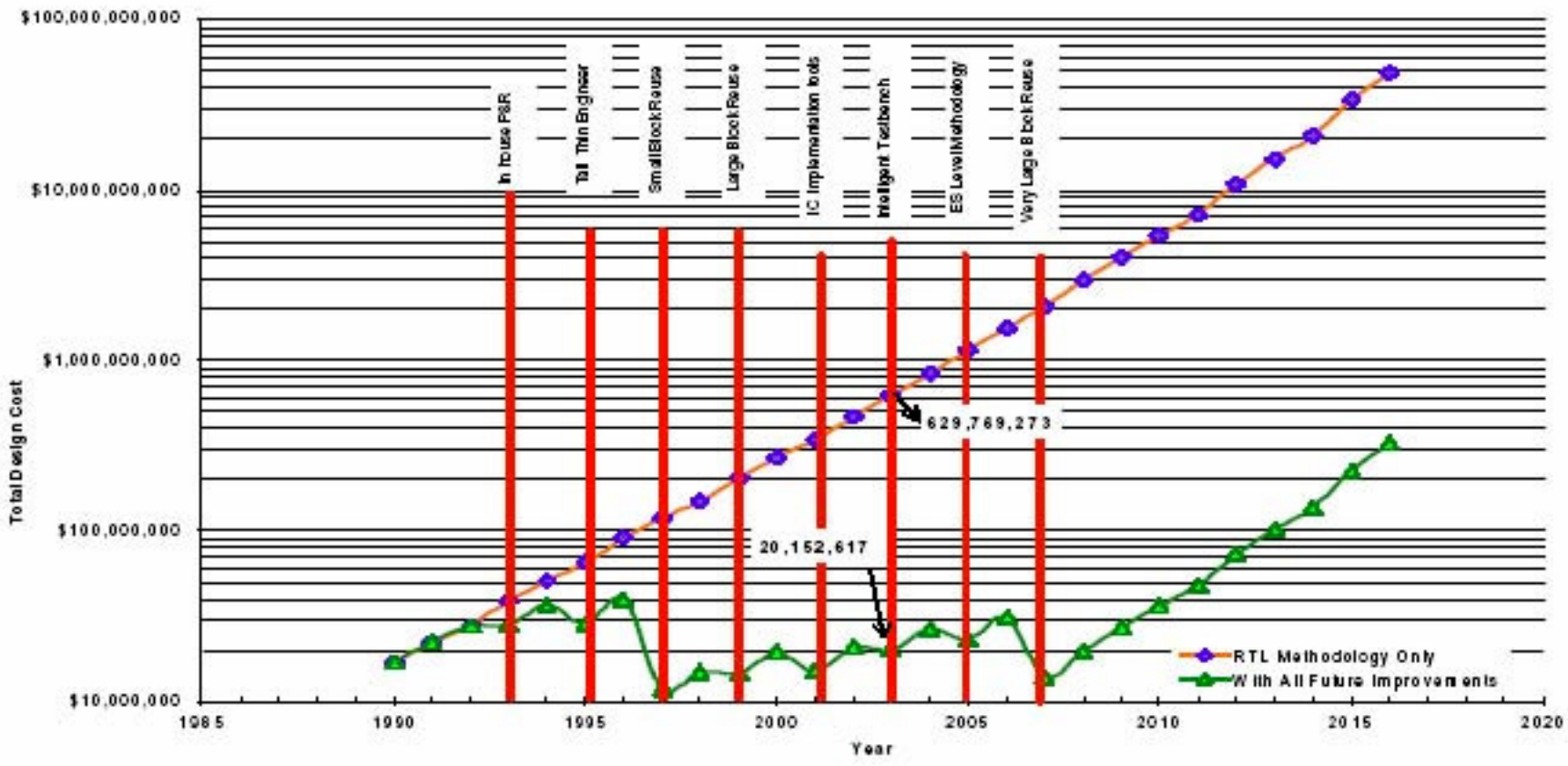
# ANALOG PRODUCTIVITY ISSUES:

- **Many Industry Analysts now Stress that Analog Design Productivity needs to GROW in order to support the fast growing need for Analog SOC/DSP Chips!**

- **What Analog Design Productivity Issues can be improved following Approaches used for ITRS Digital SOC Issues?**

- **But What will it take to *GREATLY INCREASE* Analog Design Productivity?**

# Digital Design Technology Impact Over Time




(Source: ITRS 2003 Chapter on Design Technology)

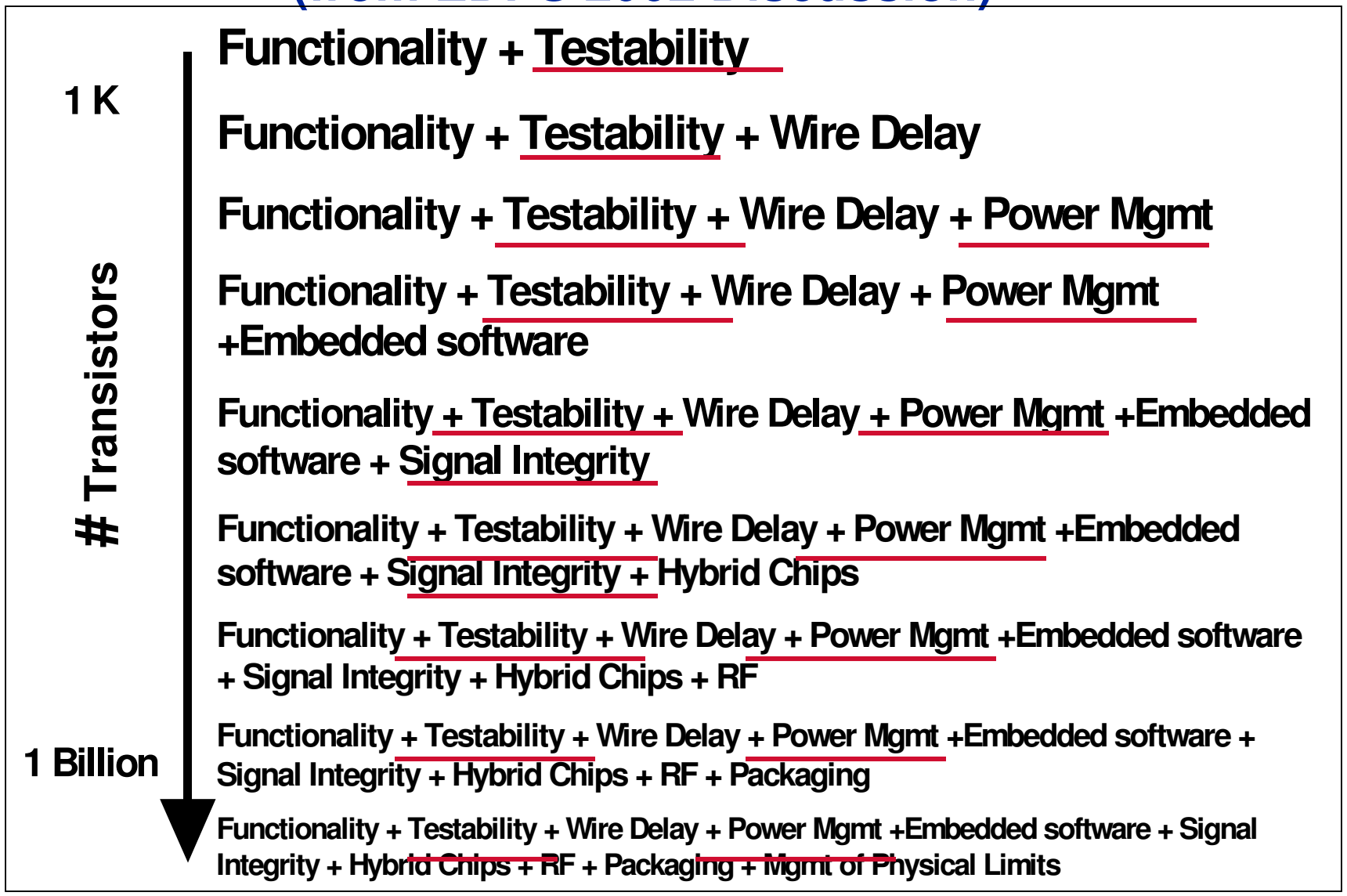
# MOORE'S LAW AND ANALOG DESIGN

- **Key metric of growing chip performance, complexity, density, and size**
  - See SIA 2003 International Technology Roadmap for Semiconductors (ITRS)[1].
- **ITRS: AMS design difficulties:**
  - Signal Isolation
  - Integrating High Performance Digital & Analog on new processes
  - Lower Supply Voltages.
  - Needed Increase in AMS Productivity
- **How does Moore's Law apply to and impact analog and mixed-signal chips, design, and needed productivity?**

# MOORE'S LAW AND ANALOG DESIGN, cont..

- **Analog Designs and Analog/AMS/Digital SOC Design Numbers, Size, Complexity, Density, etc. Seem to be Growing Similar to Digital / SOC Designs.**
- **Some (at least Limited) Productivity improvements Are Needed in AMS tools and integrated flows**
  - Similar to Digital Improvements in some Areas.
- **Issue: Limited growth in Number of Analog Designers vs Need.**
  - Currently Believed to be FLAT!
- **Must Improve Productivity across almost ALL parts of an analog and Mixed-signal design flow.**

# Analog Design vs Increasing Design Complexity? (from EDPS 2002 Discussion)




Note: RED - Indicates Areas probably not being Effectively Addressed yet.

# Analog Design vs Digital EDA Capabilities?

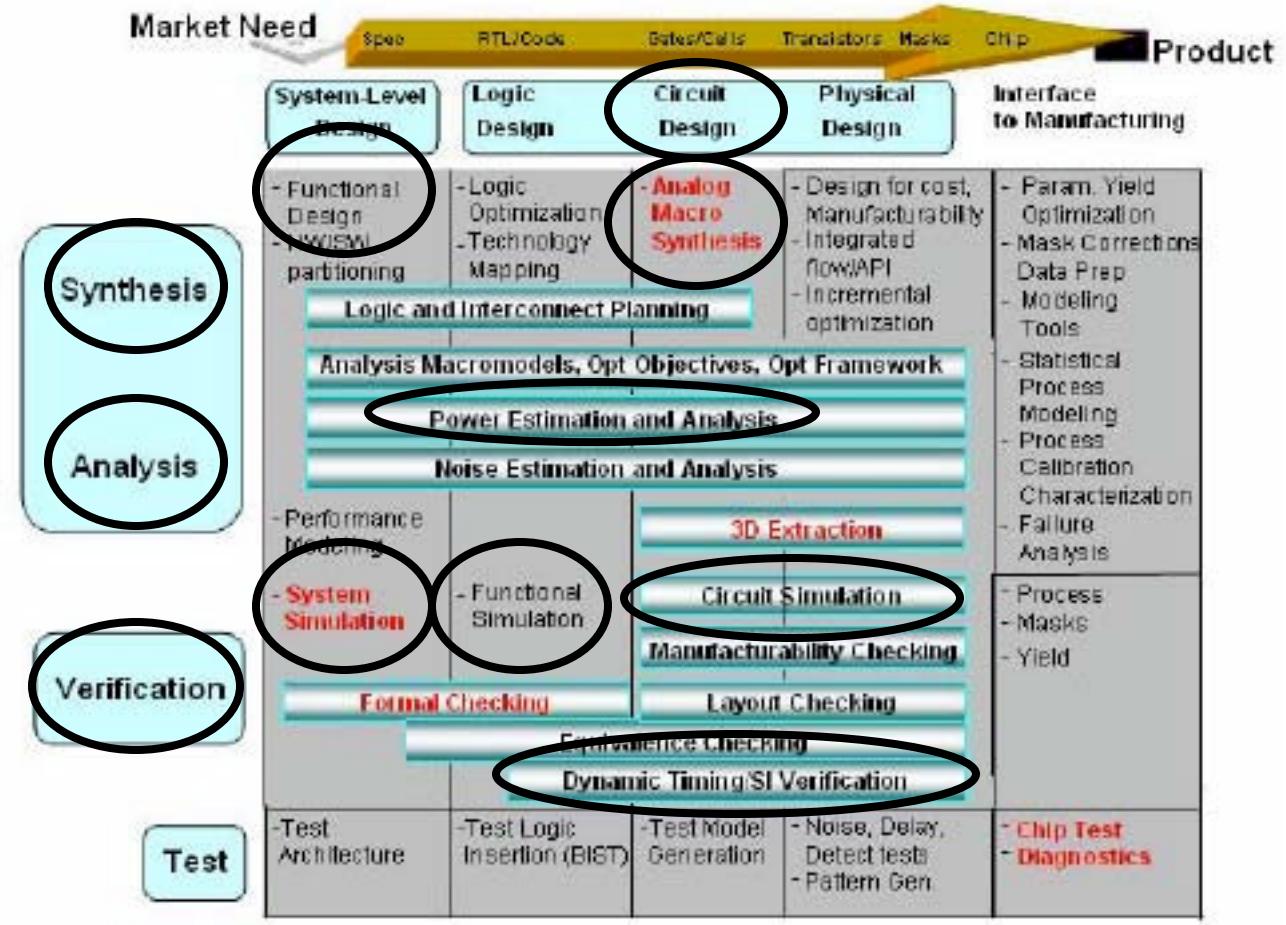

(from EDPS 2002 Discussion)

| | System Design | Logic Design | Circuit Design | Physical Design | Manufacturing Interface |
|---|---|---|---|---|---|
| **Design** | - Functional Design<br>- HW/SW Partitioning | - Logic Optimization<br>- Technology Mapping | - Analog Macro Design | - Design for Manufacturing<br>- Integrated flow/API<br>- Incremental optimization | - Param. Yield Optimization<br>- Mask Corrections<br>- Modeling tools |
| | Logic and Interconnect Planning | | | | |
| **Analysis** | - Performance Modeling<br>- Power Estimation | - Power Estimation<br>- | 3D Extraction<br>Power, Noise<br>Signal Integrity | | - Statistical Process Modeling<br>- Failure Analysis |
| **Verification** | - System Simulation | Functional Simulation | Circuit Simulation | | - Process<br>- Masks<br>- Yield |
| | Formal Checking | | Layout Checking | | |
| | | | Equivalence Checking | | |
| | | Dynamic Timing/SI Verification | | | |
| **Test** | - Test Architecture | - Test Logic Insertion (BIST) | Test Model Generation | - Noise, Delay, Defect Tests<br>- Pattern Gen. | - Chip Test<br>- Diagnostics |

**Note: RED - Indicates Areas probably not being Effectively Addressed yet.**

# ITRS 2003 Design Technology Landscape

## Annotated for AMS CAD Capability & Improvements




**Note: Only a few blocks concern Analog-specific CAD Issues.**

# TAKING A LESSON FROM DIGITAL'S HISTORY - Static Timing Analysis

- System-down-to-Cell Timing used be done Manually using TIMING DIAGRAMMING
- 1971* - Static Timing Analysis == Exhaustive Min-Max Worst-Case Across the Design Hierarchy- From System down to Cell/Device
- Extremely Fast Simulation/Analysis Produced Up-to-Date Accurate Timing Data after each Incremental Design Change
- Designers Only Had to Deal with BAD Timing Arcs - Fixing Worst ones First.

[ * = J. S. Grout Implementation at Honeywell Large Systems. ]

# ANALYSIS OF ANALOG NEEDS

- **KEY questions that led to the specific APPROACH for Analog Tools proposed in this paper.**
  - What are the parts of a particular analog design process flow that take away from or limit Analog Designers design productivity and capacity?
  - Which Process Steps do current analog CAD tools and flows not support, or support very well?
  - Especially, which of those process steps are essentially fully MANUAL, and/or, at best, are manual-like use of individual simulation-based analysis activities.
  - Finally, which of those process steps have to be REPETITIVELY done for every design change, and as the design is being 'retuned', to meet the product specifications and requirements.

# ANALOG TOOL STRATEGY - Two Prong Approach:

- **Replace MANUAL Steps with Automatic Steps**
- **As Possible Redo Automatic Steps Similar to Digital's STA Static Timing Analysis**

# Requirements: Supporting Analog CAD Environment:

- **7.1.1 Automatic Re-execution On Incremental Change**
- **7.1.2 Automatically Available Focused Filtered Results**
  - Immediately Answers/Confirms Designer's Questions about the Design
  - Immediately Shows what's OK, What's BAD, What's Unusual.
- **7.1.3 Assertions - Constraints**
  - All Assertions, Variables, and Values available to the Design Database/HDLs
- **7.1.4 Designer Controllable**
  - Scripts, Dialogue Boxes for Settings
  - Able to 'Import' Settings from Execution Logs, Adapt, Learn
- **7.1.5 Parameterized Circuit Design**
  - Lead to Designer's Tuned, Smart, Self-Learning Design Manager

# PROPOSED ANALOG TOOLS -

- **Circuitry Startup Initialization**
  - Bring to Full Power, Voltage, Biasing, including with each Incremental change.
- **Circuit Biasing**
  - Each design iteration, return to same biasing, modes, states.
  - (Help) Keep circuit conditions Unchanged.
- **Power Dissipation**
  - Show which devices/cells power are unchanged, or have moved to Unusual or Unwanted power conditions.
- **Analysis of Energy**
  - Show what circuit Energies have changed or moved to Unusual conditions.  Support “all” forms of Energy.

# PROPOSED ANALOG TOOLS -

- **"Virtual" Loop Opening and Circuit Constraining**
  - Needed to "Auto Instrument" the following Capabilities so they can be measured without explicitly changing the Design.
- **Driven & Driving Circuit Conditions**
- **Zin, Zout, Voc, Isc**
- **All Gains**
- **Analysis of Circuit Linearity**
- **Analysis of Circuit Nonlinearity and Distortion**
  - **Measure Design Conditions with Each Incremental Change.**
  - **Filter for Unusual or Unwanted Change, or Changes Out-of-Range**

# PROPOSED ANALOG TOOLS -

- **Analysis of Noise**
  - Any Form of Noise, including Internal Device noise, and unwanted Signals in a device's environment.
  - Includes verifying noise within range, unusual or unwanted values of noise.
- **Analysis of Coupling**
  - Any form of Coupling - Includes Packaging, Substrate, Isolation, Power, Ground, EMF, Particle, etc.
  - Filter for coupling within range, unusual, or unwanted values of coupling.

# PROPOSED SENSITIVITY-BASED ANALOG TOOLS
## Case for "Sensitivities" = "Active" Design Info

- **Which way to change the design?**
- **What to do to reduce design and manufacturing process variations?**
    - Use to DE-SENSITIZE the design.
- **Which circuit elements, element values and tolerances, and manufacturing process variations have a critical impact on meeting the design's specifications?**
    - Especially in ways the designer may not be aware.
- **Without sensitivities, the designer is left to searching the design / manufacturing process variation space on his own.**
- **Sensitivities are necessary for doing worst-case variational and manufacturing process range design.**
    - More on that issue in the following section?
- **Use sensitivities as a Smart Way to Explore the design and tolerance space using Monte Carlo methods [6].**

# PROPOSED ANALOG TOOLS -

- **All Sensitivities**
  - All Rates of Change from any design element, parameter, or Aspect, to any other, including across the Design Hierarchy.
  - Filtering for Sign & Values within Range, with Unwanted, or Unusual sign & values.
  - Need to include Manufacturing Process Sensitivities!
- **All Worst Case**
  - Calculate Min/Max Extremes of AMS hierarchical Circuit Design.
  - Use all usual/standard variational distribution approaches (normal, uniform, measured, etc.)
  - Filtered for values within range, unusual or unwanted.
  - Need to include Worst Case per Manufacturing Process Variations.

# Proposed Analog Design Landscape:

**Startup - Biasing - Power - Energy**

**Environ-ment:**

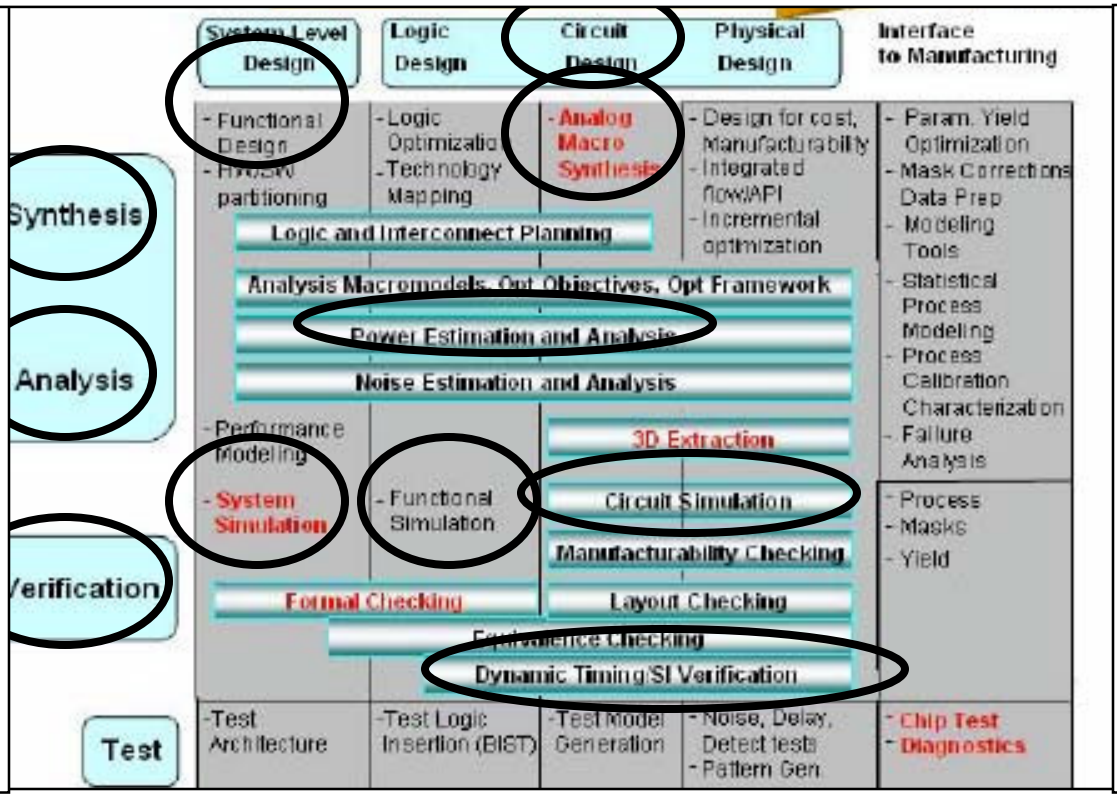
**Increment**

**Filtering**

**Assertions**

**Controls**

**Learning**




**Virtual Loops:**

**Zin, Zout**

**Gains**

**Drive/Load**

**Linear**

**Distortion**

**Startup - Biasing - Power - Energy**

# CONCLUSIONS

- **A group of analog tools has been proposed that are needed to help resolve areas in an analog design flow needing greater productivity.**
- **Main Strategy - Move from Manual Steps to Fast Focused Incremental Results to Directly Support Main Design Efforts, Automated or Not.**
- **Approach arose from adapting the paradigm of a digital hierarchical static worst-case timing analyzer tool for use on analog design tools.**
- **Main Goal - Free up the EFFORT, TIME, and MENTAL capacity of Analog designers.**