Applications of Interoperable Databases and Data Models in Production Flows at LSI Logic

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LSI LOGIC

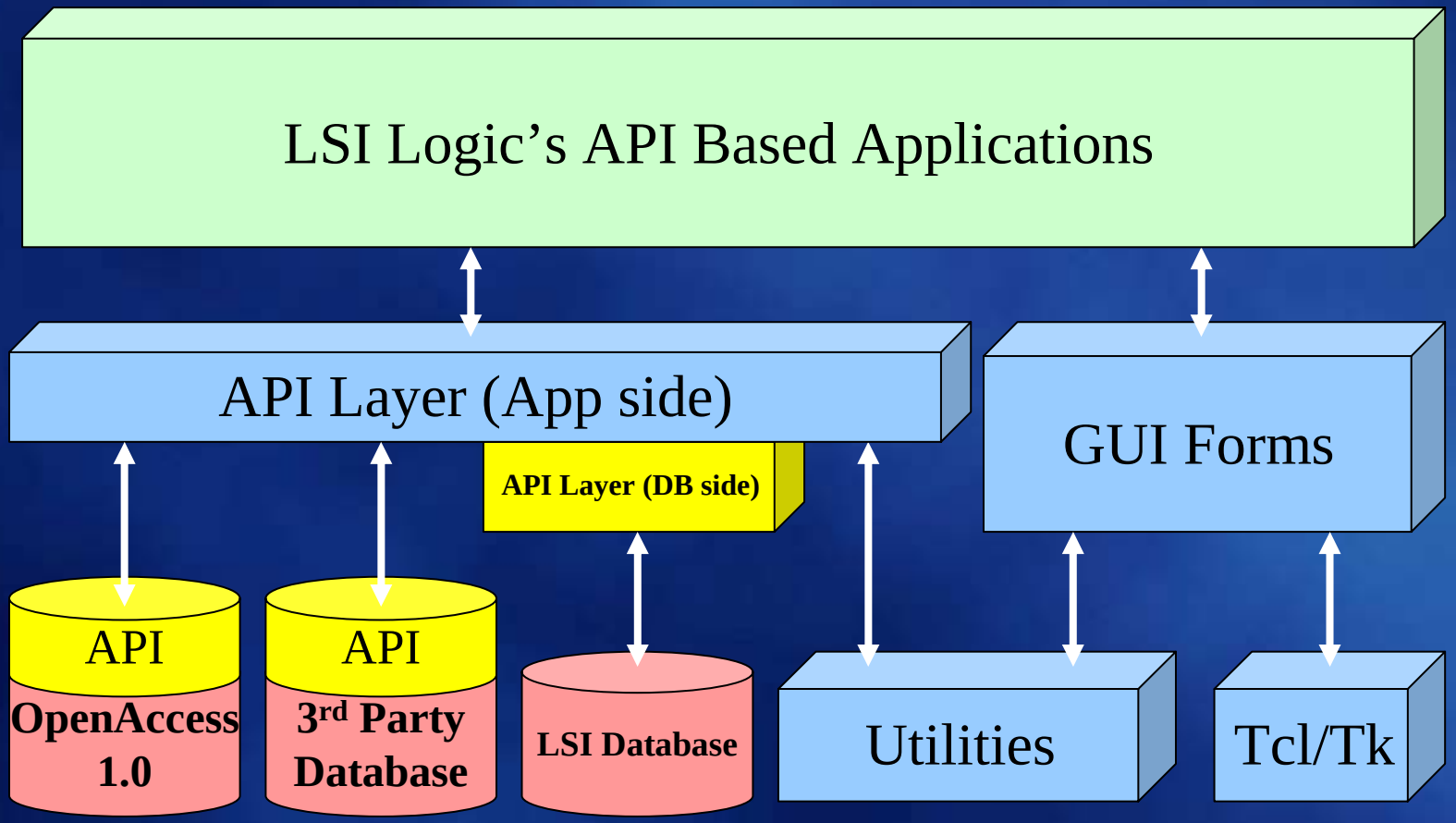
Agenda

- Background
- RapidChip™ with the RapidWorx™ design kit
- Bond Application
- Summary

Background

- LSI Logic maintains several internal databases for design kits
  - Propriety in nature and specific for feature needs
  - Maintaining propriety databases requires an investment for development and support
- LSI Logic uses commercial databases
  - Provide value add applications on commercial offerings
  - No one vendor supplies the necessary features required
- LSI Logic began investigation of OpenAccess initiative and technology late 2001
  - Initially ported a GDSII application on OA1.0
  - Determined viability of OpenAccess and proceeded to develop future RapidWorx™ design kit on OpenAccess for RapidChip™ product

Initial Investigation



GDSII Benchmarking

- LSI created a GDSII to OA converter
  - Quickest way to populate testcases
  - Centralizes OA database for translators
    - GDSII -> OA, OA -> GDSII
    - DEF -> OA, OA -> DEF
    - Etc.
- Sample data sets show good results
  - 3x file size reduction
  - Program memory usage reasonable
  - Program runtimes reasonable

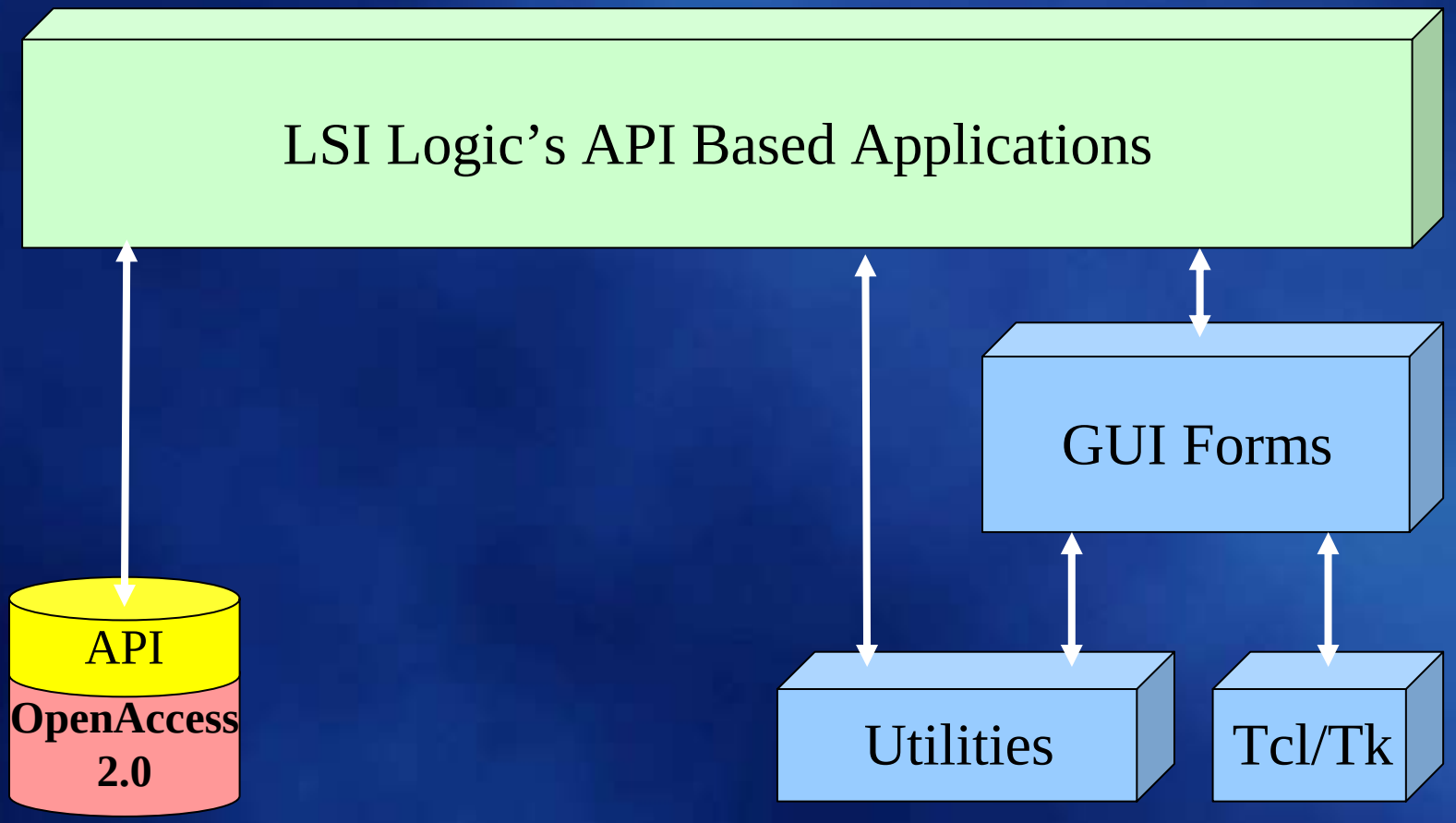
GDSII Benchmarking

	Number of Records	Read Time (ms)	Elapesed time (ms)	GDS Size (KB)	OA Size (KB)	Ratio
Design 1	464078	11456	16944	3684	1434	**2.6**
Design 2	5177017	70101	76760	42690	14215	**3.0**
Design 3	5774428	77201	85933	49296	16087	**3.1**
Design 4	6758148	75459	82899	54408	18263	**3.0**
Design 5	7078607	87235	94806	57104	19222	**3.0**
Design 6	7186254	88538	96038	58050	19405	**3.0**
Design 7	8405195	105321	111430	67688	22593	**3.0**

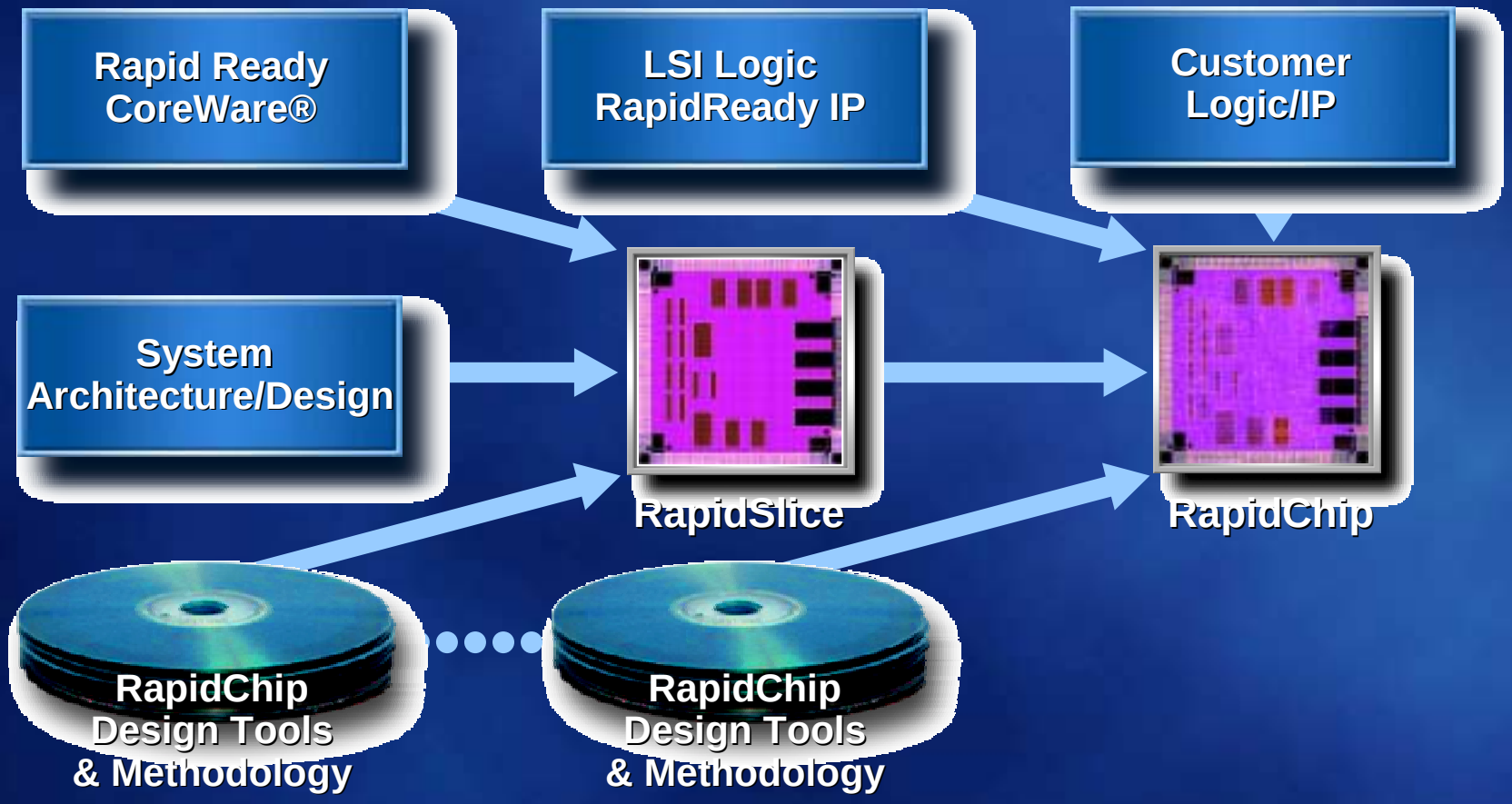
Run on

- Pentium III 700MHz processor
- 256MBytes of memory
- Win2000 operation system

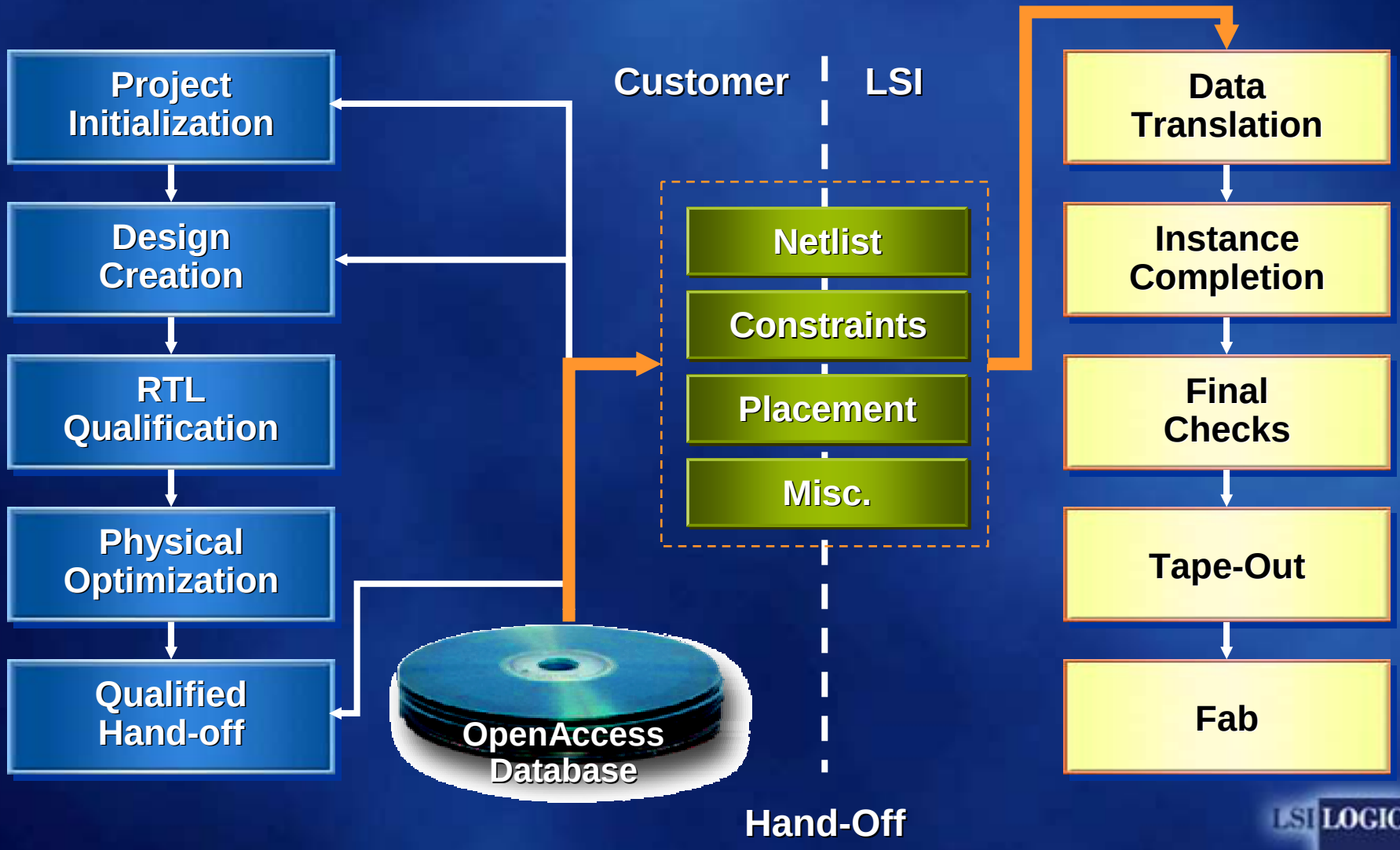
Natively Using OpenAccess



RapidChip™ Product Architecture



RapidWorx™ High Level Design Flow View

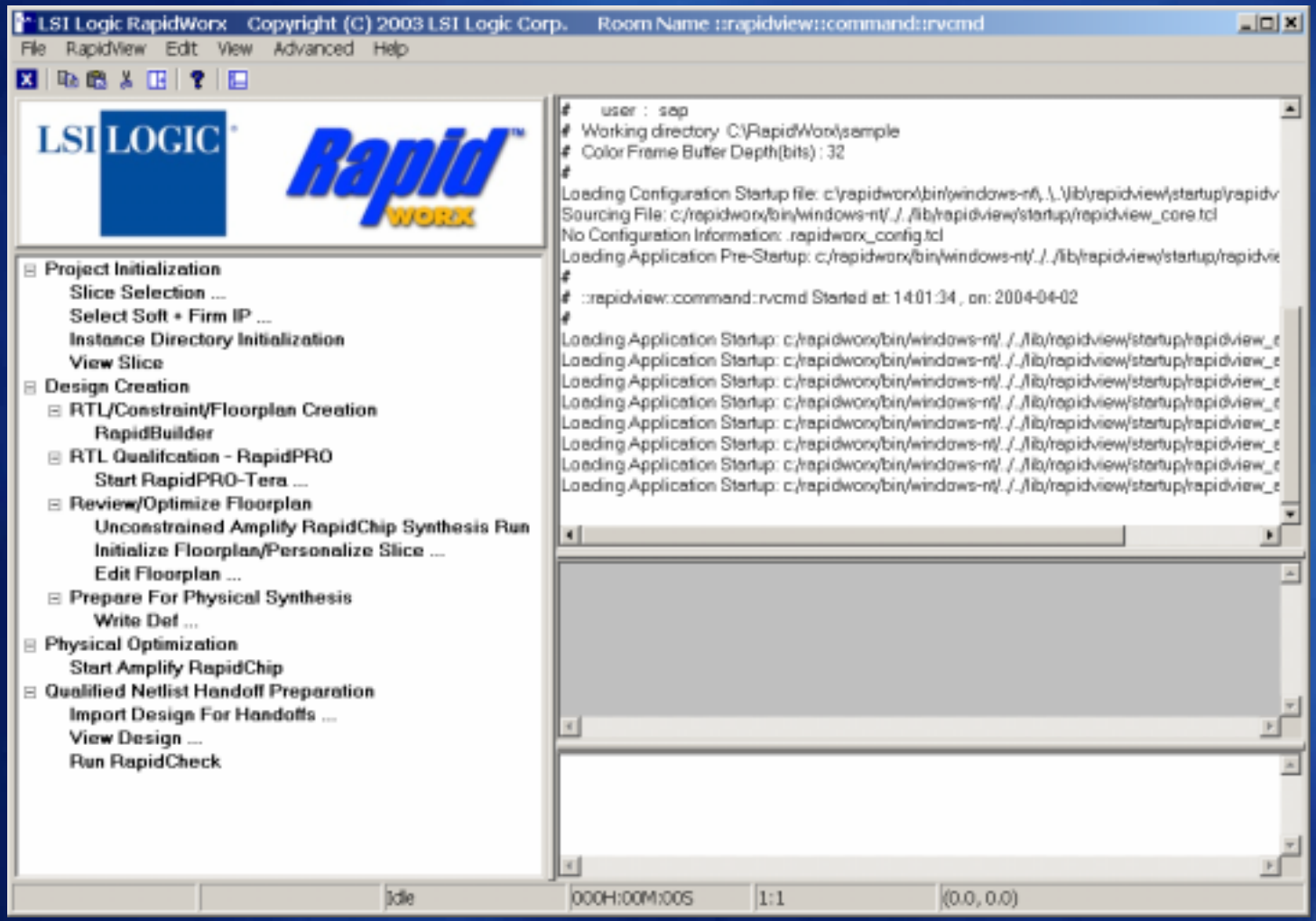


RapidChip™ Design Steps

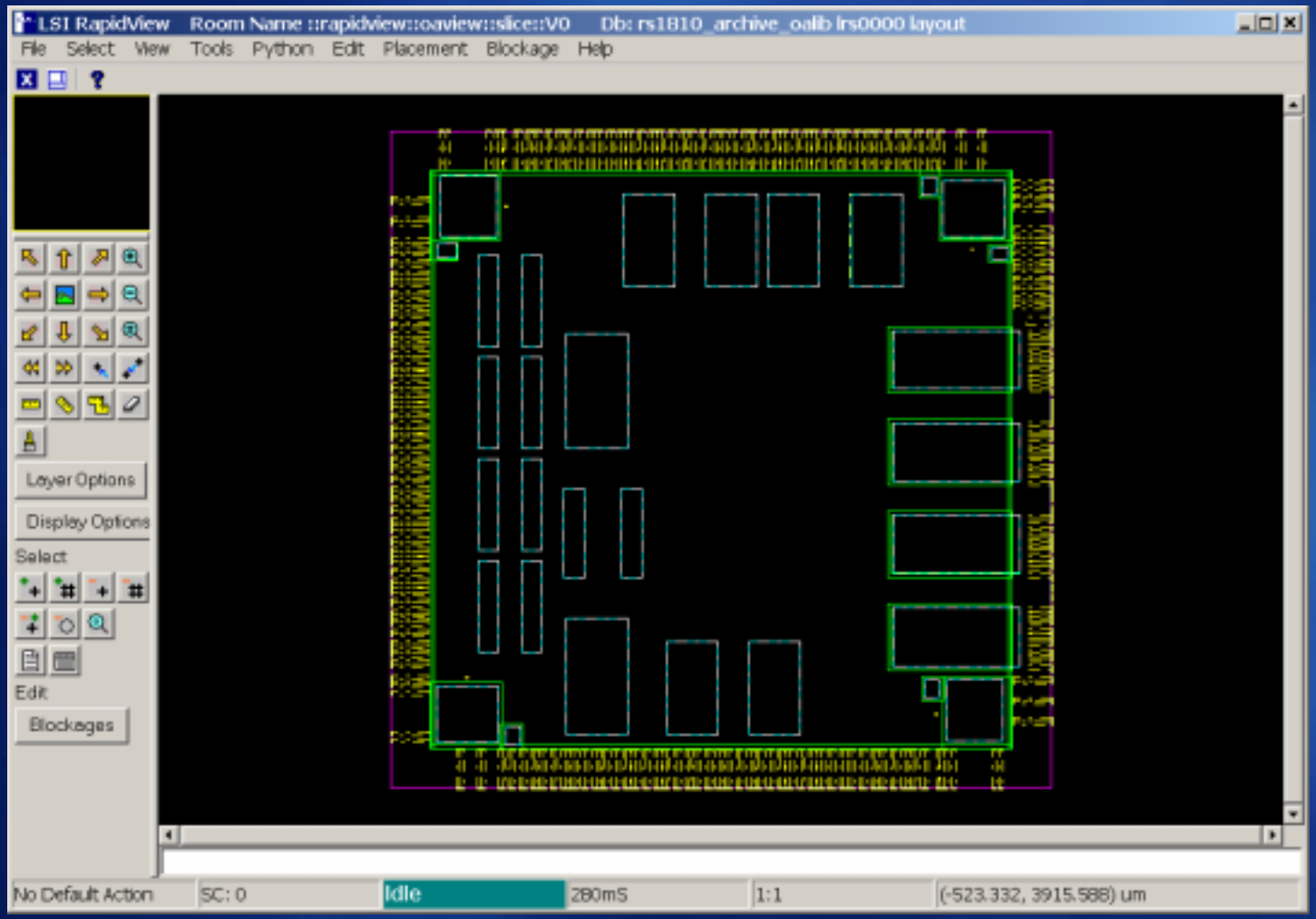
1. **Project Initialization**
   - Slice Selection
   - Select Soft + Firm IP
   - Instance Initialization
   - **View Slice**
2. **Design Creation**
   - RTL/Constraint/Floorplan Creation
     - **RapidBuilder**
   - Review/Optimization Floorplan
     - Unconstrained Synthesis
     - **Initialize Floorplan/Personalize Slice**
     - **Edit Floorplan**
   - Prepare for Physical Synthesis
     - **Write DEF**
3. **RTL Qualification**
   - RapidPRO
4. **Physical Optimization**
   - Physical Synthesis
5. **Qualified Netlist Handoff**
   - **Import Design for Handoffs**
   - **View Design**
   - **RapidCheck**

Current OA base tools
Future OA base tools

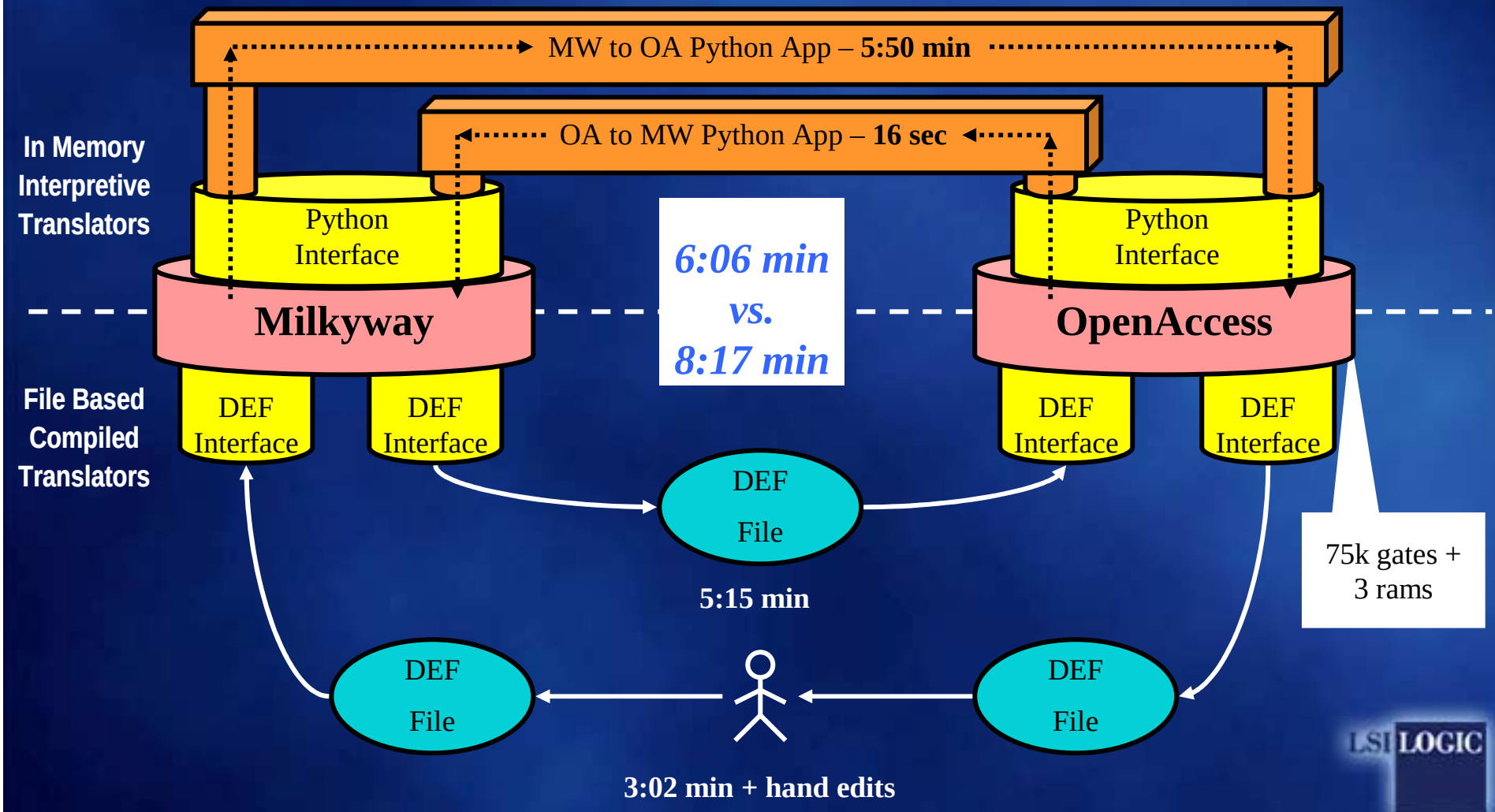
Design Cockpit based on OpenAccess



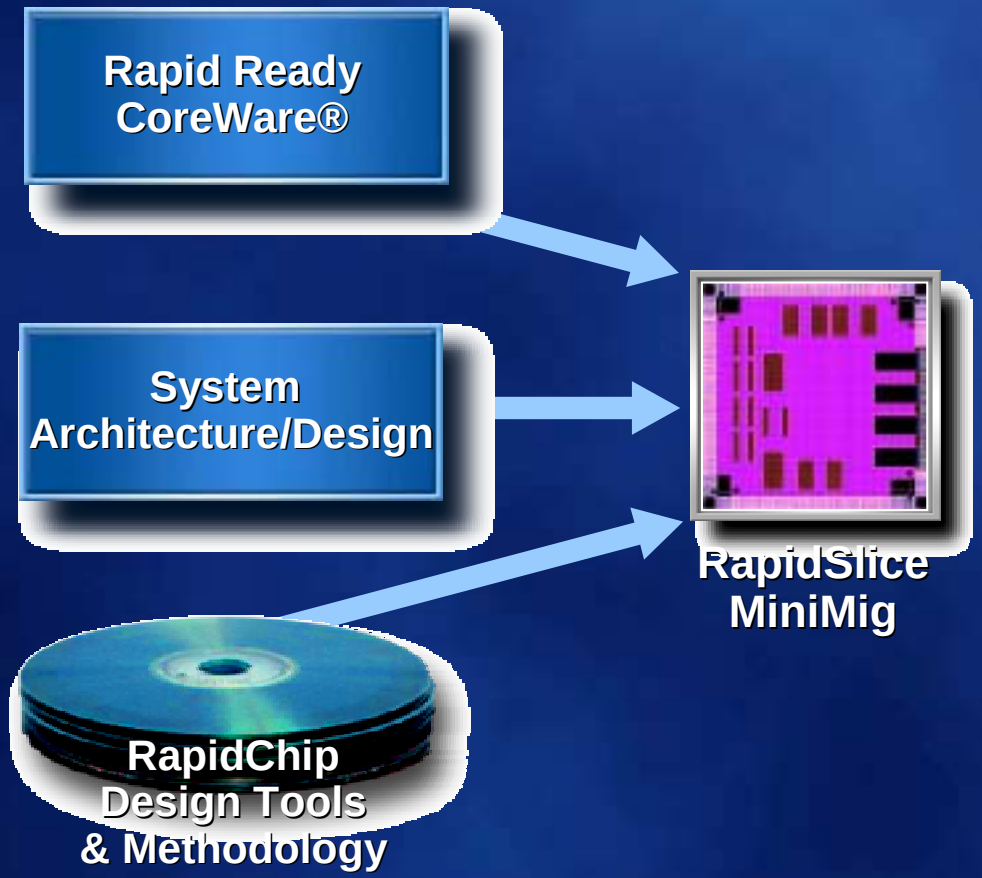
Design Viewer based on OpenAccess



Post Handoff Data Translation Example



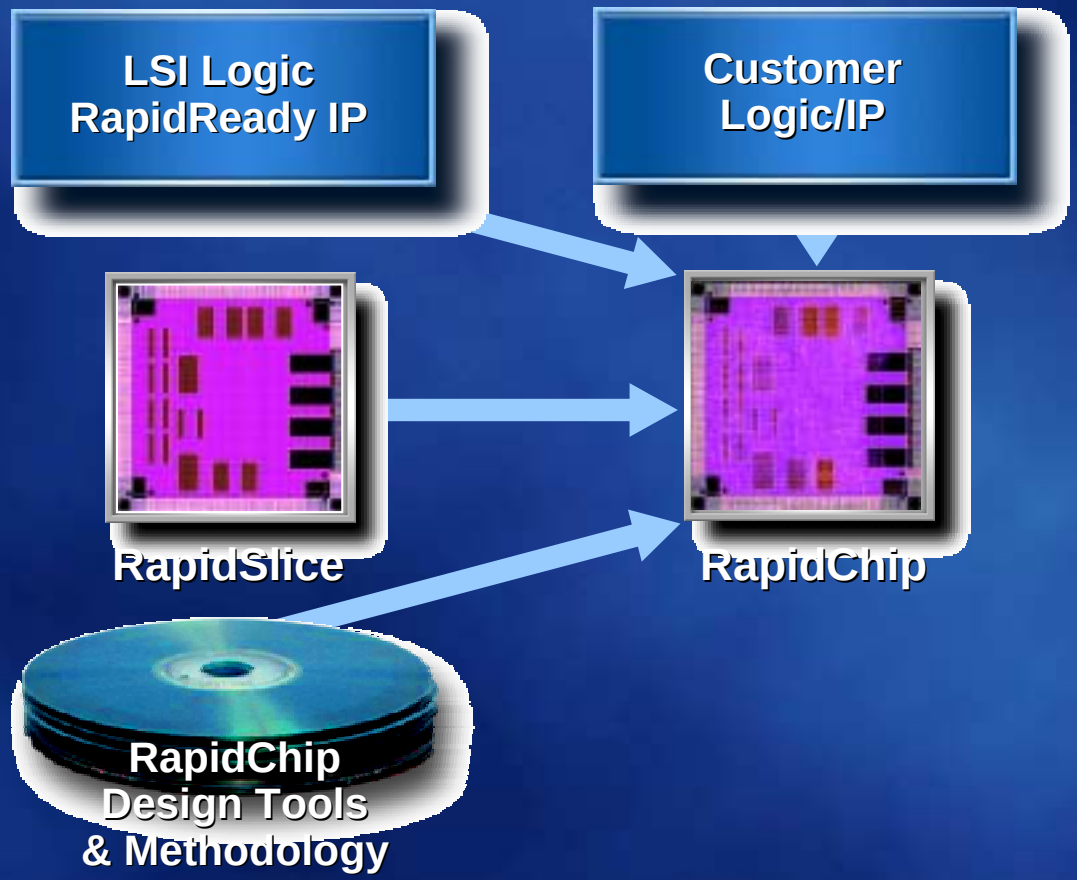
RapidSlice “MiniMig”



RapidSlice “MiniMig”

- Slice Gates
  - 1.5M Customer usable gates
- Slice Memories
  - (6) 2K word x 36 bit 2rw
  - (8) 1K word x 36 bit 2rw
  - (16) 256 word x 36 bit 2rw
  - (4) 4K word x 36 bit 1rw
- Slice Metal Programmable PLL's
  - (4) 100-500Mhz
- Slice Configurable I/Os
  - 390 Customer configurable
  - 660 Wirebond package

RapidChip™ Customer Design



RapidChip™ on MiniMig

- Slice Gates
  - 1.5M Customer usable gates
- Slice Memories
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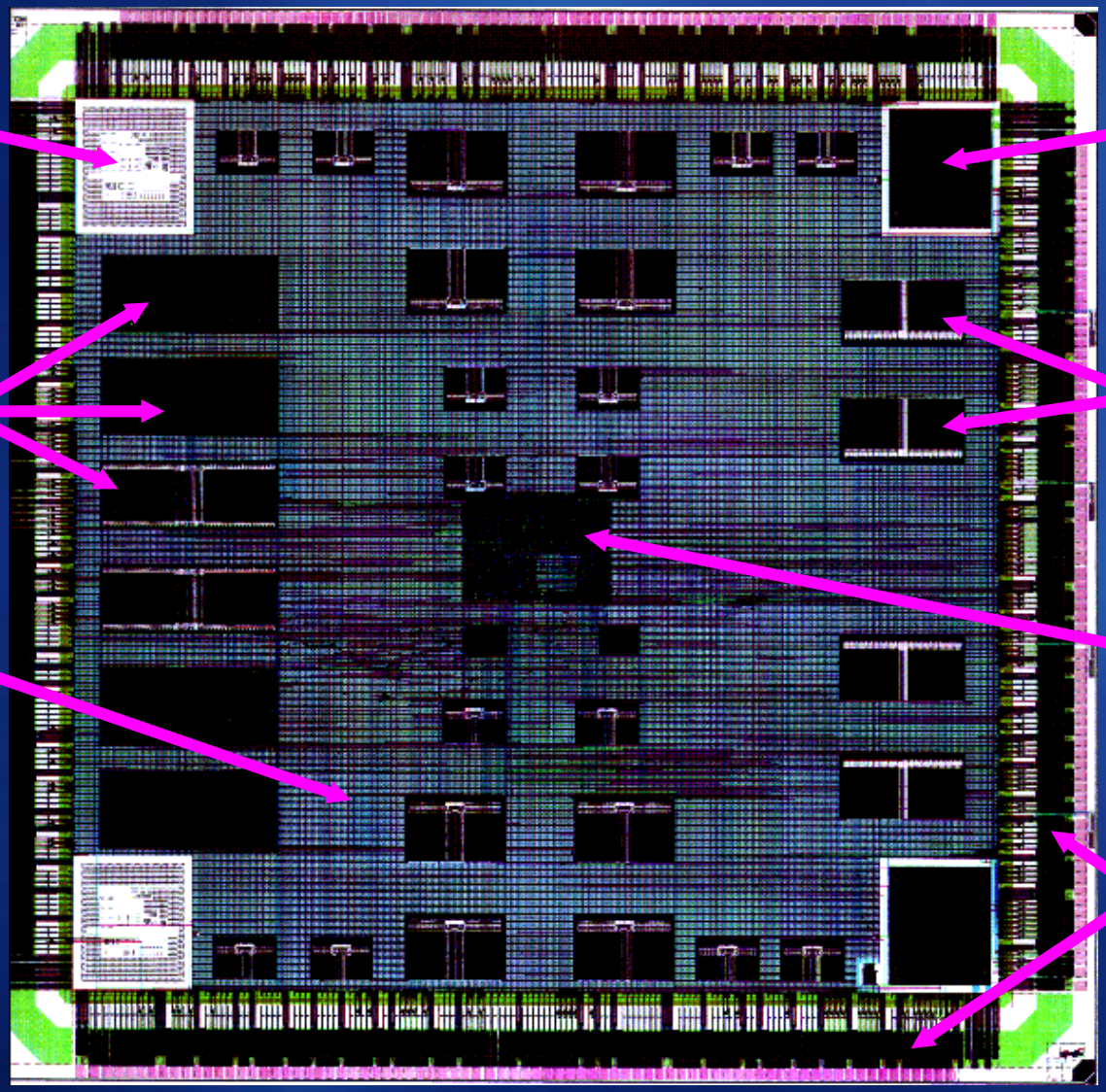
- Slice Metal Programmable PLL's
  - (4) 100-500Mhz
- Slice Configurable I/Os
  - 390 Customer configurable
  - 660 Wirebond package

- Customer Design Gates
  - 84K gates
- Customer Design Memories
  - (4) 2K word x 36 bit 2rw
- Customer Design PLL's
  - (2) 106 Mhz
- Customer Design I/Os
  - 204 2.5v BiDirect

RapidChip™ on MiniMig

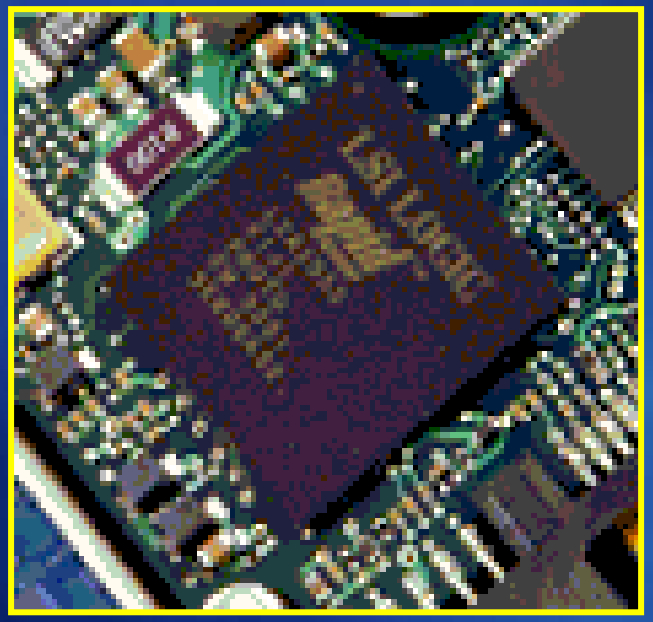


RapidChip™ Integrator Family

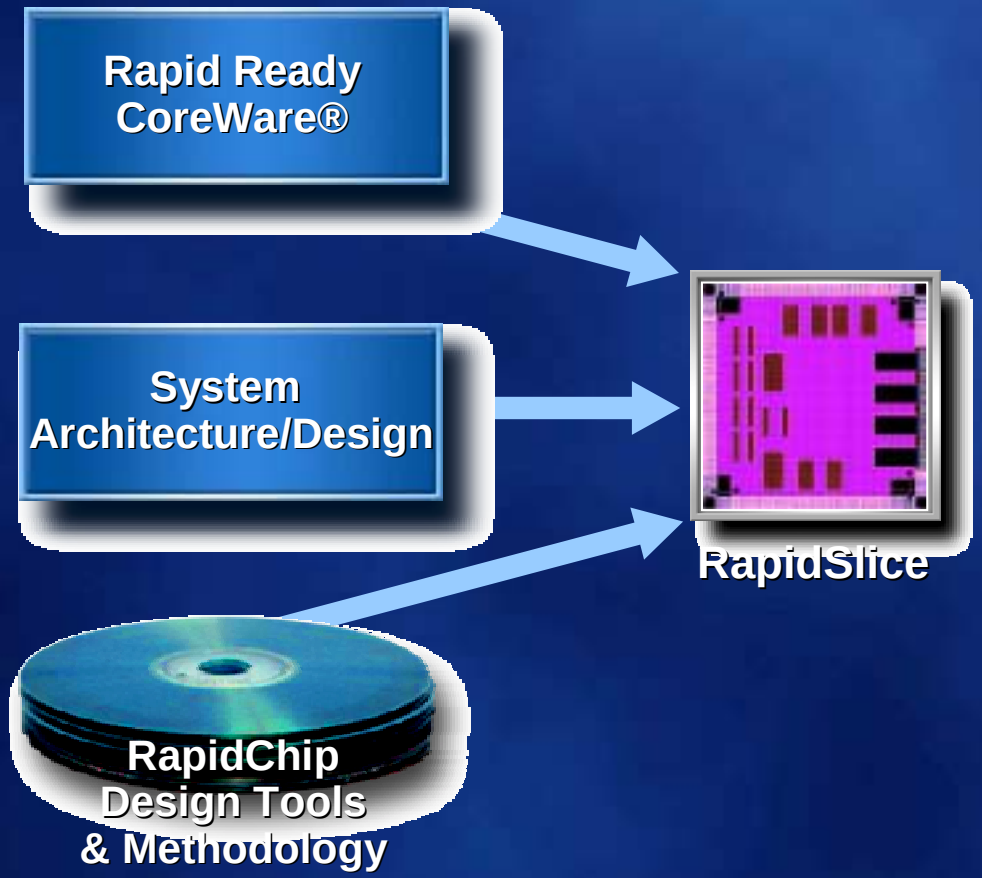
- http://lsilogic.com/products/rapidchip_platform_asic

	Integrator Family (0.11µm)						
	RC11Si210	RC11Si211	RC11Si220	RC11Si221	RC11Si230	RC11Si231	RC11Si240
Available Gates (M)	2.4	4.1	3.4	5.4	5	7	6.3
Min-Max Usable Gates (M)	0.8-1.0	1.6-2.4	1.0-2.0	2.1-3.1	1.9-2.9	2.6-4.0	2.4-3.6
RAM: 111 (1rw) 2k x 72	0	0	0	0	0	0	6
RAM: 111 (1rw) 1k x 36	16	16	16	16	16	16	10
RAM: 222 (2rw) 512 x 36	28	28	12	12	16	16	16
RAM: 222 (2rw) 1k x 36	0	0	8	8	12	12	12
RAM: 222 (2rw) 2k x 36	0	0	12	12	16	16	24
Total RAM Bits (M)	1.1	1.1	2	2	2.5	2.5	3.7
100MHz to 500MHz PLLs	4	4	4	4	4	4	4
Packages							
252 BGA - 171 Max I/O	171	171	171	0	0	0	0
480 BGA - 355 Max I/O	355	355	355	355	355	0	0
672 BGA - 491 Max I/O	0	491	491	491	491	491	491
896 BGA - 683 Max I/O	0	0	0	683	683	683	683
1152 BGA - 803 Max I/O	0	0	0	0	0	803	803

Silicon Proven Products Delivered Rapidly

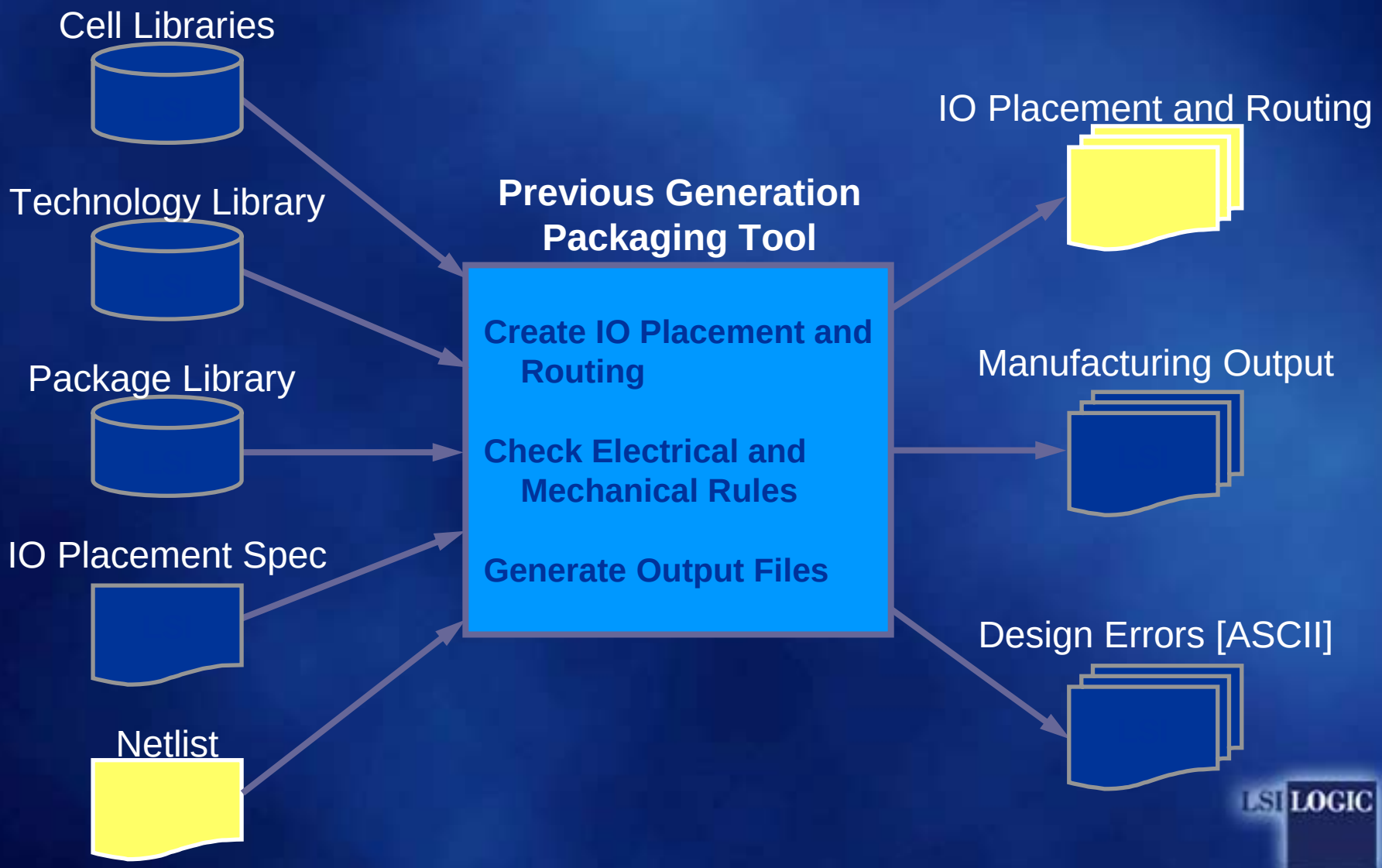


RapidSlice Creation

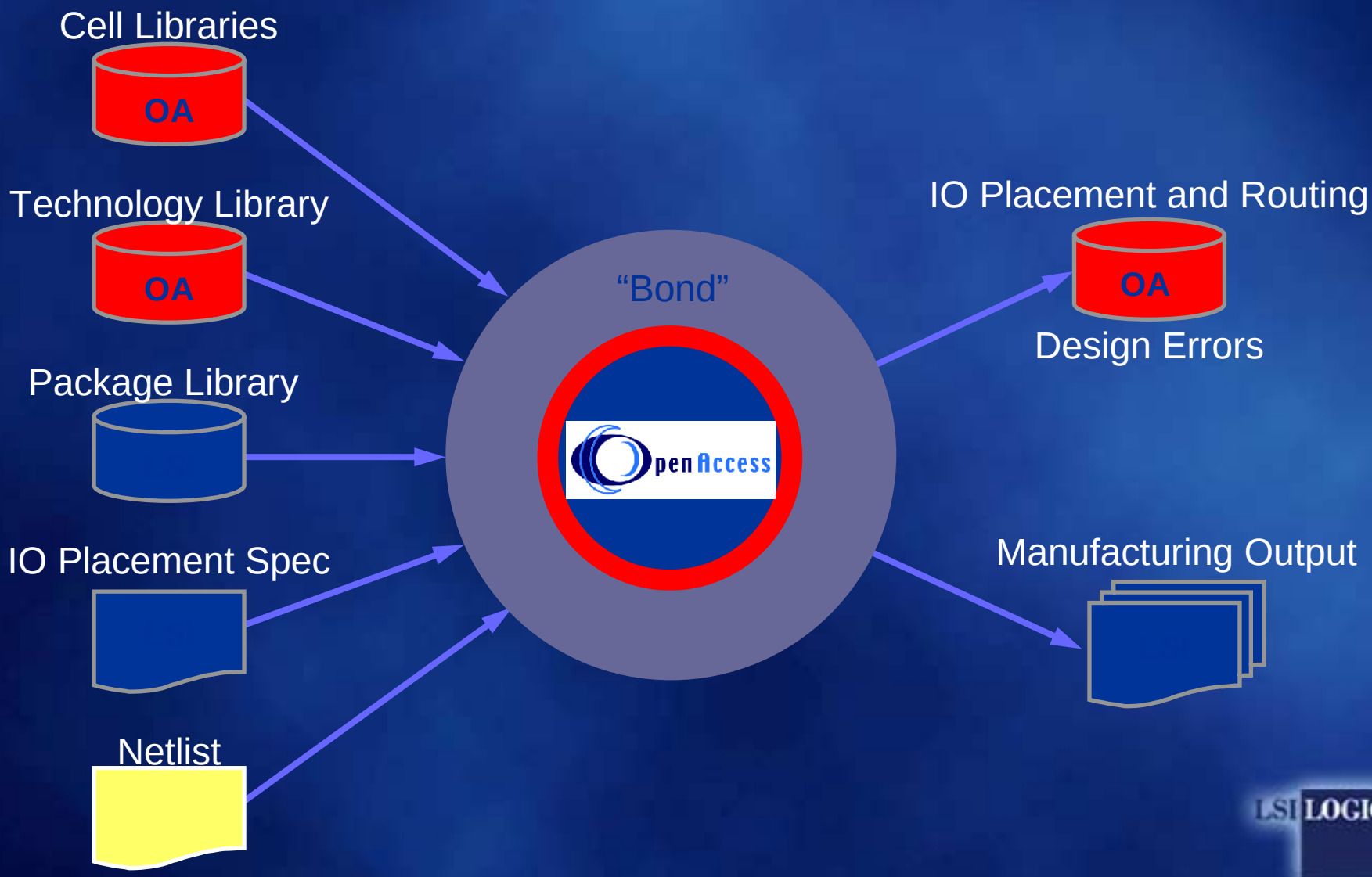


- Creation of the RapidSlice has a package bonding step
- LSI Logic created a new bonding tool based on OpenAccess
- “Bond” serves a dual role in the the creation of RapidSlices and ASICs

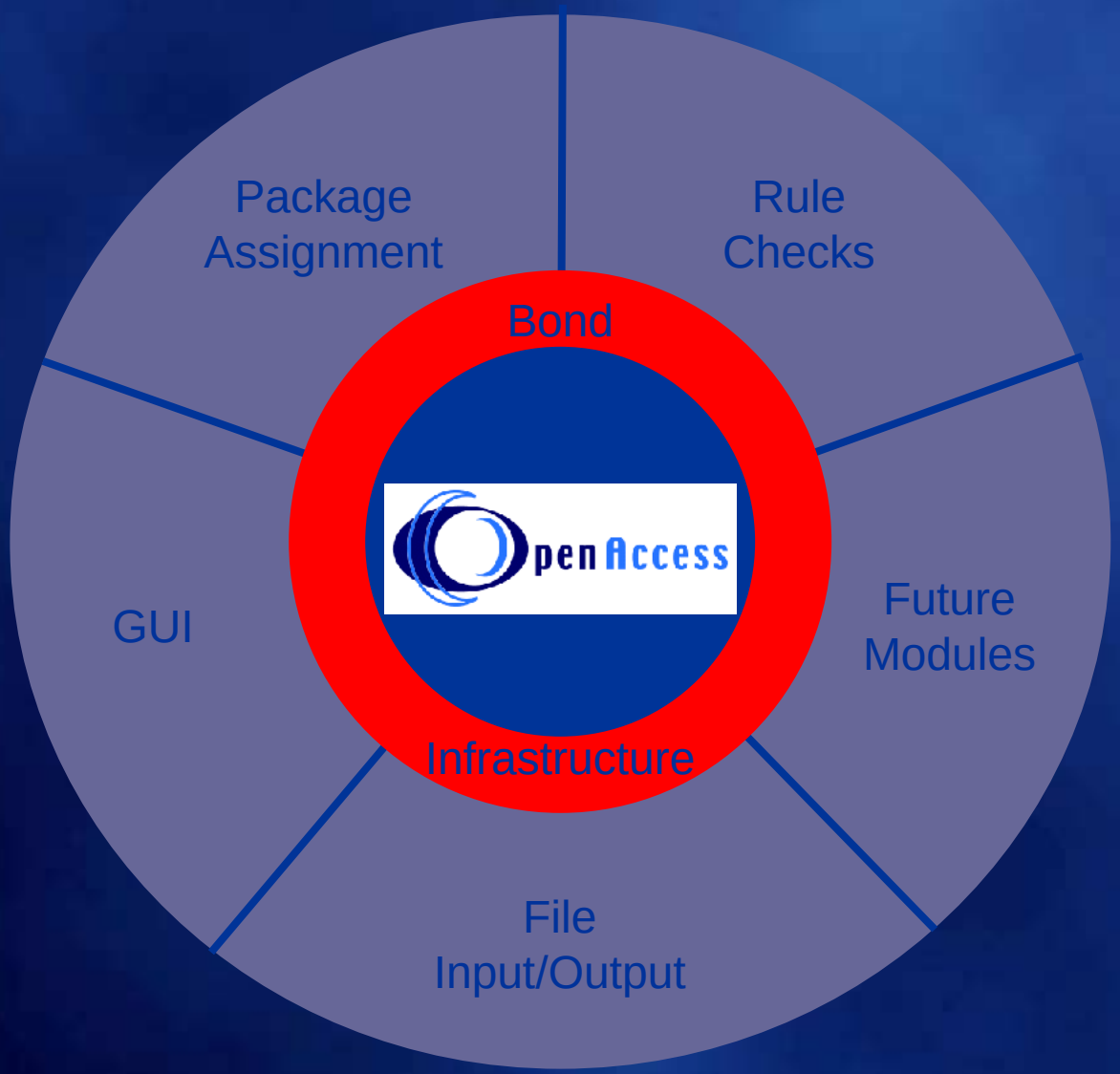
Non-OpenAccess Packaging Tool



OpenAccess Based Packaging Tool



Tool Modularity with OpenAccess



- Modules interface with each other and the main tool via a thin infrastructure.
- Module changes have little impact on other modules.
- Different developers easily work independently.

Why OpenAccess For LSI Logic?

- Source code availability
  - Debugging requires understanding the implementation
- Well defined object data model and methods
  - Enables modular development
  - Extensive API
  - Extensions
- Built-in Support for
  - Callbacks
  - Undo
  - Design Error Infrastructure
- Excellent documentation
- Scripting Interface built-in
- Open Standard
  - Not constrained by proprietary interfaces that are exclusionary
  - Permit best in class tools to work together
- Independent Control
  - Stable environment that won't change if vendors do
    - Design migration to different systems is costly
- No internal tool DB to maintain
  - No need to re-invent the wheel
  - Focus on the value-add
- Ability to make changes
  - Improves responsiveness to our customer needs

Summary

- OpenAccess has been a very positive experience for LSI
  - Its been Open
  - Its been Accessible
- No internal tool database to maintain
  - No need to re-invent the wheel
  - Focus on the value-add
  - Lowers cost
- Ability to make changes
  - Improves responsiveness to our customer needs
- Scheduled releases and Quality of deliverables have been well executed in 2003
- LSI Logic has been effective in leveraging technology
  - Silicon proven RapidChip™ is powered by OpenAccess
  - Expanding usage of OpenAccess